

FOA1252A1

2.5 Gbit/s Transimpedance Amplifier

ICs for Communications



Never stop thinking.

Edition 1998-07

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FOA1252A1**Revision History: 1998-07**

Previous Version:

Page	Subjects (major changes since last revision)

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2.5 Gbit/s Transimpedance Amplifier

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1 Overview

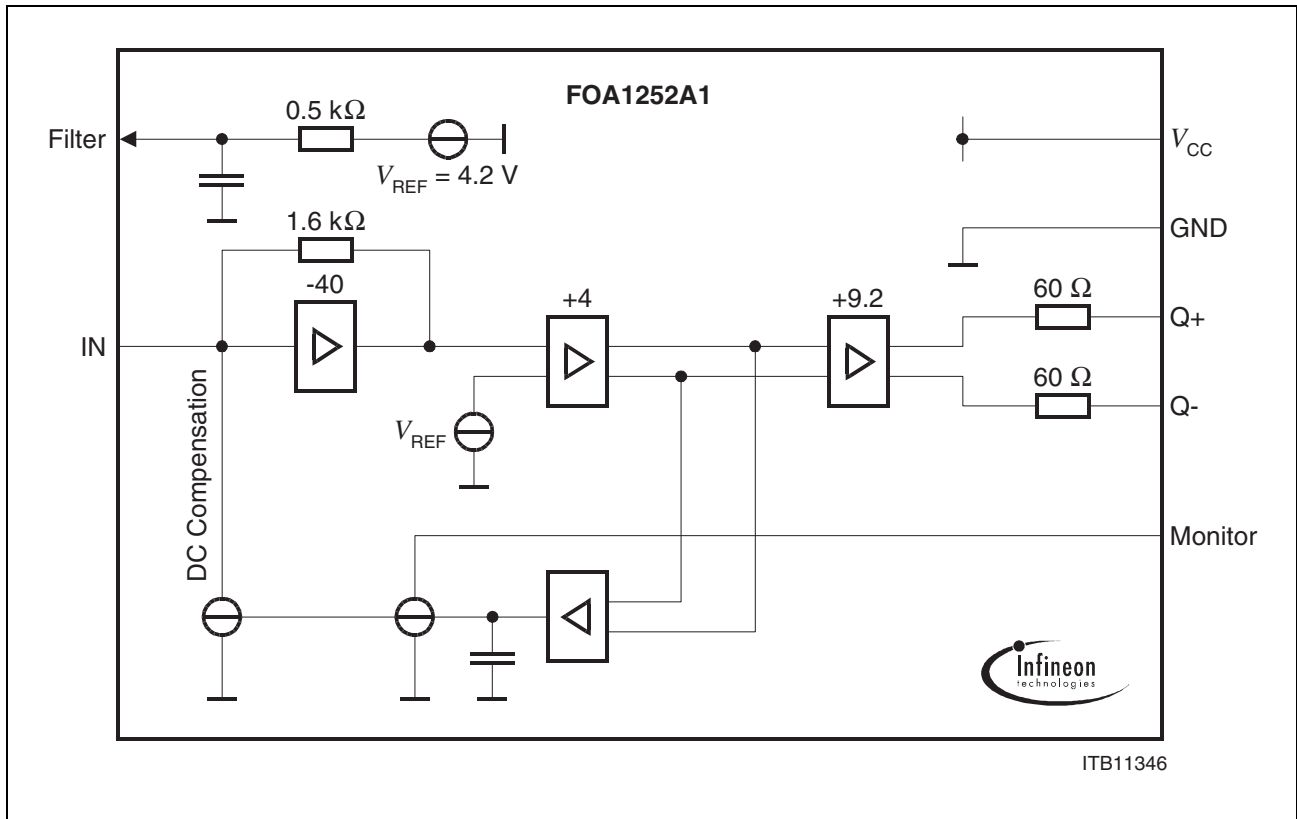
1.1 Features

- Data rate up to 2.5 Gbit/s
- Full ITU-T G958 specification compliance
- Input sensitivity -23.5 dBm at BER = 10^{-9}
- Single supply voltage: +4.5 V to +5.5 V
- Internal DC-compensation loop increases dynamic range
- No external components needed
- Internal bias generation for PIN-photodiode
- Internal low-pass filter to improve power supply rejection
- Operates with PIN- or APD-photodiode
- Monitor output for mirrored photodiode current
- Additional pair of complementary output pins optimized for TO packages

1.2 Applications

- Fibre optics data communication systems: SDH, SONET, ATM, OC, STM
- Pre-amplifier modules

Type	Ordering Code	Package
FOA1252A1	Q67000-H4128	bare die


Figure 1 Block Diagram
Table 1 Pin Description

Symbol	Function
V_{CC}	Supply voltage
IN	Data input from PIN- or APD-photodiode
Q ₊	Non-inverting data output
Q ₋	Inverting data output
FILTER	Bias voltage for PIN-diode
MONITOR	Mirrored photodiode current (connect pin via 0 ... 2 kΩ to V_{CC})
GND	Ground

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Ambient temperature $T_{amb} = -40\text{ °C} \dots +85\text{ °C}$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	V_{CC}	-0.5	6.0	V	–
Junction temperature	T_j	-40	+125	°C	–
Storage temperature	T_S	-40	+150	°C	–
Relative ambient humidity	–	–	85/85	%/°C	no condensation
ESD integrity	V_{ESD}	500	–	V	see note

Note: HBM according to MIL STD 883D, method 3015.7 and ESD Assn. Standard S5.1-1993

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Recommended Operating Conditions

Ambient temperature $T_{amb} = -40\text{ °C} \dots +85\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply voltage	V_{CC}	+4.5	+5.0	+5.5	V	–
Data transmission rate	–	–	2.5	–	Gbit/s	–
Supply current	I_{CC}	–	46.7	–	mA	–
Thermal resistance	Θ_{JA}	–	140	–	K/W	¹⁾
Junction temperature	T_j	-10	–	+125	°C	–

¹⁾ Junction-to-ambient thermal resistance measurement conditions for packaged device:
 PCB area: 10 cm × 10 cm × 1.5 mm; copper area approx. 60%; via holes to ground layer underneath the device; all pins soldered.

2.3 AC/DC Characteristics

 Conditions: $T_{amb} = +25\text{ }^{\circ}\text{C}$, $V_{CC} = +5.0\text{ V}$, $C_{external} = 0.85\text{ pF}$

Parameter	Symbol	Limit Values			Unit	Remarks
		min.	typ.	max.		
Supply current	I_{VCC}	–	47	57	mA	–
Input voltage	V_{IN}	–	+1.65	–	V	–
Input current	I_{IN}	–	–	2200	μApp	¹⁾
Input current before clipping	$I_{IN,CL}$	–	30	–	μApp	–
Input resistance	R_{IN}	–	40	–	Ω	–
Input sensitivity	P_{IN}	–	-23.5	–	dBm	BER < 10^{-9} ¹⁾
Overload	P_{OVL}	–	0	–	dBm	BER < 10^{-9} ¹⁾
Transimpedance	R_T	–	26	–	k Ω	differential into $2 \times 50\text{ }\Omega$
Output voltage swing (Q_+ - Q_-)	ΔV_{OUT}	0.6	0.78	1.1	Vpp	
Bandwidth (-3 dB)	f_{3db}	–	1600	–	MHz	
Output resistance	R_{OUT}	48	60	72	Ω	internally connected to V_{CC}
Output voltage	V_{CMOUT}	–	$V_{CC} - 0.6$	–	V	$(Q_+ + Q_-)/2$
Output pattern jitter ¹⁾	$t_{j,p}$	–	15 45	–	ps	$50\text{ }\mu\text{App} < I_{IN} < 500\text{ }\mu\text{App}$ $500\text{ }\mu\text{App} < I_{IN} < 2\text{ mApp}$
Power supply rejection ratio	$PSSR$	–	35	–	dB	$f < 10\text{ MHz}$ ²⁾
Bias resistance	R_{BIAS}	400	500	600	Ω	–
Bias voltage	V_{BIAS}	–	+4.2	–	V	–
Low frequency cutoff	$f_{3db,low}$	–	65	–	kHz	AC-coupled outputs (via 22 nF)

¹⁾ Data rate: 2.5 Gbit/s; data sequence: PRBS 2²³ - 1, overload measured electrically, 0 dBm = 1 mA average

²⁾ Generated noise on power supply: sine curve, 100 mVpp (see application note b)

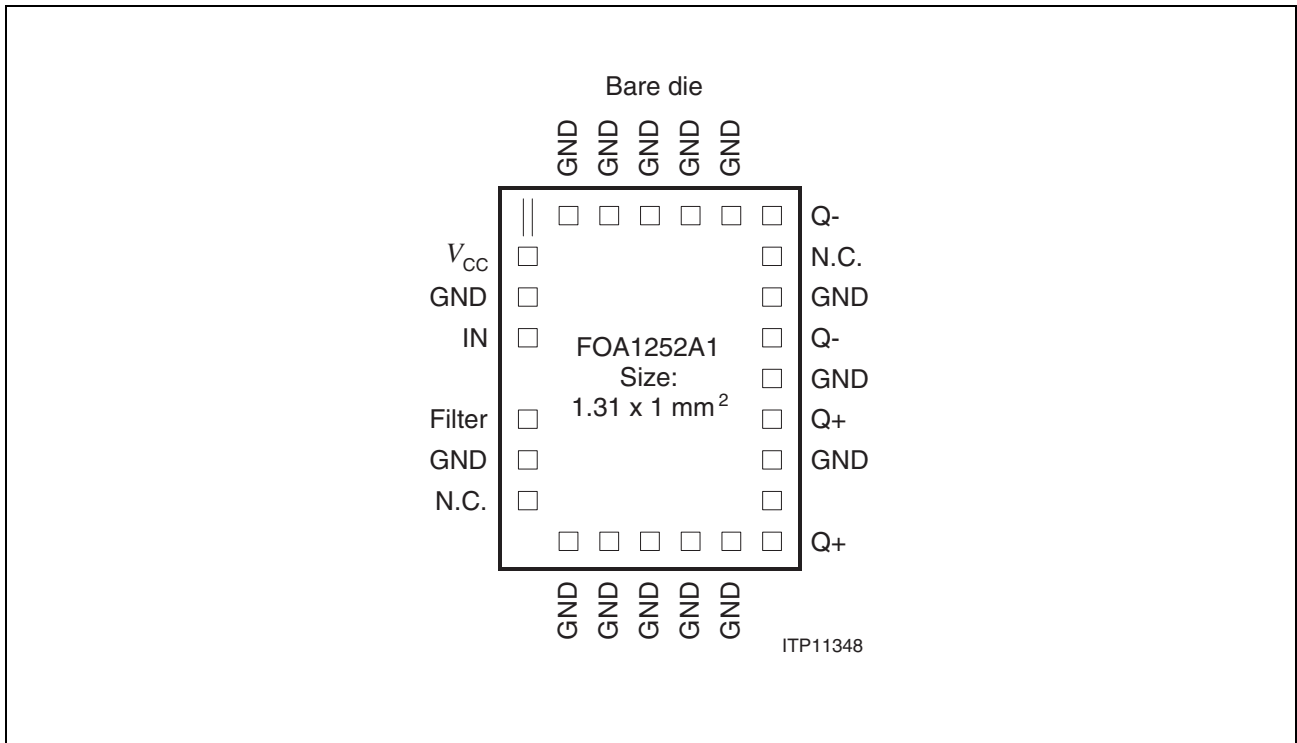


Figure 2 Pad Assignment

2.4 Eye-diagrams Measured at Data Rates of 2.5 Gbit/s

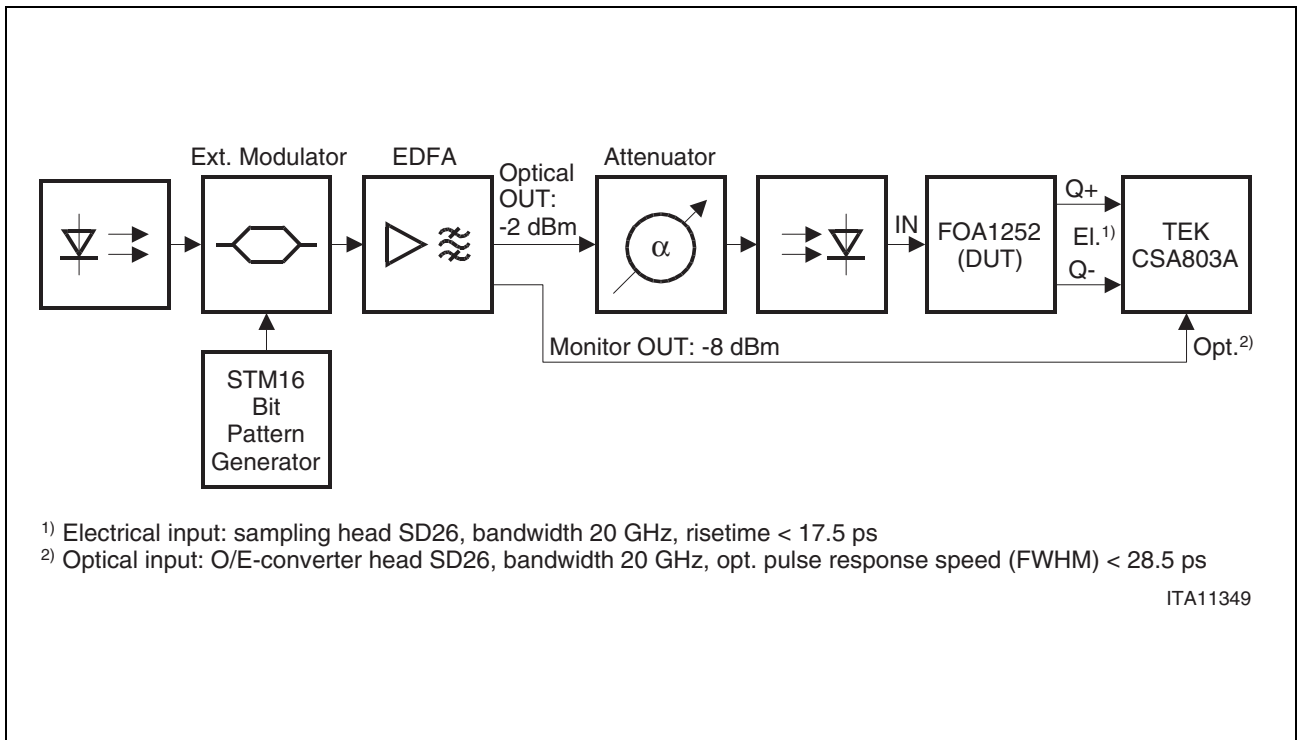


Figure 3 Measurement Set-up

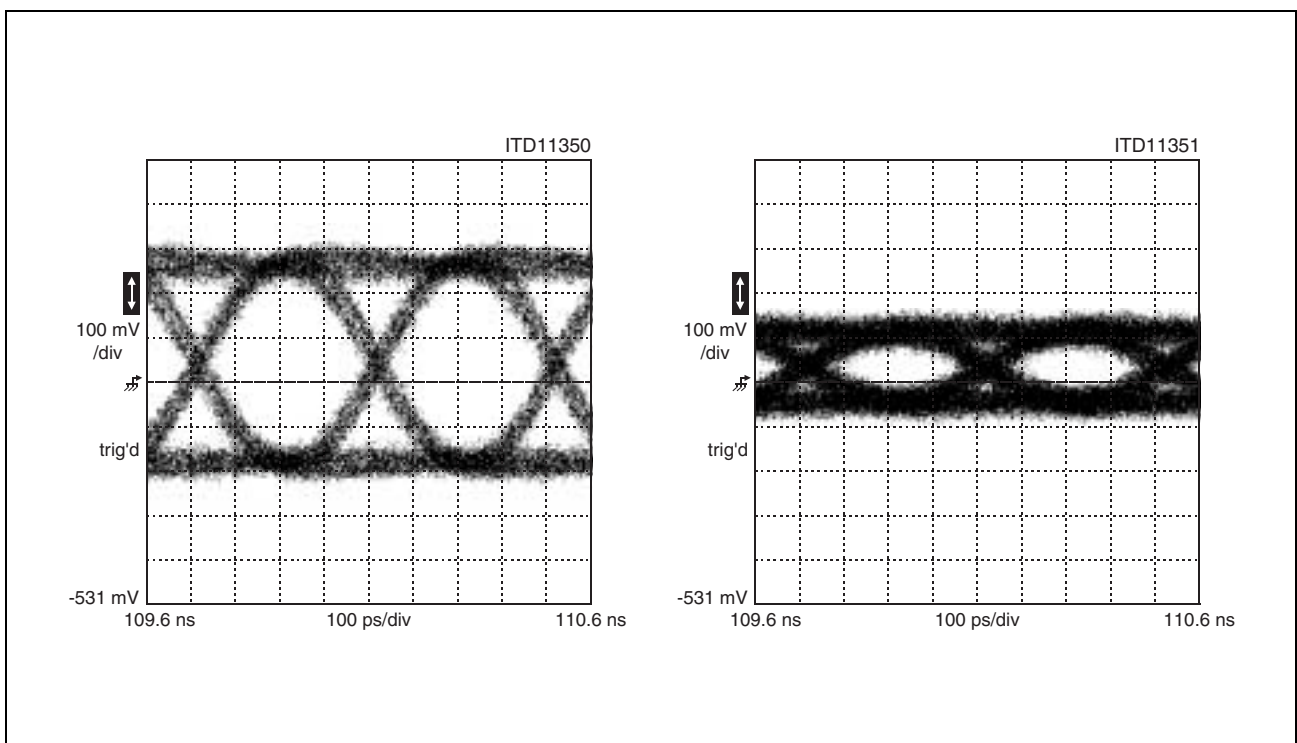


Figure 4 Eye Diagrams at input Power -20 dBm (top) and -25 dBm (bottom)

2.5 Bit Error Rate (BER) Measurements

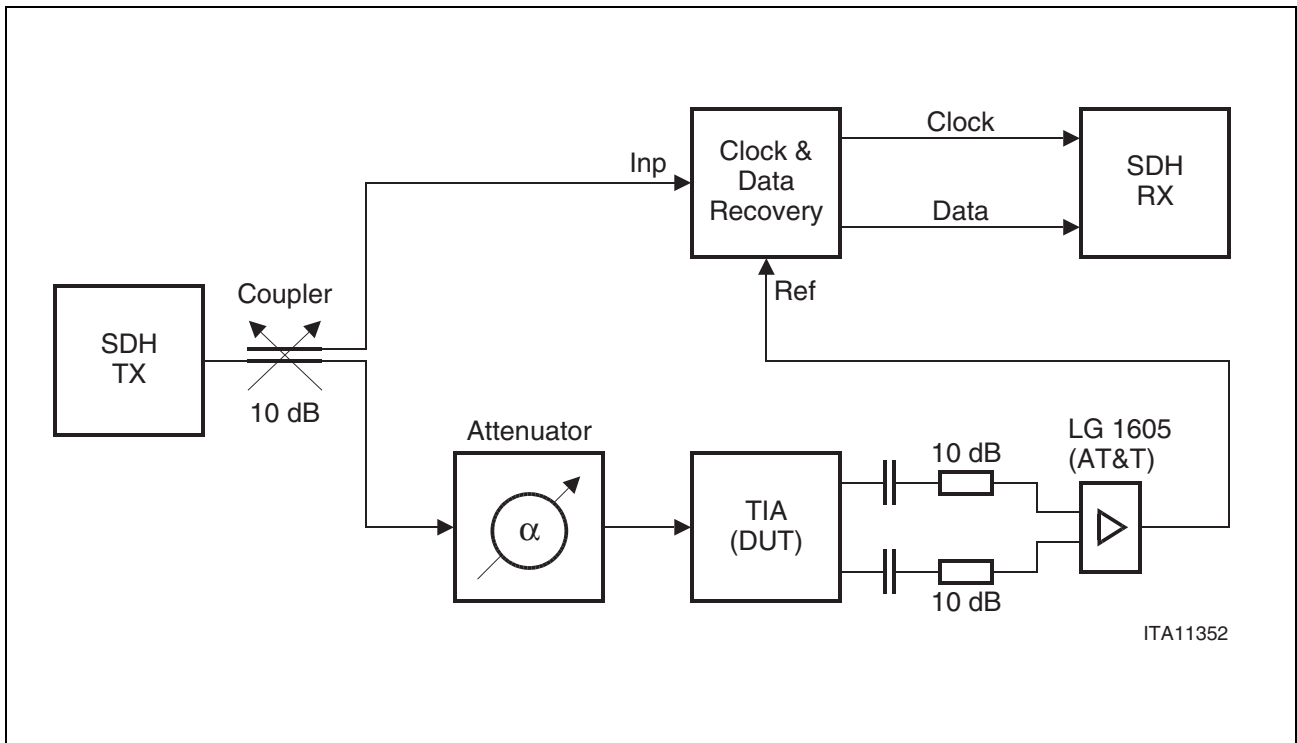


Figure 5 Measurement Set-up

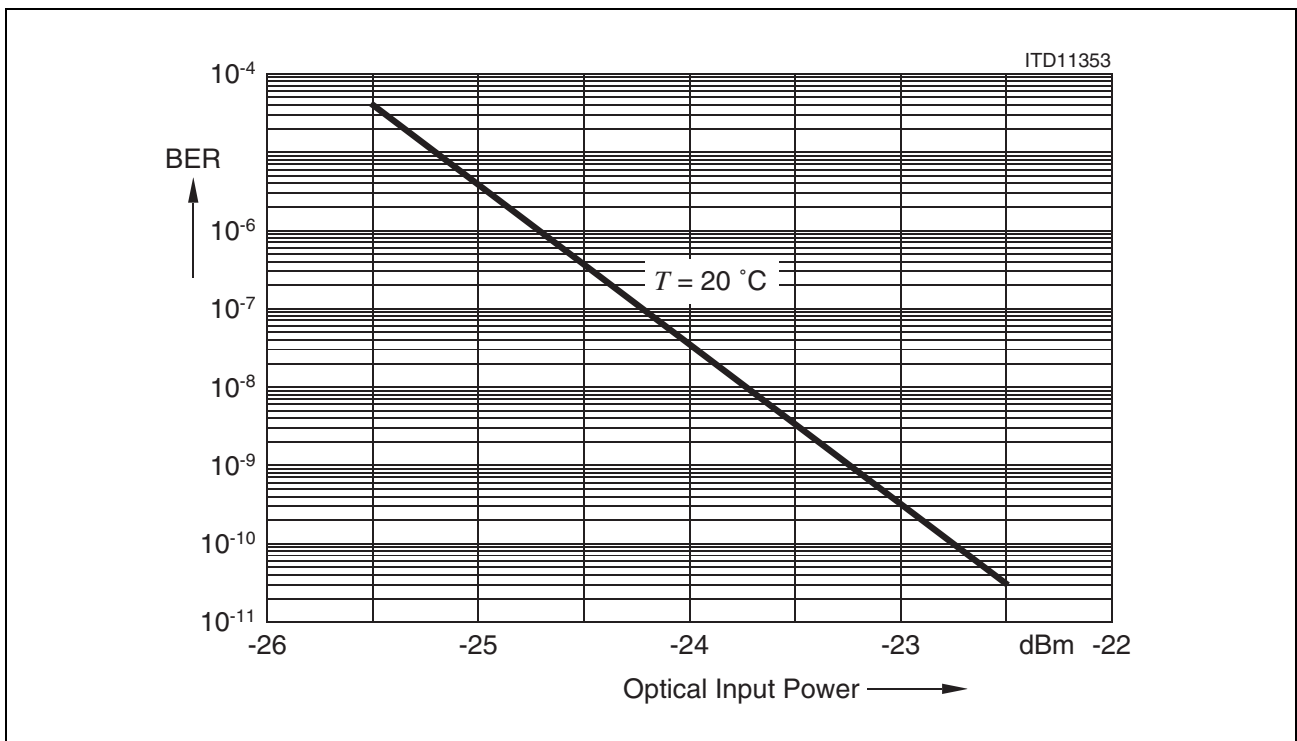


Figure 6 Measured Bit Error Rate for STM-16 Signal

3 Application Notes

a) General information

- The output pins Q_+ and Q_- must be terminated equally to prevent instabilities.
- It is recommended to minimize stray capacitance when connecting photodiode to transimpedance amplifier.
- To improve power supply rejection ratio (*PSRR*), V_{CC} should be supplied via resistor (4.7Ω), capacitor (100 nF) to GND, and inductor (BLM11A601, Murata) to V_{CC} -pin.
- The monitor pin (not used in these application notes) must be left open or connected to V_{CC} via resistor of $0 \dots 2 \text{ k}\Omega$.

b)

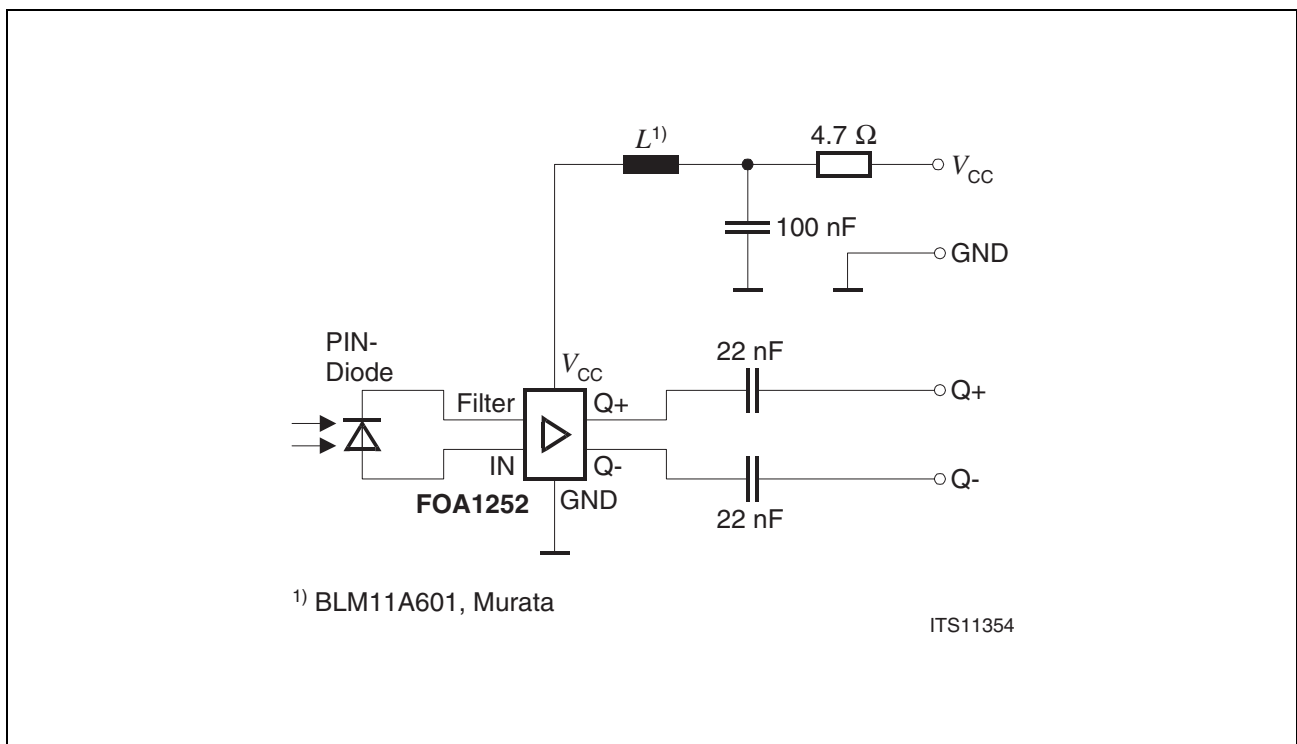


Figure 7 Application Using PIN-photodiode

c)

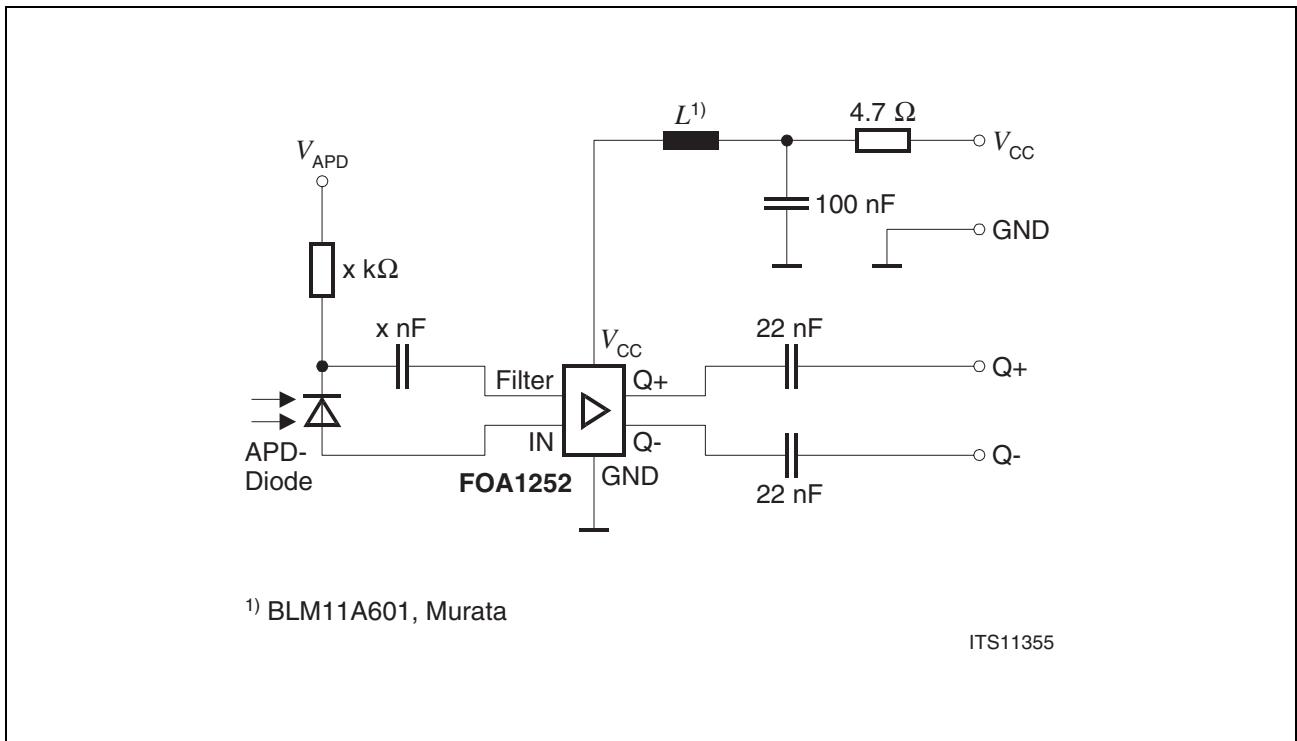


Figure 8 Application Using APD-photodiode

d)

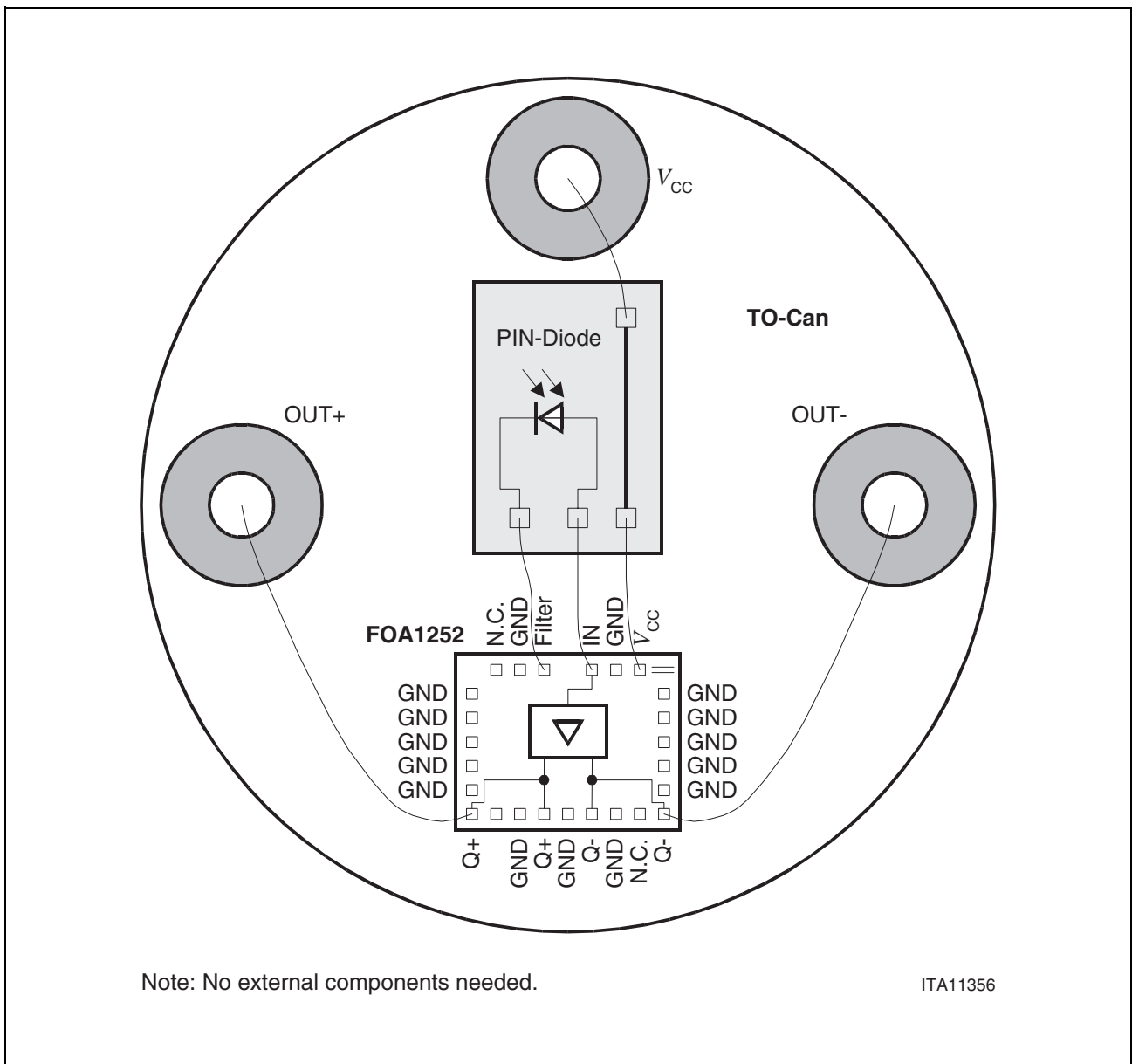


Figure 9 Application Example of FOA1252A1 Mounted in TO-can

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Dr. Ulrich Schumacher

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