GENESYS LOGIC

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GL700FW

ATA/ATAPI to 1394 Native Bridge

SPECIAFICATION 1.1

Dec. 15, 2000

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Index

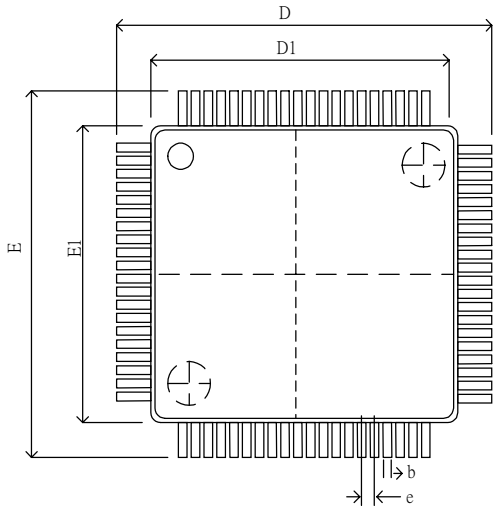
Description

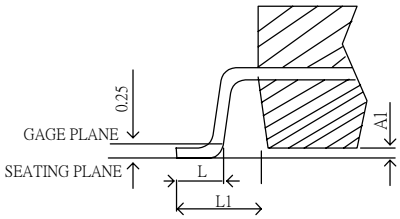
The GL700FW is a high-performance 1394 to ATA/ATAPI native bridge with an embedded SBP-2 target solution. It supports a solution for link/transaction layer controller conforming to the IEEE Std 1394 (IEEE 1394-1995 and IEEE 1394.a) up to 400Mbps transfer rate. It provides a SBP-2 protocol engine to semi-automatically achieve the transport of SCSI command and data over IEEE Std 1394 serial bus. Through the SBP-2 port driver, supported by Microsoft Windows 2000, Windows ME and Windows 98 Second Edition, SCSI class drivers can use SBP-2 to communicate with IEEE 1394 device using the SCSI command set. The GL700FW is ideally suited with hard disk drives, CD-ROM, CD-R, CD-RW and DVD, allowing IDE drives to be connected to a 1394 serial bus in a plug-and-play fashion. Both ATA and ATAPI devices are supported.

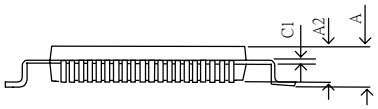
Features

- Data transfer rates of S100, S200 and S400
- Fully interoperable with implementation of IEEE-1394(1995) and IEEE 1394.a-2000 compliant
- Standard PHY/link Interface
- Firmware support for SBP-2 target agent
- Semi-automatic SBP-2 protocol management by an internal hardware engine to improve performance and firmware efficiency
- Auto acknowledge-code response for all packets that targeted to Management/Command ORB agent
- SBP-2 protocol engine
- Semi-automatic Management ORB fetch
- Linked Command ORB fetch
- Auto address increment DMA for both direct and indirect addressing
- Automatic Page Table fetch
- Dedicated asynchronous data transfer
- Automatic packing/de-packing for asynchronous transmit/receive data of DMA
- Semi-automatic single-retry protocol and split transaction control
- Fully ATA-4 compliant
- 2 sets of 4-quadlet registers for Asynchronous Receive/Transmit packet header
- 2 sets of 8-quadlet registers for general Asynchronous Receive/Transmit packet data block payload
- 5 sets of 8/8/2/2/2-quadlet registers for Receive packet data block payload dedicated for SBP-2 requirement (MORB, CORB, PTE, MOP and COP)
- 4K bytes of FIFO for bi-directional transmit/receive data

Package

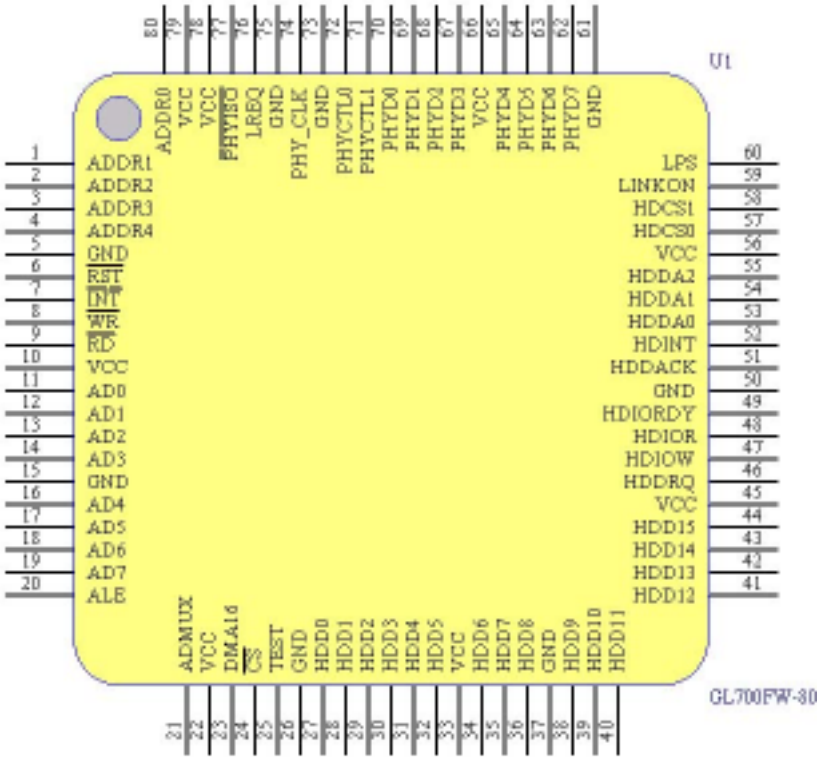






SYMBOLS	MIN	MAX
A	-	1.6
A1	0.05	0.15
A2	1.35	1.45
C1	0.09	0.16
D	14 BSC	
D1	12 BSC	
E	14 BSC	
E1	12 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

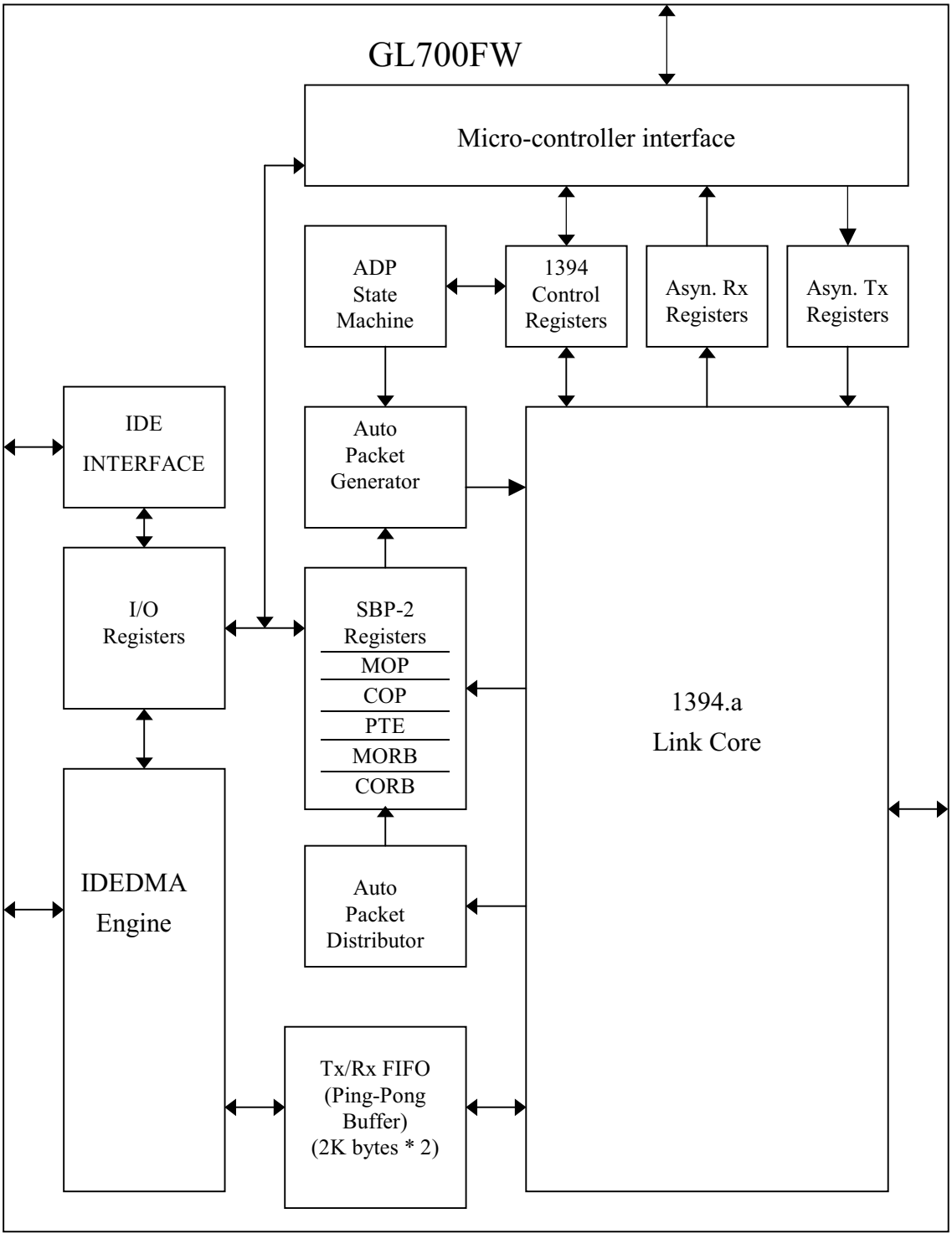
Pin Configuration



Pin Description

PIN	SYMBOL	I/O	DESCRIPTION
6	RST#	I	Master reset signal, low active.
10,22,33, 45,56,66, 78,79	VCC	-	3.3V power supply.
1-4,80	ADDR0-4	I	UP: address bus bit 0 to bit 4 (When set ADMUX = '0'), these address lines are used with CS#, IOR#, and IOW# to access the internal I/O registers.
9	RD# /	I	UP: this active low signal enables the reading of internal register.
8	WR# /	I	UP: this active low signal enables the writing of internal register.
11-14, 16-19	AD0-AD7	I/O	UP: address & data bus bit 0 to bit 7(When set ADMUX = '1'). UP: data bus bit 0 to bit 7(When set ADMUX = '0').
5,15,26,3 7,50,61,7 3,75	GND	-	Ground.
20	ALE	I	ALE is used to enable the address latch that separates the address from the data.
21	ADMUX	I	ADMUX is used to indicate the address & data bus is separated or not.
23	DMA16	I	This bit is used to enable 16-bits DMA function.
25	TEST	I	This bit is used only in test mode. This bit must tie low in normal.
7	INT#	O	This is an output pin to drive the active low interrupt signal to external controller.
24	CS#	I	This active low signal acts as the chip select during register access cycle.
52-54	HDA0-2	O	IDE device address. The 3-bit binary coded address asserted by the ATA host to access a register or data port in the device.
57	HDCS0#	O	IDE chip select 0. The chip select signal from the ATA host used to select the Command Block registers.
58	HDCS1#	O	IDE chip select 0. The chip select signal from the ATA host used to select the Control Block registers.
47	HDIOW#	O	IDE device I/O write. The write strobe signal from the ATA host.
48	HDIOR#	O	IDE device I/O read. The read strobe signal from the ATA host.
27-32, 34-36, 38-44	HDD0-15	I/O	IDE device data. The 8- or 16-bit data bus to/from the ATA device. Only the lower 8 bits are used for 8-bit register transfers.
49	HDIORDY	I	IDE I/O channel ready in. This signal is de-asserted by the device when the current transfer is not ready to proceed.
52	HDINT	I	IDE device interrupt. This input signal is used to interrupt the host system when interrupt pending is set.
51	HDDACK#	O	IDE DMA acknowledge. This signal is used by the ATA host in response to DMARQ to initiate DMA transfers.
46	HDDRQ	I	IDE DMA request. This signal is asserted by the ATA device when it is ready to perform a DMA data transfer to or from the ATA host when a DMA operation has been enabled.
59	LINKON	I	Request Link to power up when in a low power mode.
60	LPS	O	LPS for PHY Mode. Contend for LINK Mode and Normal Mode
71,72	PHY_CTL1 PHY_CTL0	I/O	Control1 and Control 0 of the PHY-link control bus. CTL1 and CTL0 indicate the four operations that can occur in this interface.
76	LREQ	O	Link request. LREQ is an output that makes bus requests and accesses the PHY layer.
62-65, 67-70	PHY_D7-0	I/O	PHY data7 through data0 of the PHY-link data bus. Data is expected on D0-D1 for 100Mb/s packets, D0-D3 for 200Mb/s, and D0-D7 for 400Mb/s.
74	PHY_SCLK	I	System clock. PHY_SCLK is a 49.152-MHz clock from the PHY, that generates the 24.576 clock.
77	PHY_ISO#	I	Isolation barrier(active low). This ISO# is asserted (low) when an isolation barrier is present.

Block Diagram



Block Outline

The GL700FW is designed to simplify the firmware issue of μP and save hardware cost. Upon the completion of a packet reception, the GL700FW will automatically respond acknowledge code according to the destination offset and generate the corresponding interrupt to inform the firmware to check the received packet is met with SBP-2 and 1394 protocol or not. The data payload dedicated to SBP-2 protocol is moved to the specified registers so that firmware can easily inquire and reply the data packet according to the received packet if necessary. The μP has to do is to set "1394 instruction register" properly and then the internal SBP-2 engine will automatically collect all fields from SBP-2 registers to generate the data packet.

For the SCSI command that requested from initiator, firmware need to transfer these commands to ATA/ATAPI commands, and write them to IDE device through I/O register to access IDE interface.

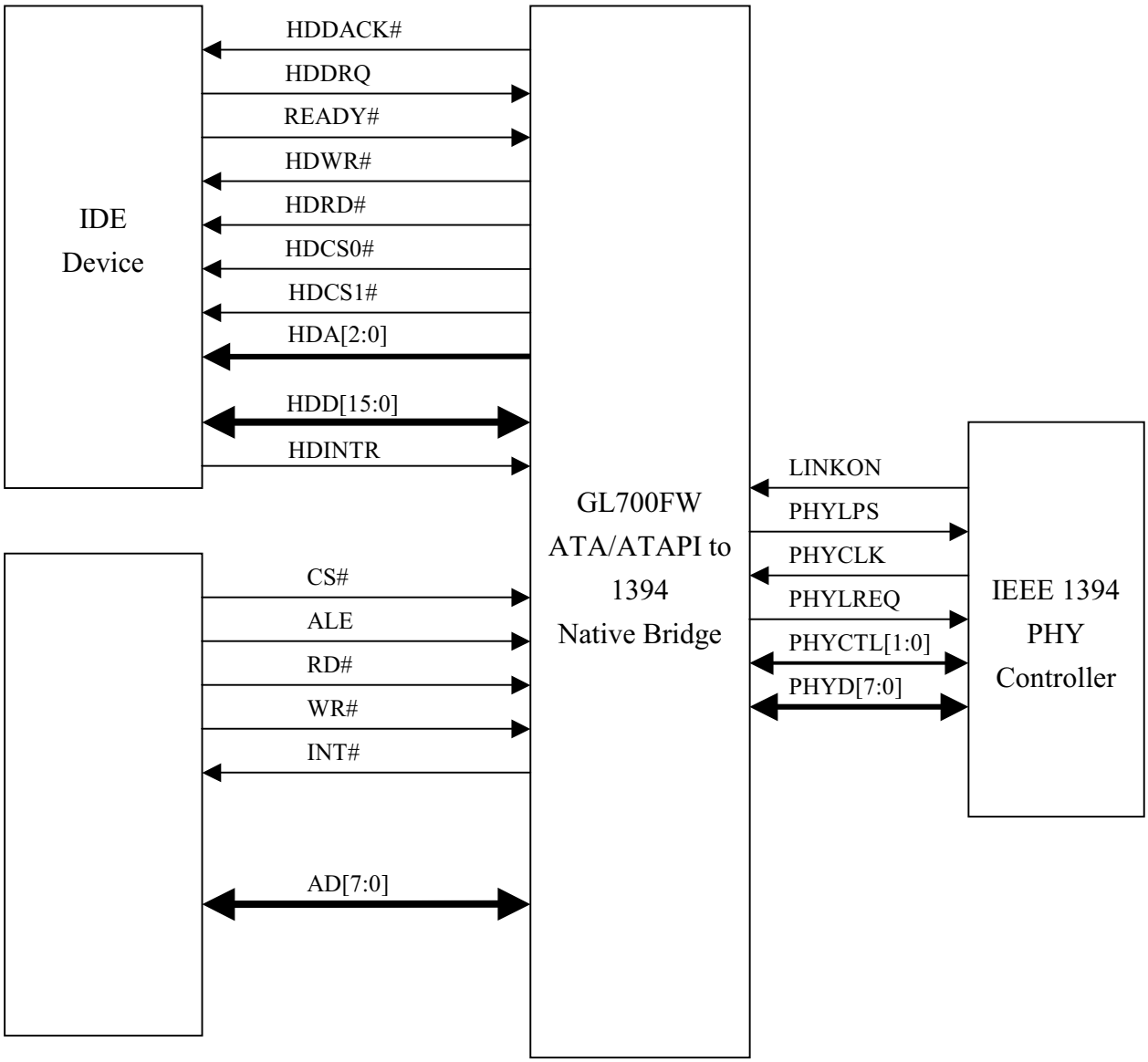
GL700FW architecture:

1. **Asyn Tx registers:** general asynchronous packet transmit registers, 4-quadlets for 1394 header and 8-quadlets for data payload. After getting all fields of packet ready, the firmware can set “AsynTx” instruction to send the packet. Some packets to transmit like “Login Response”, “Query Login Response” and “Status Block” packet are prepared by the registers whose maximum data payload is 8 quadlets.
2. **Asyn Rx registers:** general asynchronous packet receive registers, 4-quadlets for 1394 header and 8-quadlets for data payload. The received packet other than the SBP-2 associated read response packets, like "Config ROM Read Request" from the initiators, is stored in the registers. However, all the SBP-2 read response packet received from the initiators are always expected by the target and forwarded to the Auto Packet Distributor.
3. **1394 Control Registers:** control and interrupt registers for IEEE 1394 and SBP-2 protocol, see the details in the section of 1394 control register.
4. **ADP State Machine:** Automatic data pipe control for SBP-2 data transfer and page table fetch.
5. **Auto Packet Generator:** generate the read or write request packet header of those packets with standard format like Config ROM read response packet, Management ORB read request, Command ORB read request, Page Table read request, Block data read request from or write request to initiator.
6. **Auto Packet Distributor:** The data payload of SBP-2 associated packet is stored at the specified registers according to its destination offset, Tlabel or last request packet command. The received data payload is classified by the GL700FW to 7 types: Management ORB agent pointer(2 quadlets), Command ORB agent pointer(2 quadlets), Management ORB(8 quadlets), Command ORB(8 quadlets), Page Table pointer(2 quadlets), general Rx data payload(8 quadlets), and general data moved from or to initiator.(1K quadlets).
7. **SBP-2 Registers:** the registers for received data payload of SBP-2 associated packet including Management ORB agent pointer(2 quadlets), Command ORB agent pointer(2 quadlets), Management ORB(8 quadlets), Command ORB(8 quadlets) and Page Table pointer(2 quadlets).
8. **Tx/Rx Data FIFO:** 4Kbytes of ping-pong buffer for data moved between the initiator and target.
9. **IDEDMA Engine:** interface to IDE device and automatically access data IDE DMA mode.
10. **I/O Control Registers:** a register space to store information about status, packet and chip, accessible by

system ASIC and µP.

11. **IDE Interface**: an interface for accessing IDE device internal registers.

System Block Diagram



I/O Registers Summary

Mnemonic	Offset	Description	Remarks
VERSION	0	Version number of this chip	
SCSIDATA	1	SCSI Command data register	
INTSTS	2	Interrupt status	
INTEN	3	Interrupt enable	
MISC	4	Miscellaneous register	
FIFOPORT	5	FIFO port for read/write entry	
FIFOSTAT	6	FIFO status	
PacketSizeHi	8	Data size high byte for current packet	
PacketSizeLo	9	Data size low byte for current packet	
FIFOFLAGHi	A	Byte counter high byte in the FIFO	
FIFOFLAGLo	B	Byte counter low byte in the FIFO	
IDEADDR	C	Control & address bits for IDE	
IDEDATALo	D	Data Low for IDE	
IDEDATAHi	E	Data High for IDE	

VERSION (offset 0)

Read Only
Version Number

SCSIDATA (offset 1)

R/O	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
SCSID7	SCSID6	SCSID5	SCSID4	SCSID3	SCSID2	SCSID1	SCSID0

This register is used to buffer the SCSI command in SBP-2 command block ORB up to 12 bytes. The GL700FW will set the status bit SCSISTS and generate an interrupt to inform the external ASIC of having received SCSI command by the GL700FW. And then the ASIC can read the SCSI command one by one in byte from this register.

INTSTS (offset 2)

R/U	*R/U*	*R/U*	*R/W/C*	*R/W/C*	*R/O*	*R/W/C*	*R/O*
INT	1394STS	IDESTS	FIFOSTS	NxtPktSTS	Reserve	SCSISTS	Reserve

INT: This bit responds the state of interrupt.

1394STS: This bit represents the value of INTSTS of INTSTAT register (offset 13h).

NxtPktSTS: A new packet is requested. If the direction is move from initiator to target, this bit will be asserted to indicate a read response block packet is received. If the direction is from target to initiator, this bit will be asserted when the write request block packet is transmitted completely.

SCSISTS: Set when a new SCSI command is received.

FIFOSTS: This bit is a wire-or of FIFOSTAT register. When any bit of FIFOSTAT register is set, this bit will be asserted. A write one action will clear the related interrupt bit.

IDESTS: This bit represents the status of the hard-disk interrupt pin, only clear the hard-disk interrupt pin can clear this interrupt.

INTEN (offset 3)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
INTJEN	1394INT	IDEINT	FIFOINT	NxtPktINT	Reserve	SCSIINT	Reserve

INTJEN: Enable responds the state of pin IRQJ.

1394INT: Enable interrupt when 1394STS bit is set.

NxtPktINT: Enable interrupt when a Next packet signal is set.

SCSIINT: Enable interrupt when a new SCSI command is received.

FIFOINT: Enable interrupt after a FIFO status condition is detected.

IDEINT: Enable interrupt after a hard-disk status condition is detected.

MISC (offset 4)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
UNION	StartSCSI	IDEPIO	Reserve	Reserve	PIO/DMA	DRQREL	DBLOCK

DBLOCK: DMA mode select. 0: single transfer, 1: block transfer.

DEGLITCH: Enable DRQ release option for DMA signals.

PIO/DMA: Data transfer through PIO or DMA interface. 0: DMA mode, 1: PIO mode. If you need to access the incoming data in FIFO, change them and then write to hard-disk, you need to set PIO/DMA as “1” and then read out or write in data through FIFO port.

IDEPIO: This bit is used for firmware to move data through FIFO by accessing data port 1F0. When this bit is set as “1”, firmware can access data port 1F0 without setting the IDEDATAHI & IDEDATALO registers, if you want to read data from hard-disk, just write IDEADDR register with “0x80”, the data read from hard-disk will be written to FIFO. And write value “0x40” to IDEADDR register will cause hardware get a word from FIFO and write it to hard-disk. (When IDEPIO and ENIDE is set, all read or write operation to 1F0 port is through FIFO, not through IDEDATAHi or IDEDATALo register).

StartSCSI: This bit is used for external μP to initiate the starting address of SCSI command, this bit is written once cleared.

UNION : This bit is used for FIFO union, when set as 1, the FIFO is union, when 0, FIFO is separate as a ping-pong buffer.

FIFOPORT (offset 5)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
FFD7	FFD6	FFD5	FFD4	FFD3	FFD2	FFD1	FFD0

This register is used for PIO mode to transmit and receive data through a write or read action to this register. When the direction is from initiator to target, read this register can get the data out from FIFO. If the direction is from target to initiator, write this register can move the data to FIFO.

FIFOSTAT (offset 6)

				R/U	*R/U*	*R/U*	*R/U*
				FIFOA Full	FIFOF ull	FIFOAE mpty	FIFOE mpty

FIFOEmpty: This bit is set when the FIFO flag is equal to zero.

FIFOFull: This bit is set when the FIFO flag is equal to value of packet_size.

FIFOAEmpty: This bit is set when the FIFO flag is equal to 4.

FIFOAFull: This bit is set when the FIFO flag is equal to value of packet_size - 4

PKTSIZEHi (offset 8)

R/U	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*
PktSize15	PktSize14	PktSize13	PktSize12	PktSize11	PktSize10	PktSize9	PktSize8

PKTSIZELo (offset 9)

R/U	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*
PktSize7	PktSize6	PktSize5	PktSize4	PktSize3	PktSize2	PktSize1	PktSize0

These two registers, PKTSIZEHi and PKTSIZELo, are used for PIO mode. When a new packet is requested, the GL700FW will generate an interrupt and also update these two registers to indicate the needed packet size for the following transfer.

FIFOFLAGHi (offset A)

R/U	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*
ByteCnt	ByteCnt	ByteCnt	ByteCnt	ByteCnt	ByteCnt	ByteCnt	ByteCnt

15	14	13	12	11	10	9	8

FIFOFLAGLo (offset B)

R/U	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*	*R/U*
ByteCnt 7	ByteCnt 6	ByteCnt 5	ByteCnt 4	ByteCnt 3	ByteCnt 2	ByteCnt 1	ByteCnt 0

These two registers, FIFOFLAGHi and FIFOFLAGLo, combine to indicate the byte counts of data in the FIFO.

IDEADDR (offset C)

R/W/U	*R/W/U*	*R/W/C*	*R/W*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
RDREQ	WRREQ	RDDON	WRDON	CS1/CS0	ADDR2	ADDR1	ADDR0

IDEDATALo (offset D)

R/W/U	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

IDEDATAHi (offset E)

R/W/U	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8

These three registers are used for IDE PIO mode programming, for IDE PIO mode, there are 8 ports in address range 1F0~1F7(CS0), and one port for 3F6(CS1), and only 1F0 port is 16-bits operation, for write operation, you need to put the data in IDEDATALO register (for all registers), IDEDATAHI register(only 1F0 port operation) and then set WRREQ and CS1/CS0 and ADDR2~ADDR0 bits in IDEADDR register. When write operation is completed, the WRREQ will be clear and WRDONE bit will be set. For read operation, you can set WRREQ and CS1/CS0 and ADDR2~ADDR0 bit in IDEADDR register. When read operation is completed, the RDREQ will be clear and RDDONE bit will be set. And the data for this read request port will be represent in IDEDATALO and IDEDATAHI (only for 1F0 data port) register.

For example: if you want to read 1F7 port, you need to set “0x87” to IDEADDR register, after this operation is completed, the value in IDEADDR register will be set as “0x27”, and the value for this port will be set at IDEDATALO register. If you want to write 1F0 port, you need to set the IDEDATAHI and IDEDATALO (For ATAPI packet command only, the IDEPIO bit in MISC register must be set as “0”) registers for 16-bits data port operation, and then set “0x40” value to IDEADDR register, when this operation is completed, the value in IDEADDR will be “0x10”.

These three registers are only active when ENIDE pin is set to high.

1394 Register Summary

Mnemonic	Offset	Description	Remarks
1394INST	0	1394 instruction register	
1394CTL	1	1394 control register	
INTMASK	2	Interrupt mask register	
INTSTAT	3	Interrupt flag register	
SBPCTL	4	SBP-2 control register	
SBPSTS	5	SBP-2 status register	
TXSTAT	6	Transmit status register	
RXSTAT	7	Receive status register	
1394ADR	8	1394 register ADDRESS	
1394DATA	9	1394 register DATA	
PHYCTL0	A	PHY control register0	
PHYCTL1	B	PHY control register1	
ERRSTS	C	Error status register	
OPTIONS	D	Some options for control	
CAGSTS	E	Interrupt of Command Agent	

1394INST (offset 0)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
AsyncTx	ConfigROMResp	MORBReq	CORBReq	NxtCORBReq	PreCORBReq	SPD1	SPD0

The 1394INST register is an instruction set for the firmware to send a specified IEEE 1394 transmit packet. There are 5 types of transmit packet supported by bit[7:2] of the 1394 instruction register:

AsyncTx: When a general Asynchronous Transmit packet is sent by the GL700FW, the firmware shall prepare for all necessary data in AsyncTx registers firstly and then set this bit and speed code in this register. Once AsynTx is set, the GL700FW will start to send the data in the format of asynchronous transmit packet.

ConfigROMResp: When receiving a read request for Config-ROM space (FFFFF0000400-FFFFF0000800), the GL700FW will set bit RxDis to disable the reception of next packet, set bit CSRSTS of register INTSTAT and issue an interrupt to the internal microprocessor. The µP shall prepare the data for the destination ID (first two bytes of 1st quadlet), the realative Tlabel value(bit 7 to 4 of third byte in 1st quadlet) and the addressed Config-ROM data (the 4th quadlets of AsyncTX register) firstly and then set this bit ConfigROMResp to send a read response for the

Config-ROM read request. Once the data for response is ready, the firmware shall clear bit RXDis to enable the reception of next packet.

MORBReq: When receiving a write request for data block (8 bytes) to management agent address, the GL700FW will set bitRxD to disable the reception of next packet at first, then set bit SBP2STS of register INTSTAT and bit MagHit of register SBPSTAT to issue an interrupt. When the firmware is award of the interrupt due to above condition, it needs to prepare the destination ID (first two bytes of 1st quadlet) and set bit MORBReq to send a 32-byte block read request packet to the address specified by the MORB pointer in fore write request.

CORBReq: When receiving a write request for data block (8 bytes) Command ORB_POINTER registers, the GL700FW will set bit RxDis to disable the reception of next packet at first, then set bit SBP2STS of register INTSTAT and bit CagHit of register SBPSTAT to issue an interrupt. When the firmware is aware of the interrupt due to above condition, it needs to set bit CORBReq to send a 32-byte block read request packet to the address specified by the CORB pointer in fore write request.

NxtCORBReq: When completing an access of one Command ORB, the GL700FW will set bit ADPstop in register SBPCTL and bit ADPSTS in register INTFlag to issue an interrupt. If NEXT_ORB field in CORB registers is not null, the firmware needs to set this bit NxtCORBReq to issue a 32-byte block read request packet for the next ORB. Once bit NxtCORBReg is set, the GL700FW will update the contents of register ORB_POINTER with the old NEXT_ORB field in the current command block ORB, and auto-generate a 32-byte block read request packet with the destination offset decided by the contents of CORB data payload.

PreCORBReq: When receiving write request for data quadlet to Command DOORBELL register, the GL700FW will set bit SBP2STS of register INTSTAT and bit CagHit of register SBPSTAT to issue an interrupt. Firstly the µP needs to check the Next_ORB field of current CORB. If it is null, the firmware needs to set this bit, PreCORBReq, to re-fetch a new address pointer. Once the bit is set, the GL700FW will auto-generate a new 32-bytes block read request packet with the destination offset decided by the NEXT_ORB field of what had been the last ORB (This data has been saved in the register ORB_POINTER). However, if Next_ORB field of current CORB is not null, it means the activation of the doorbell is redundant and the firmware needs not to do anything.

SPD[1:0]: Speed code for transmit packet, 00-100mps, 01- 200mbps, 10- 400mbps, 11- reserved.

1394CTL (offset 1)

R/U	*R/W/U*	*R/W*	*R/U*	*R/W*	*R/W*	*R/W*	*R/W/U*
IDVAL	RxDis	IDETIME	LinkOn	LPS	SplTrEn	RetryEn	SoftReset

This register performs setting for the GL700FW basic operations.

IDVAL: This bit is used to indicate whether the address in NODEID register is valid or not.

RxDis: This bit is used to disable the GL700FW to receive packets. When this bit is set to “1”, the GL700FW will reject all packets received and respond with “Ack_Busy”. The source ID of received packet header is normally required for the GL700FW to send a corresponding response packet. When the GL700FW finishes receiving an asynchronous packet, a Config_ROM read request packet or a management ORB request packet or command agent registers are hit, the hardware will set this bit spontaneously to prevent the data of received packet header from being updated by next receiving packet. The firmware shall clear the bit to enable the reception of another packet after current received data being processed.

IDETIME: This bit is used for timing set for IDE DMA timing, when set as”0”, the timing for DMARDJ signal is active low 100 ns, active high 60 ns, when “1”, the timing is active low 80ns, active high 40ns.

LinkOn: This bit represents the status of the input pin LINKON.

LPS: Sets the state of pin LPS.

SplTrEn: Enables the timer of ATF for split transaction. When SplTrEn is set to 1 and a split transaction is used, the GL700FW shall receive an Ack_Pending response firstly and can not transmit any packet until receiving a Complete response packet or the Split-Timeout occurs. When this bit is set to "0", the time-out function is disabled.

RetryEn: Enables retry function of pack transmission. When RetryEn is set to 1, the GL700FW will attempt to retry packet transmission automatically if receiving the response of Ack_Busy_X, Ack_Busy_A or Ack_Busy_B.

SoftReset: This bit is used for reset the registers those are not related to PHY interface.

INTMASK (offset 2)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
INT	CFRINT	SBP2INT	ERRINT	ADPINT	TXCINT	RXINT	BusReset

INTSTAT (offset 3)

R/W/C	*R/W/C*	*R/W/C*	*R/W/C*	*R/W/C*	*R/W/C*	*R/W/C*	*R/W/C*
INTSTS	CFRSTS	SBP2STS	ERRSTS	ADPSTS	TXCSTS	RXSTS	BusReset

This register is read to reflect the status of various interrupt due to internal 1394 Link Core. Writing a one to the individual bit will clear the bit automatically.

INTSTS: Responds the status of interrupt pin.

CFRSTS: When the GL700FW receives a read request for Config_ROM whose destination offset is ranged from FFFFF00400h to FFFFF00800h, this bit will be set to "1".

SBP2STS: When the received packet is related to SBP-2 protocol, this bit is set to "1". At the same time the bits in register SBPStatus are also properly set to report further information about SBP-2

protocol.

ERRSTS: This bit is set when any one of TxErr, RxErr, RetryTimOut, SplitTimOut bit in ERRSTAT register is set.

ADPSTS: This bit is set upon the completeness or error while an access of CORB by the ADP engine.

TXCSTS: This bit is set if a packet transmitted completely.

RXSTS: This bit is set if receiving a general asynchronous packet which is not a Config_ROM Read request or any packet related to SBP-2 protocol.

BusReset: This bit is set if a Bus Reset was detected by PHY.

A write one action will clear the related interrupt bit.

SBPCTL (offset 4)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W/U*	*R/W/U*	*R/W/U*
Max3	Max2	Max1	Max0	P_align	ADPreset	ADPstop	ADPgo

Max[3:0]: After the µP issues a CORBReq instruction, the GL700FW shall send a corresponding request packet and then expect a 32-byte response packet for Command ORB. Upon receiving this packet, both SBP2STS of register INTSTAT and CORBSTS of register SBPSTAT are set. When the µP receives the interrupt, the firmware needs to check the data payload of CORB register. If it is not a dummy ORB, the firmware has to calculate the maximum length to transfer for a packet (if the FIFO size of the GL700FW is 2K bytes, the value is Min(11, max_payload+2, page_size+8)).

ADPgo: Set ADPgo to activate the automatic data transfer data between the initiator and target, this bit will be reset when 1394 Bus-Reset happen, firmware need to set this bit after receive reconnect Management-ORB.

P_align: This bit is used in mode 1 (when p=0 and page_size<>0). The firmware shall set this bit to "1" if the memory space of initiator is page-aligned. In mode 2, the total transfer length in one page element shall not cross the page boundary, so the hardware needs not to consider the issue of page alignment. When this bit is “0”, the transfer size for 1st to last-1 packet is 2^(Max[3:0}). When this bit set to “1”, the transfer size for 1st packet is Min(xfer_size, 2^(Max[3:0])-offset_address(Max[3:0]-1:0)), and 2nd to last-1 packet is 2^(Max[3:0]). For both case, the size of the last packet is the residual byte count.

ADPreset: When GL700FW receives a write request for quadlet packet to AGENT_RESET register, or 1394 serial bus entering Bus Reset state, or firmware set this bit to “1”. And ADP state machine will enter idle state and set ADPreset bit to “1”, ADPgo =”0” and set ADPSTS bit of INTSTAT register to “1”. This is a abnormal ADP stop condition.

ADPstop: The ADP will stop when either it has normally completed the transaction of the packet that was loaded in the Command ORB or an error has occurred. Upon both cases, the GL700FW will set this bit to “1” and set ADPSTS bit of INTSTAT register to “1”. This is a Normal ADP

stop condition.

SBPSTAT (offset 5)

R/W/C	*R/W/C*	*R/W/C*	*R/W/C*	*R/W/C*	*R/W*	*R/W*	*R/W*
MagHit	CagHit	MORBSTS	CORBSTS	StatusWriteOK	CagSTS1	CagSTS0	CagVld

This register reflects various interrupt status about the SBP-2 protocol. Setting one to any bit of the register will also cause the setting of bit SBP2STS in the INTSTAT register.

MagHit: This bit is set when the GL700FW receives an 8-byte write request for data block packet whose destination address hits that of the Management agent. A write one action will clear the related interrupt bit.

CagHit: This bit is set when the GL700FW receives a packet whose destination address hits the Command agent. A write one action will clear the related interrupt bit.

MORBSTS: This bit is set when the GL700FW receives a MORB response packet. After the GL700FW transmits a Management ORB request packet, the initiator will transmit a 32-byte read response packet whose tLabel consists with that of the read request packet (the tLabel of Management ORB request for the GL700FW is fixed to "11"). A write one action will clear the related interrupt bit.

CORBSTS: This bit is set when the GL700FW receives a CORB response packet. After the GL700FW transmits a Command ORB request packet, the initiator will response a 32-bytes packet whose tLabel consists with that of the read request packet (the tLabel of the Command ORB request for the GL700FW is fixed to "12"). A write one action will clear the related interrupt bit.

StatusWriteOK: This bit is set when any of the bit StatusGood or StatusComplete of the MISC register is set. This bit is used for external µP tell internal µP that the status FIFO is already write complete and the internal µP can prepare the status FIFO packet for this command ORB. A write one action will clear the related interrupt bit.

CagST[1:0]: These two bits represent the two LSBs of the AGENT_STATE register for the Command agent. 00: RESET, 01:ACTIVE, 10:SUSPENDED, 11: DEAD.

CagVld: Command agent valid. When the GL700FW receives a Management request with the function LOGIN ORB, the firmware shall return a Login Response with a specified login_ID and address of the Command block agent. And set this bit to filter the packet that is hit the command agent. This bit will be reset automatically when 1394 Bus-Reset happen, Firmware need to set this bit if receive reconnect Management-ORB.

TXSTAT (offset 6)

R/O	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
TXSPD1	TXSPD0	AckValid	AckMiss	TXACK3	TXACK2	TXACK1	TXACK0

This register reflects the detailed status of an asynchronous transmitted packet when bit TXCSTS of register INTSTAT is set.

TXSPD[1:0] Report the speed of transmitted packet: 00 – 100Mb/s, 01 – 200Mb/s, 10 – 400 Mb/s, 11– reserved.

AckValid This bit is set when the GL700FW receives Acknowledge code from the destination node after completing a packet transmission.

AckMiss This bit is set if any error occurs during the reception of the Acknowledge code.

TXACK[3:0] Store received Acknowledge code.

RXSTAT (offset 7)

R/O	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*	*R/O*
RXSPD1	RXSPD0	AckValid	Reserved	RXACK3	RXACK2	RXACK1	RXACK0

This register reflects the detailed status of an asynchronous received packet when bit RXSTS, SBP2STS or CSRSTS of register INTSTAT is set.

RXSPD[1:0] Report the speed of received packet.

AckValid This bit is set when the GL700FW receives Acknowledge code from the destination node after completing a packet reception. This bit is auto cleared after read.

RXACK[3:0] Store returned Acknowledge code.

1394ADR (offset 8)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
A7	A6	A5	A4	A3	A2	A1	A0

1394DATA (offset 9)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
D7	D6	D5	D4	D3	D2	D1	D0

These two registers are used for the firmware to access the 1394-related data field. All the data field and index are listed in appendix. If the μP intends to access the data filed relative with the IEEE 1394 or SBP-2 protocol, it has to set the 1394ADR register at first, and then write data to the 1394DATA register will cause the data to be written to the data field specified by the 1394ADR register. A read to the 1394DATA register will always return the data indexed by the current contents of the register 1394ADR.

PHYCTL0 (offset A)

R/W/U	*R/W/U*	*R/W/C*	*R/O*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
RDREQ	WRREQ	RDDON	Reserve	ADDR3	ADDR2	ADDR1	ADDR0

PHYCTL1 (offset B)

R/W/U	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

The PHY control registers, PHYCTL0 and PHYCTL1, are used to access the registers of PHY controller via the standard PHY/Link interface. To read a register, the address of the register is written to ADDR[3:0] of the PHYCTL0 register along with a 1 to the RDREQ bit. When the read request has been sent to the PHY (through the Lreq pin), the RDREQ bit is cleared to 0. When the PHY returns the register data through a status transfer, the RDDON bit transitions to one, and the data will be stored in the PHYCTL1 register. The firmware has to poll the status of RDDON bit to ensure the most updated data returned.

To write to a PHY register, prepare the written data at the PHYCTL1 register, the address of the register ADDR[3:0] of the PHYCTL0 register, then a 1 to the WRREQ bit. The WRREQ bit is cleared when the write request has been transferred to the PHY.

The µP shall always check the foregoing register read or write has finished before issuing a new read or write request to the PHY registers.

ERRSTAT (offset C)

	R/U	*R/U*	*R/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
	ADPSTAT2	ADPSTAT1	ADPSTAT0	TxErr	RxErr	RetryTimeOut	SplitTimeOut

ADPSTAT[2:0]: Report the state of ADP state machine, for debugging and firmware development only.

TxErr: This bit is set if any error happens when transmitting packet.

RxErr: This bit is set if any error happens when receiving packet.

RetryTimeOut: This bit is set if Ack_busy* happens and the retry number exceeds the setting.

SplitTimeOut: This bit is set if time-out happens and there is still no read response packet received when the GL700FW has sent a read request packet and the split transaction is used.

OPTIONS (offset D)

R/W	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*	*R/W*
LinkSus	NotWaitOneIdle	AddOneIdle	CRCChkDis	ByteSwap	PHY_DTE	NotAck3Idle	AphyEnable

CAGSTS (offset E)

R/W	*R/W*	*R/W*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*	*R/W/U*
			UN_STS_EN	DOORBELL	ORB_PNT	CAG_RST	CAG_STS

CAG_STS: When a read request quadlet packet is hit to AGENT_STATE register, this bit will be set to "1", a write "0" to this bit will clear this bit.

CAG_RST: When a write request quadlet packet is hit to AGENT_RESET register, this bit will be set to "1", a write "0" to this bit will clear this bit.

ORB_PNT: When a write request block with 8 bytes length packet is hit to ORB_POINTER register, this bit will be set to "1", a write "0" to this bit will clear this bit.

DOORBELL: When a write request quadlet packet is hit to DOORBELL register, this bit will be set to "1", a write "0" to this bit will clear this bit.

UN_STS_EN: When a write request quadlet packet is hit to UNSOLICITED_STATUS_ENABLE register, this bit will be set to "1", a write "0" to this bit will clear this bit.