HD63487

Memory Interface and Video Attribute Controller (MIVAC)

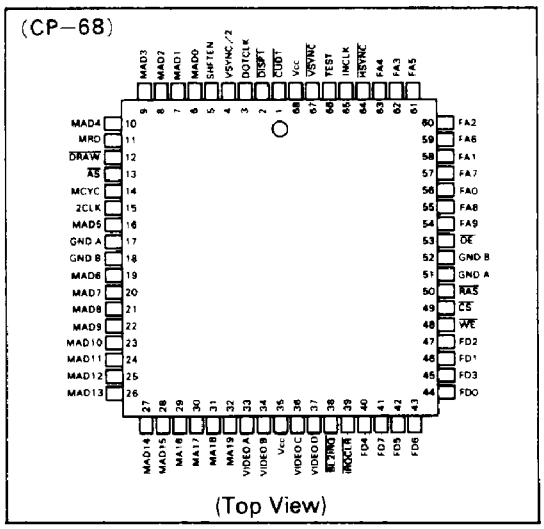
The MIVAC belongs to the HD63484 ACRTC (Advanced CRT Controller) family. It includes peripheral control circuits for graphic display on a chip. Incorporating bus driver circuits and a DRAM interface, the MIVAC allows direct connection to DRAMs with no external circuits. On-chip Parallel/Serial converting shift register generates high speed video signals. Adopting static column mode, fast memory access achieves high throughput in spite of narrow memory data bus. The MIVAC provides most functions required at peripherals of a frame buffer for graphic display constructed with 1 to 4 memory chips, and enables small size graphic system easily. Using the Hi-BiCMOS process, the MIVAC achieves high speed memory access with low power dissipation.

Features

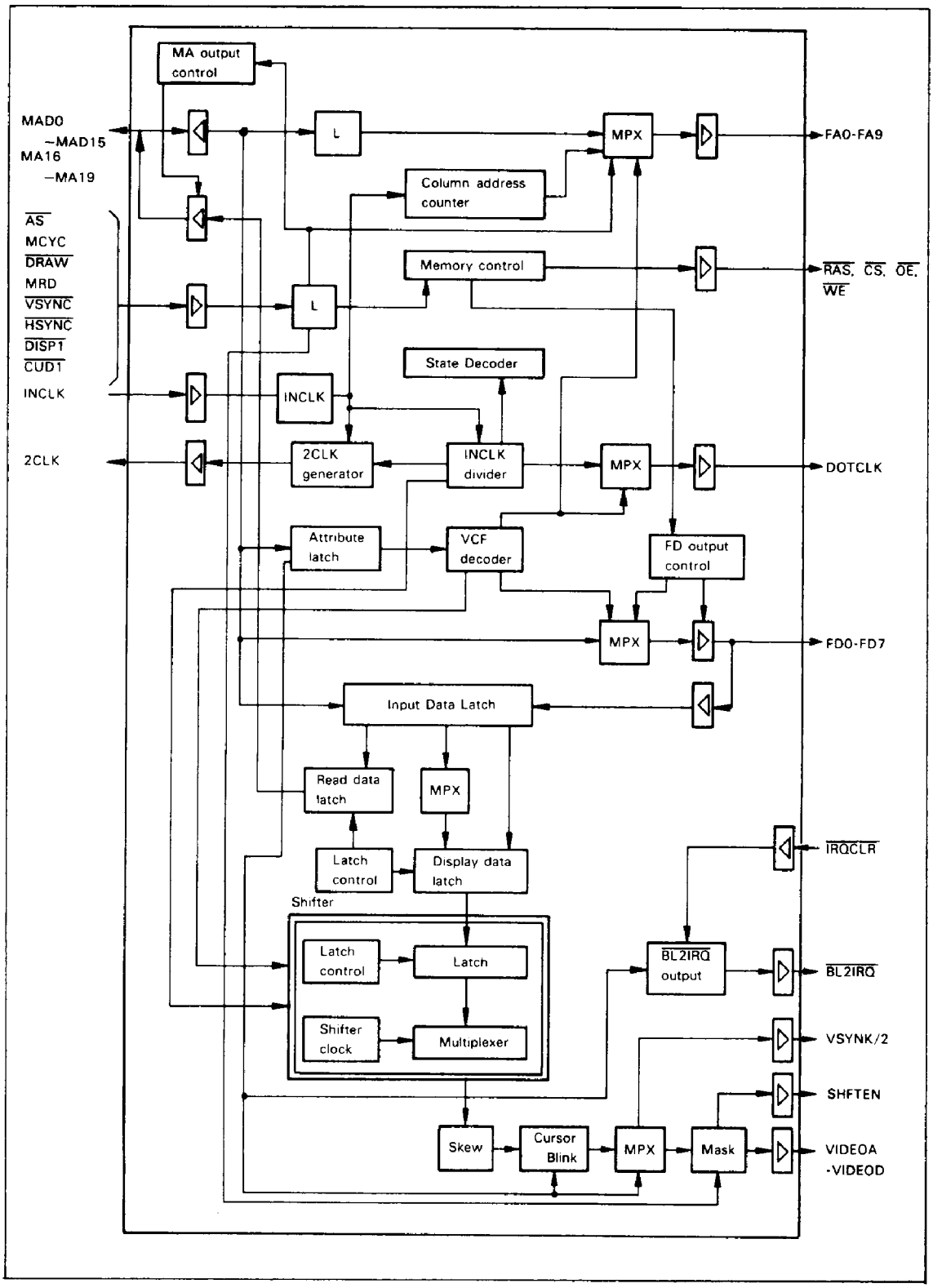
- Directly connected with 1 to 4 memory devices (x 4 bit organization, static column mode)
- Generates DRAM interface signals: row and column address, $\overline{RAS}$, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$ and memory data
- Generates high speed video signal: dot rate of 33MHz (max)
- 16 kinds of operation modes by the combination of;
  —2, 4 and 16 colors (1, 2 and 4 bit/pixel)
  —8, 16 and 32 dot shift
  —Single/Dual access
  —1, 2 and 4 chips memory
- Blinking block cursor display
- Memory variation: 256kx4 static column mode DRAM
- Generates special clock to drive the ACRTC (asymmetrical 2CLK)
- Input clock divider to generate dot clocks (divided by 1, 2 and 4)
- Supports frame sequential application
  —$\overline{VSYNC}$ divider and VSYNC/2 output
  —4 → 2 bit video output multiplexer
- BLINK2 interrupting control ($\overline{BL2IRQ}$ output)
- $\overline{CS}$ before $\overline{RAS}$ refresh
- Direct interface with the ACRTC
- Supports hardware window of ACRTC
- TTL compatible input/output
- Single +5V power supply
- Low power dissipation

2

Pin Assignment



Block Diagram

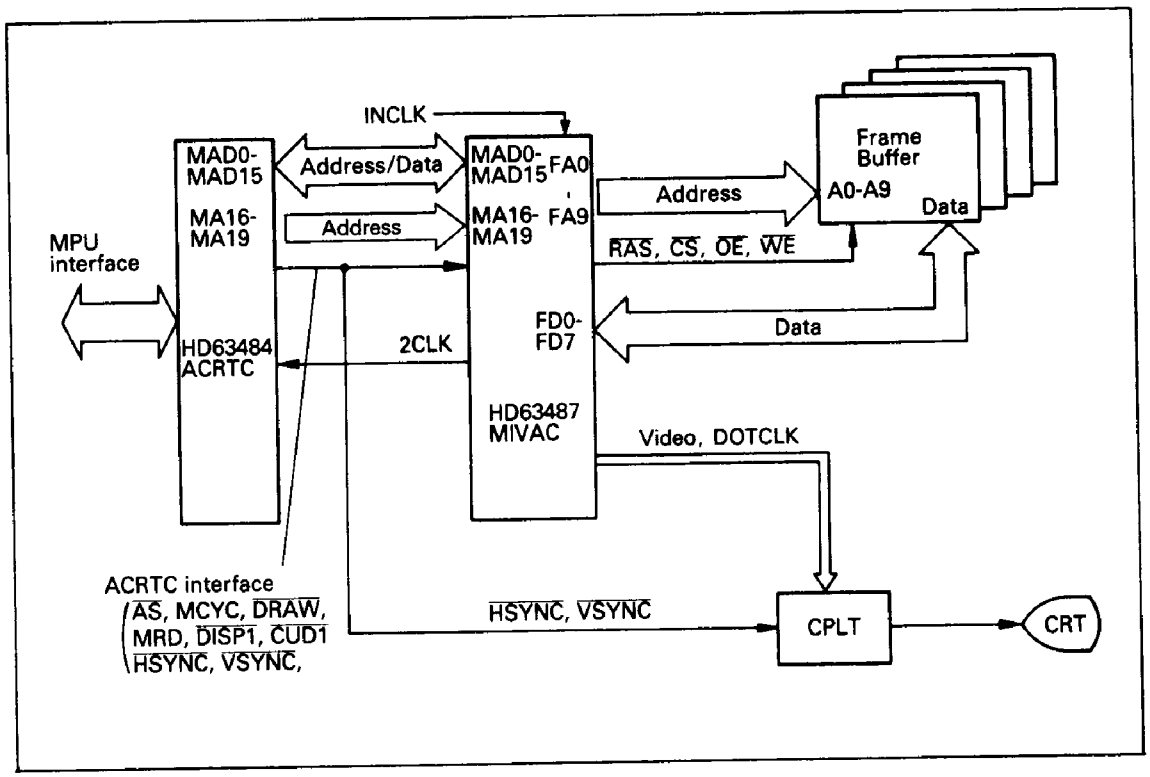


Function Table

Mode	Attribute code (ACRTC) MAD3	MAD2	MAD1	MAD0	MCYC Fetch	Access Mode	Memory Chip	Bit/ Pixel	Shifted Dot	DOTCK Division
0	0	0	0	0	1	Single	1	1	16	1
1	0	0	0	1	1	Single	1	2	8	2
2	0	0	1	0	1	Single	1	4	4	4
3	0	0	1	1	1	Single	2	2	16	1
4	0	1	0	0	1	Single	2	4	8	2
5	0	1	0	1	1	Single	4	4	16	1
6	0	1	1	0	1	Dual	1	1	16	2
7	0	1	1	1	1	Dual	1	2	8	4
8	1	0	0	0	1	Dual	2	1	32	1
9	1	0	0	1	1	Dual	2	2	16	2
A	1	0	1	0	1	Dual	2	4	8	4
B	1	0	1	1	1	Dual	4	2	32	1
C	1	1	0	0	1	Dual	4	4	16	2
D	1	1	0	1	2	Single	1	2	32	1
E	1	1	1	0	2	Single	1	4	16	2
F	1	1	1	1	2	Single	2	4	32	1

2

System Application Example



CRT Display Interface

Dot Clock (DOTCLK): The MIVAC internally divides INCLK by 1, 2 or 4 to generate the DOTCLK output. DOTCLK division ratio depends on VCF0-VCF3 of attribute code.

Video Outputs (VIDEOA-VIDEOD): VIDEOA-VIDEOD are the four bits output from the MIVAC's parallel-to-serial conversion shift register. They are supplied during a display period specified by the display signal ($\overline{DISP}$). Which outputs are usable depends on the attribute code (VCF0-VCF3).

Shift Enable (SHFTEN): SHFTEN is active high output. This output indicates the active display period of the screen.

Vertical Sync Divide-by-2 (VSYNC/2): VSYNC/2 output is $\overline{VSYNC}$ signal from the ACRTC divided by two.

Others

BLINK2 Interrupt ($\overline{BL2IRQ}$): This output is sat by BLINK2 (MA19) of the attribute code. $\overline{BL2IRQ}$ is low when BLINK2 is high.

BLINK2 Interrupt Clear ($\overline{IRQCLR}$): This input clears the $\overline{BL2IRQ}$ signal. When $\overline{IRQCLR}$ is low, $\overline{BL2IRQ}$ is clear and high.

2

Pin Description

Signal	Description	Pin No.
V_{CC}	Power	68
V_{CC}	Power	35
V_{SS}	Logic ground	52
V_{SS}	Logic ground	51
V_{SS}	Logic ground	18
V_{SS}	Logic ground	17
2CLK	Output clock to the ACRTC	15
$\overline{MCYC}$	Memory cycle input from the ACRTC	14
$\overline{DRAW}$	Draw input from the ACRTC	12
$\overline{MRD}$	Memory read input from the ACRTC	11
$\overline{AS}$	Address strobe input from the ACRTC	13
MAD0	Multiplex frame buffer address/data to/from ACRTC	6
MAD1	Multiplex frame buffer address/data to/from ACRTC	7
MAD2	Multiplex frame buffer address/data to/from ACRTC	8
MAD3	Multiplex frame buffer address/data to/from ACRTC	9
MAD4	Multiplex frame buffer address/data to/from ACRTC	10
MAD5	Multiplex frame buffer address/data to/from ACRTC	16
MAD6	Multiplex frame buffer address/data to/from ACRTC	19
MAD7	Multiplex frame buffer address/data to/from ACRTC	20
MAD8	Multiplex frame buffer address/data to/from ACRTC	21
MAD9	Multiplex frame buffer address/data to/from ACRTC	22
MAD10	Multiplex frame buffer address/data to/from ACRTC	23
MAD11	Multiplex frame buffer address/data to/from ACRTC	24
MAD12	Multiplex frame buffer address/data to/from ACRTC	25
MAD13	Multiplex frame buffer address/data to/from ACRTC	26
MAD14	Multiplex frame buffer address/data to/from ACRTC	27
MAD15	Multiplex frame buffer address/data to/from ACRTC	28
MA16	Memory address line 16 from the ACRTC	29
MA17	Memory address line 17 from the ACRTC	30
MA18	Memory address line 18 from the ACRTC	31
MA19	Memory address line 19 from the ACRTC	32

Pin Description (cont)

Signal	Description	Pin No.
$\overline{\text{HSYNC}}$	Holizontal sync input from the ACRTC	64
$\overline{\text{VSYNC}}$	Vertical sync input from the ACRTC	67
VSYNC/2	Vertical sync divide-by-2 output	4
$\overline{\text{CUD1}}$	Cursor control input from the ACRTC	1
$\overline{\text{DISP1}}$	Display input from the ACRTC	2
$\overline{\text{RAS}}$	Row address strobe output to DRAM	50
$\overline{\text{CS}}$	Chip select output to DRAM	49
$\overline{\text{WE}}$	Write enable output to DRAM	48
$\overline{\text{OE}}$	Output enable output to DRAM	53
FA0	Frame buffer (memory) address output 0	56
FA1	Frame buffer (memory) address output 1	58
FA2	Frame buffer (memory) address output 2	60
FA3	Frame buffer (memory) address output 3	62
FA4	Frame buffer (memory) address output 4	63
FA5	Frame buffer (memory) address output 5	61
FA6	Frame buffer (memory) address output 6	59
FA7	Frame buffer (memory) address output 7	57
FA8	Frame buffer (memory) address output 8	55
FA9	Frame buffer (memory) address output 9	54
FD0	Frame buffer data input/output line 0	44
FD1	Frame buffer data input/output line 1	46
FD2	Frame buffer data input/output line 2	47
FD3	Frame buffer data input/output line 3	45
FD4	Frame buffer data input/output line 4	40
FD5	Frame buffer data input/output line 5	42
FD6	Frame buffer data input/output line 6	43
FD7	Frame buffer data input/output line 7	41
INCLK	Main timing clock input	65
DOTCLK	DOT clock output to video circuit	3
VIDEOA	Video A output	33
VIDEOB	Video B output	34
VIDEOC	Video C output	36
VIDEOD	Video D output	37
TEST	Test pin input	66
SHFTEN	Shift enable output	5
$\overline{\text{BL2IRQ}}$	BLINK2 interrupt output	38
$\overline{\text{IRQCLR}}$	BLINK2 interrupt clear input	39

Operation

Basic operating clock

Output signals from MIVAC define INCLK which inputs to MIVAC as a basic operating clock, and input signals to MIVAC define 2CLK which is output from MIVAC as well. 2CLK, the basic operating clock of ACRTC which is output from MIVAC, is generated from INCLK. In order to save the memory access time, 2CLK is configurated unsymmetrically between the first half and the latter half of cycle times as shown below.

Frame buffer control

MIVAC uses the DRAM of the static column mode as a memory for the frame buffer, and reduces the number of memory used for the frame buffer by accessing the memory several times per memory cycles. Using one, two, and four DRAMs respectively, MIVAC can deal with various kinds of applications. Figure 2 shows the connection of MIVAC to the DRAM.

To control these DRAMs, MIVAC generates $\overline{RAS}$, $\overline{CS}$, $\overline{OE}$ and $\overline{WE}$. And it outputs the row and the column address as the ones for DRAM, adapting to the timing of $\overline{RAS}$ and $\overline{CS}$.

The Drawing Read cycle is shown in figure 3, the Drawing Write cycle in figure 4, the Display Read cycle in figure 5 and 6, and $\overline{CS}$ before $\overline{RAS}$ Refresh cycle in figure 7 respectively.

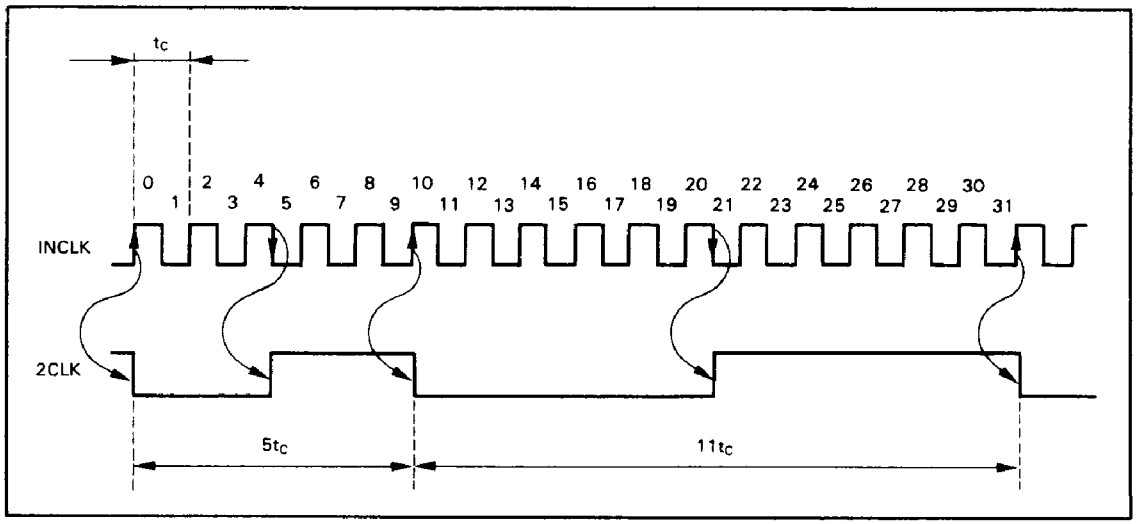


Figure 1. 2CLK Output Timing

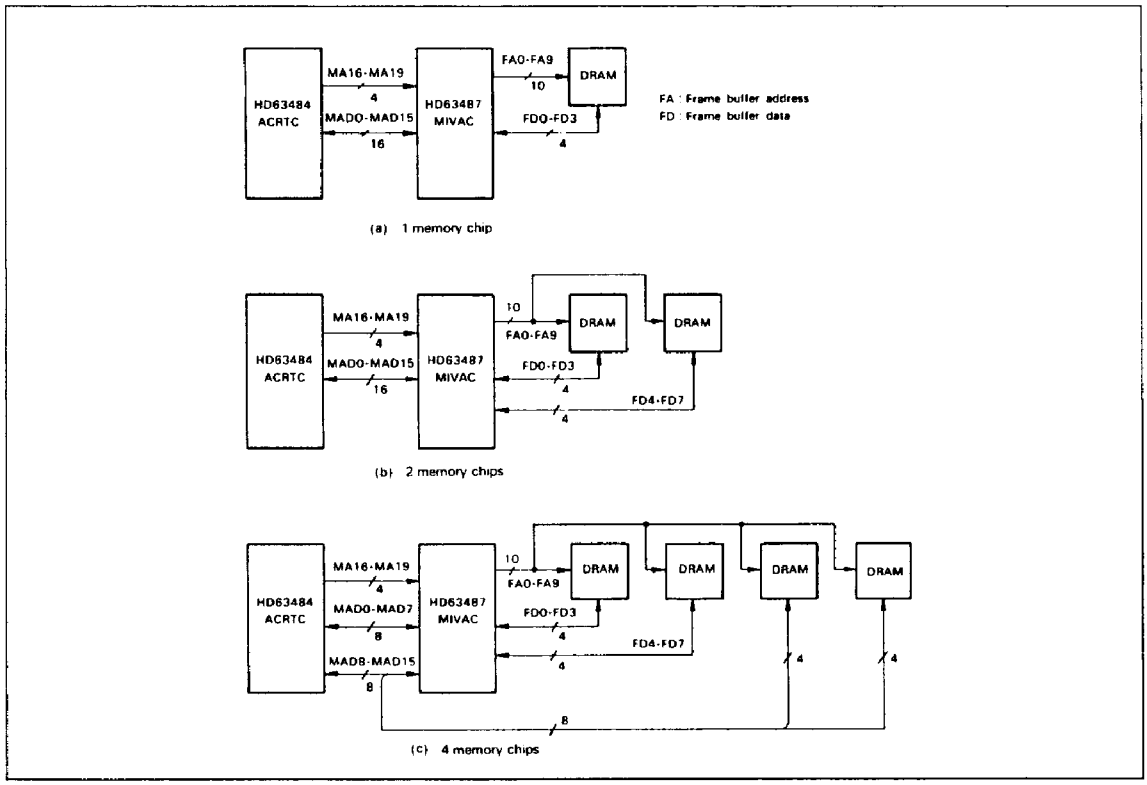


Figure 2. Frame Buffer Connections

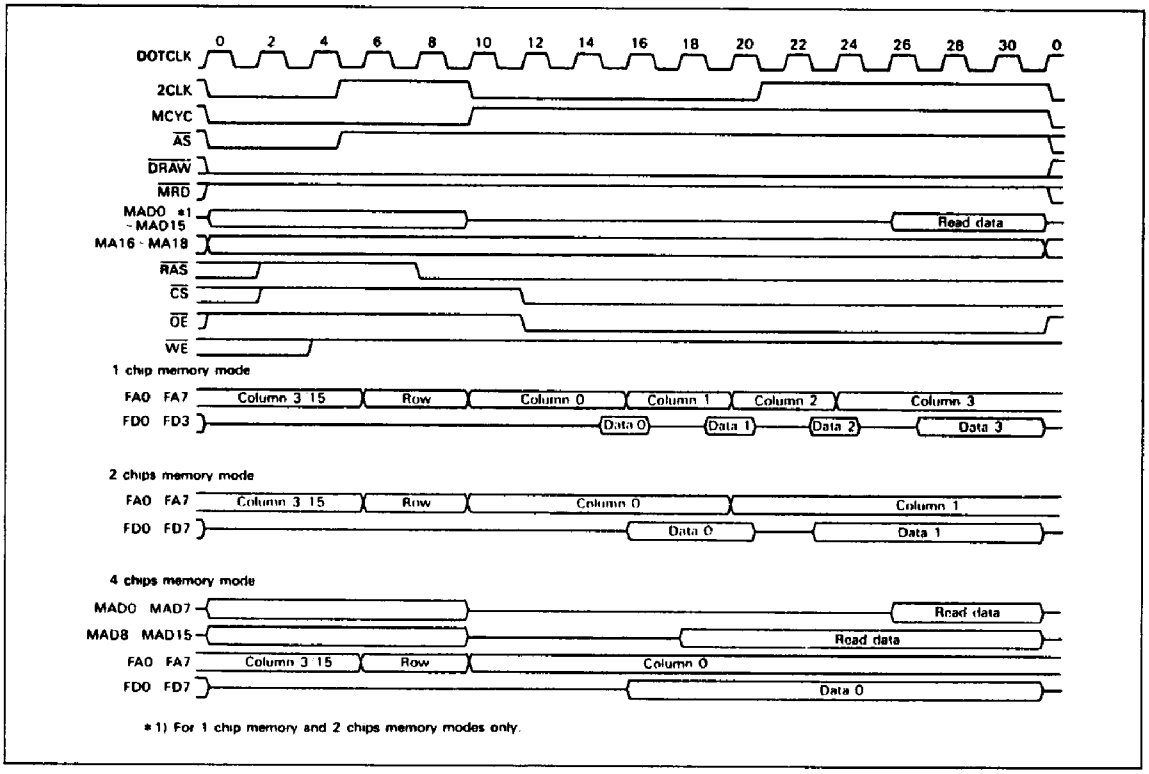


Figure 3. 1MCYC Drawing Read Cycle

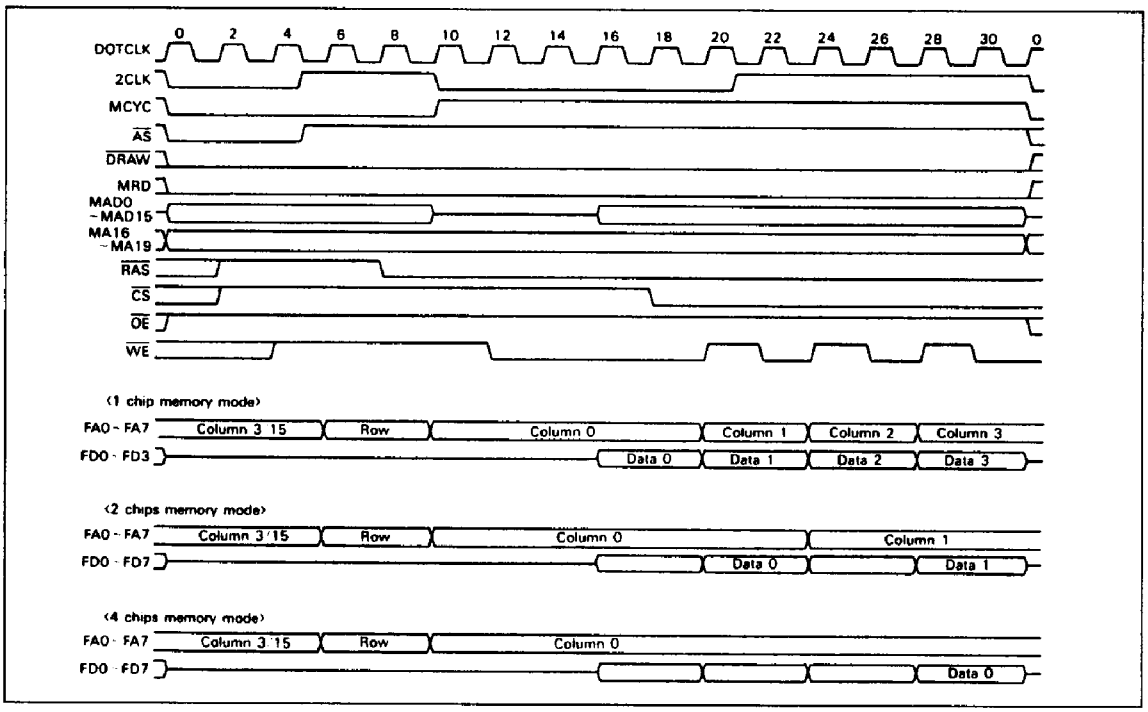


Figure 4. 1MCYC Drawing Write Cycle

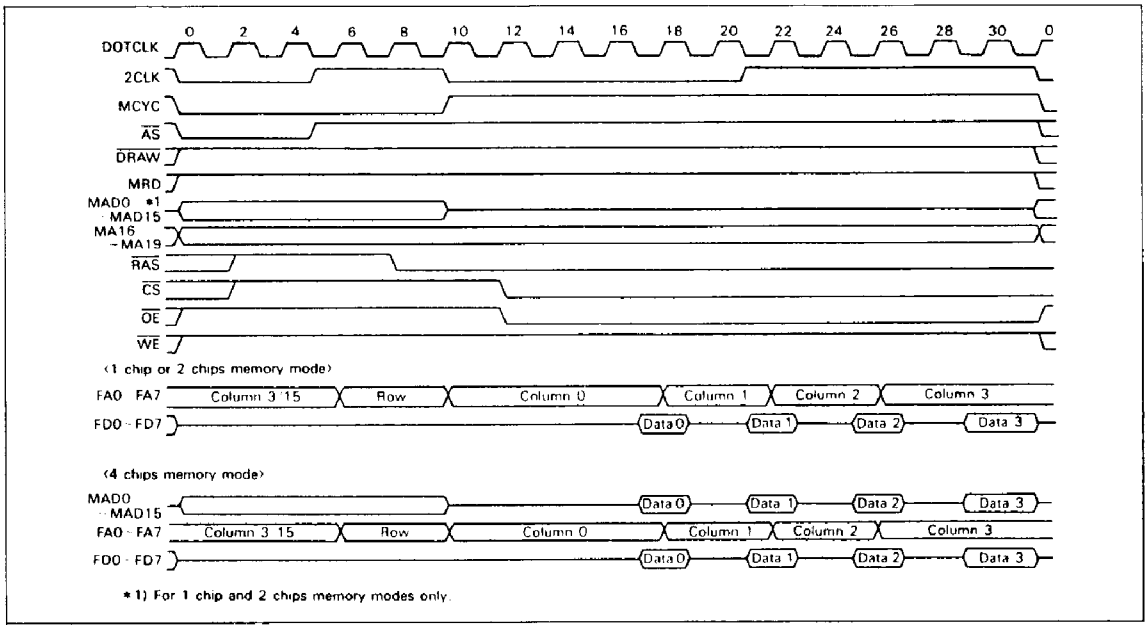


Figure 5. 1MCYC Display Read Cycle

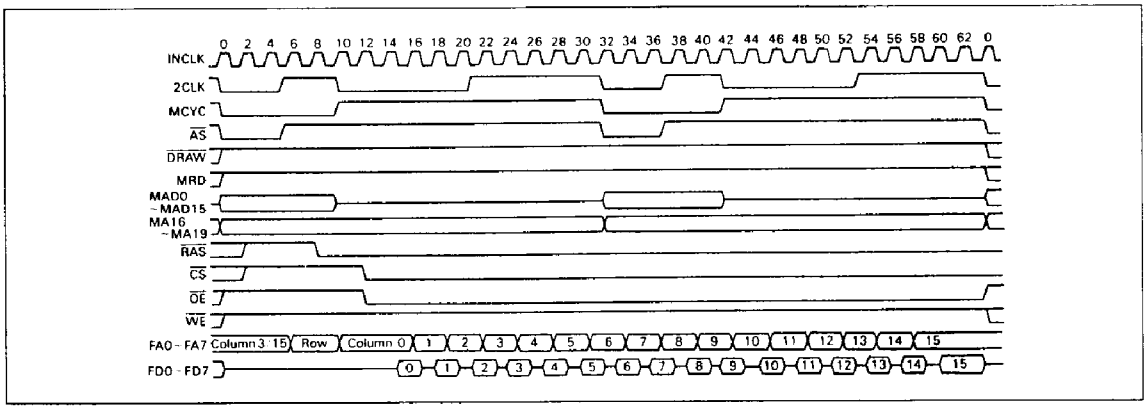


Figure 6. 2MCYC Display Read Cycle

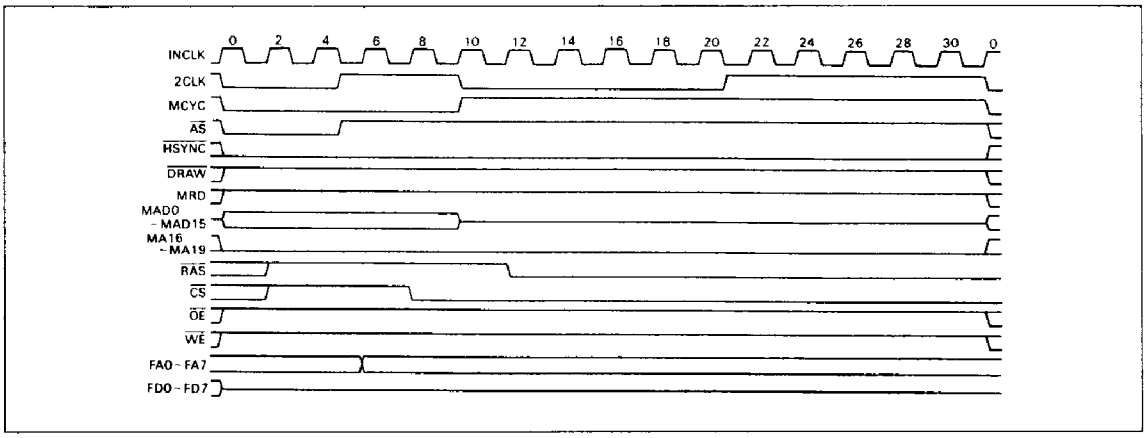


Figure 7. CS Before RAS Refresh Cycle

Data Transfer

The MIVAC contain control circuits for bidirectional transfer between the ACRTC and frame buffers. To transfer data, the MIVAC receive the ACRTC's memory cycle (MCYC), memory read (MRD), draw ($\overline{DRAW}$) and address strobe ($\overline{AS}$) signals.

The MIVAC recognize a nondisplay cycle when $\overline{DRAW}$ is low. In nondisplay cycles the data transfer direction is determined by the memory read signal (MRD). MRD high signifies a read cycle to transfer data from frame buffers to the ACRTC. MRD low signifies a write cycle to transfer data from the ACRTC to the frame buffers. Timing for the data transfer is determined by the MCYC input. When MCYC is high, frame buffers or the ACRTC three-state output buffers are enabled for transfer.

Drawing Write Cycle: The MIVAC recognize a drawing write cycle when both $\overline{DRAW}$ and MRD are low.

Drawing Read Cycle: The MIVAC recognize a drawing read cycle when $\overline{DRAW}$ is low and MRD is high.

When MCYC is high during this cycle, the MIVAC enable the data buffer (MAD0-MAD15) for the ACRTC and output a word from the frame buffers.

Video signal generation

MIVAC converts the parallel display data, which is output from the frame buffer, to serial in the internal shift register, and outputs the display data from VIDEOA-VIDEOD pins after making it simultaneous with DOTCLK. As the pins for VIDEOA-VIDEOD are determined by the graphic bit mode, they must be connected to CRT carefully. Table 1 shows the relation between the mode and the used pins.

Figure 8 shows the relation between the memory access and the video output.

Table 1. Operation Mode and Video Outputs

Mode	Graphic bit mode (bit/pixel)	Display colors (or Gray scale)	VIDEOA	VIDEOB	VIDEOC	VIDEOD
0	1	Monochrome (2)	○	×	×	×
1	2	4 (4)	○	○	×	×
2	4	16 (16)	○	○	○	○
3	2	4 (4)	○	○	×	×
4	4	16 (16)	○	○	○	○
5	4	16 (16)	○	○	○	○
6	1	Monochrome (2)	○	×	×	×
7	2	4(4)	○	○	×	×
8	1	Monochrome (2)	○	×	×	×
9	2	4 (4)	○	○	×	×
A	4	16 (16)	○	○	○	○
B	2	4 (4)	○	○	×	×
C	4	16 (16)	○	○	○	○
D	2	4 (4)	○	○	×	×
E	4	16 (16)	○	○	○	○
F	4	16 (16)	○	○	○	○

○ : Available
× : Not available

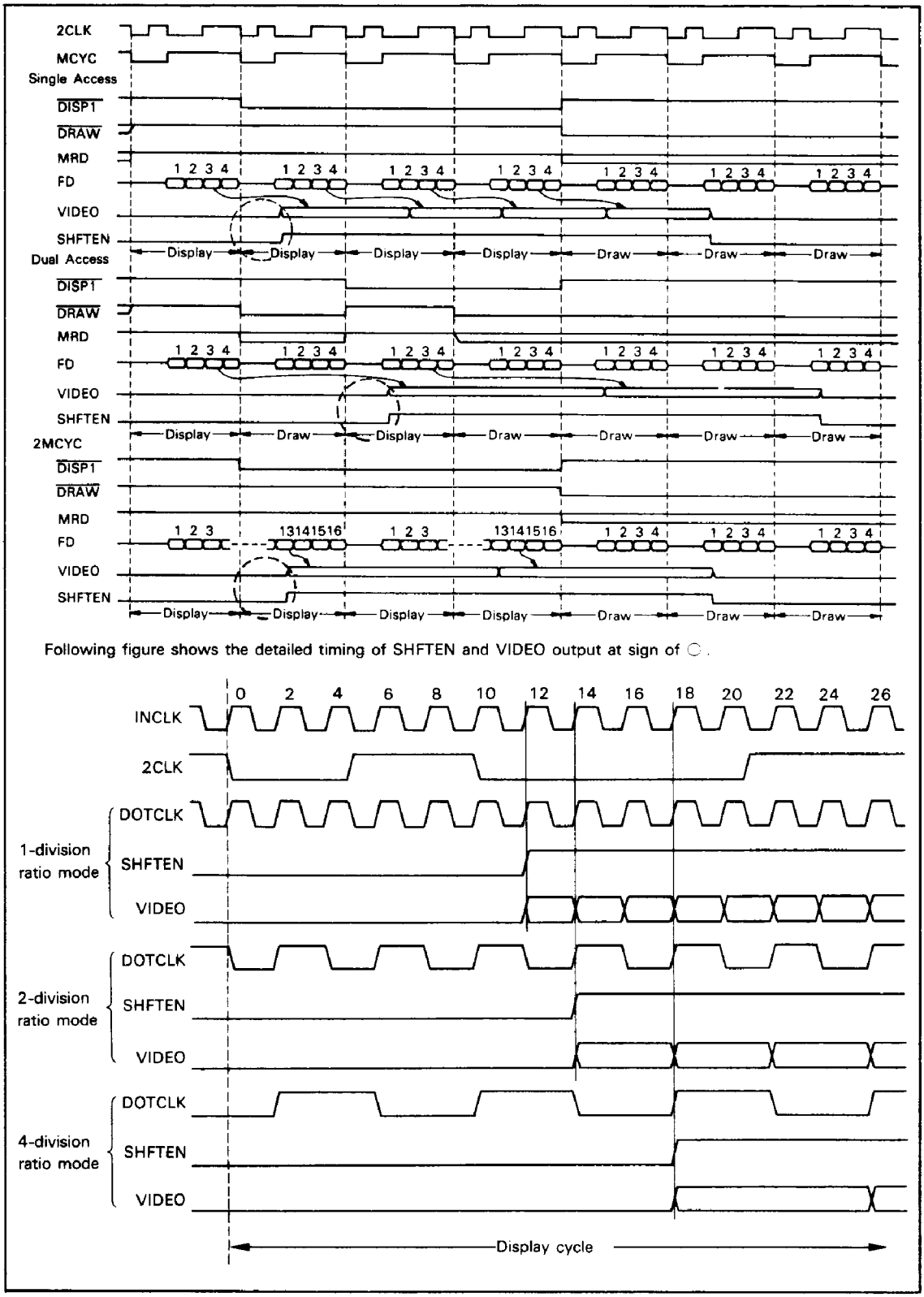


Figure 8. Display Timing (Single Access, Dual Access, 2MCYC)

Attribute Control Codes

The MIVAC sets colors, the number of shift bits, and access mode when it receives attribute codes and blink information from the ACRTC. The ACRTC outputs 20 bits of attribute control codes (MAD0 to MAD15, MA16 and MA19) during the attribute control code output cycle (figure 9). This information includes user-definable codes and blink control codes (figure 10).

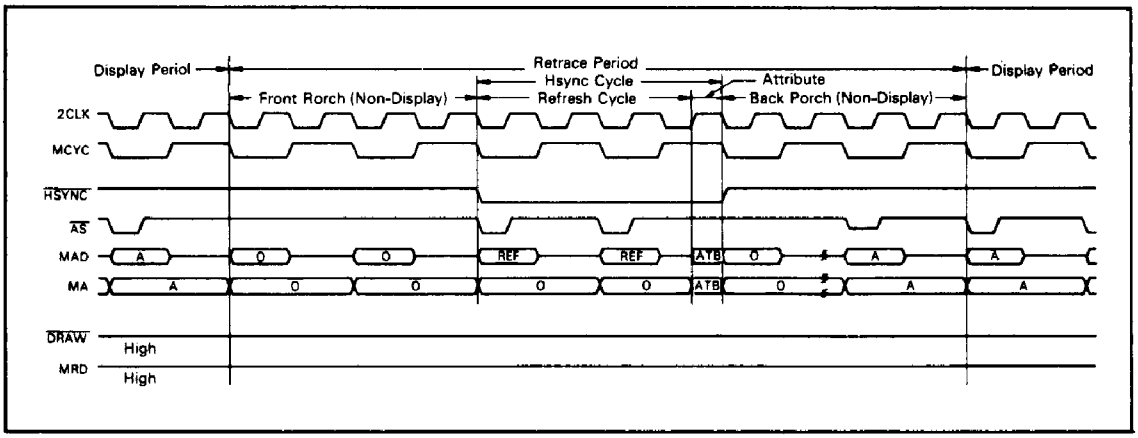


Figure 9. DRAM Refresh and Attribute Code Output Timing (Single Access Mode)

Signal	Attribute Control Codes	
MA19	BLINK2	BL2IRQ output
MA18	BLINK1	Graphic cursor cursor blinking
MA17	SPL2	
MA16	SPL1	
MAD15	HZ3	
⟨	⟨	
MAD12	HZ0	MIVAC does not use
MAD11	HSD3	
⟨	⟨	
MAD8	HSD0	
MAD7	MUXEN	Video multiplex output enable
MAD6	VMD	Frame buffer depth
MAD5	CUR1	Color of graphic cursor
MAD4	CUR0	
MAD3	VCF3	MIVAC operating modes
MAD2	VCF2	
MAD1	VCF1	Attribute Control Codes
MAD0	VCF0	

Figure 10. Attribute Control Codes

VCF0—VCF3 (MAD0—MAD3)

VCF0 to VCF3 (MAD0 to MAD3) define sixteen basic operating modes as shown in the tables 2 and 3.

Table 2. Operating Modes

Mode	ACRTC Attribute Code Setting VCF3	VCF2	VCF1	VCF0	Screen Configuration (Dots × Rasters)	Frame Buffer (Bytes)	ACRTC Operating Frequency (MHz)	Memory Access	Access Mode	Memory Chips	Color Gradation	Shift (Bits)	DOTCLK Division Ratio	DOTCLK Maximum Frequency (MHz)
0	0	0	0	0	640×200, 350, 400, 480	512k/128k	4.13	480 ns/ 4 times	Single access mode	1	B&W	16	1	33
1	0	0	0	1	640×200, 480×240, 320×200, 240						4	8	2	16.5
2	0	0	1	0	320×200, 240 256×192						16	4	4	8.25
3	0	0	1	1	640×200, 350, 400, 480	1M/256k				2	4	16	1	33
4	0	1	0	0	640×200, 480×240, 320×200, 240						16	8	2	16.5
5	0	1	0	1	640×200, 350, 400, 480	2M/512k				4		16	1	33
6	0	1	1	0	640×200, 480×240, 320×200, 240	512k/128k			Dual access mode 0	1	B&W		2	16.5
7	0	1	1	1	320×200, 240 256×192						4	8	4	8.25
8	1	0	0	0	640×200, 350, 400, 480	1M/256k				2	B&W	32	1	33
9	1	0	0	1	640×200, 480×240, 320×200, 240						4	16	2	16.5
A	1	0	1	0	320×200, 240 256×192						16	8	4	8.25
B	1	0	1	1	640×200, 350, 400, 480	2M/512k				4	4	32	1	33
C	1	1	0	0	640×200, 480×240, 320×200, 240						16	16	2	16.5
D	1	1	0	1	640×200, 350, 400, 480	512k/128k		960 ns/ 16 times	Single access mode	1	4	32	1	33
E	1	1	1	0	640×200, 480×240, 320×200, 240						16	16	2	16.5
F	1	1	1	1	640×200, 350, 400, 480	1M/256k				2		32	1	33

Table 3. Dot Clock Frequency Range

Mode	Frequency
0, 3, 5, 8, B, D, F	33—11 MHz
1, 4, 6, 9, C, E	16.5—5.5 MHz
2, 7, A	8.25—2.75 MHz

MCYC Fetch: The MCYC fetch defines the number of cycles.

1: One, two, or four memories
2: One or two memories

Access Mode: The MIVAC supports single- and dual-access 0 modes.

1: Single access/dual access 0
2: Single access

Memory Chips: The MIVAC can connect one, two, or four memory chips.

1 chip : connect FD0 to FD3 to data bus
2 chips: connect FD0 to FD8 to data bus
3 chips: connect FD0 to FD7 to low-order 8 bits, and MAD8 to MAD15 to high-order 8 bits of data bus.

Bit/Pixel: The MIVAC can display:

- 1 bit/pixel (B&W)
- 2 bits/pixel (4 colors)
- 4 bits/pixel (16 colors)

Dot Shift: The MIVAC can shift by 4, 8, 16, or 32 dots.

DOTCLK Division: The MIVAC can divide the INCLK frequency by 1, 2, or 4 depending on the number of shifted dots and access modes.

CUR0 and CUR1 (MAD4 and MAD5)

CUR0 and CUR1 set the cursor color (table 4).

VMD0 (MAD6)

VMD0 selects memory chips (table 5).

MUXEN (MAD7)

MUXEN selects the multiplex video output. Multiplexing is defined by MUXEN and VSYNC/2 (table 6). VSYNC/2 is obtained by dividing $\overline{\text{VSYNC}}$ from the ACRTC by 2.

Note: VIDEOD is not multiplexed.

BLINK1 (MA18)

BLINK1 defines the blinking of cursor (table 7).

BLINK2 (MA19)

BLINK2 controls $\overline{\text{BL2IRQ}}$ output. When BLINK2 is 1, $\overline{\text{BL2IRQ}}$ is asserted (low).

Table 4. Cursor Color

CUR1	CUR0	Cursor Color
0	0	Black (VIDEOA to VIDEOD — 0)
0	1	White (VIDEOA to VIDEOD — 1)
1	0	Color specified by each bit (VIDEOA to VIDEOD) is inverted
1	1	Color specified by each bit (VIDEOA to VIDEOC) is inverted. (VIDEOD is not changed.)

Table 5. Memory Chips

VMD	Memory chips
0	256k words × 4 bit DRAM
1	1M words × 4 bit DRAMs

Table 6. Video Multiplex

MUXEN	VSYNC/2	VIDEOA	VIDEOB
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

Table 7. Cursor Blink

BLINK1	Cursor
0	No blinking
1	Blinking

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC} (Note)	−0.3 to +7.0	V
Input Voltage	V_{in} (Note)	−0.3 to V_{CC}+0.3	V
Output Voltage	V_{out} (Note)	5.5	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

Note: This value is in reference to V_{SS} = 0 V.

2

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} (Note)	4.75	5.00	5.25	V
Input "Low" Level Voltage	V_{IL} (Note)	0	—	0.7	V
Input "High" Level Voltage	V_{IH} (Note)	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Note: This value is in reference to V_{SS} = 0 V.

Electrical Characteristics
DC Characteristics
(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

Item		Symbol	Min	Max	Unit	Test Condition
Input "High" Level Voltage	All Inputs	V_{IH}	2.2	V_{CC}	V	
Input "Low" Level Voltage	All Inputs	V_{IL}	−0.3	0.7	V	
Input Clamp Voltage	All Inputs	V_I	—	−1.5	V	V_{CC} = 4.75 V I_{IN} = −18 mA
Output "High" Level Voltage	All Outputs	V_{OH}	2.7	—	V	V_{CC} = 4.75 V I_{OH} = −400 μA
Output "Low" Level Voltage	All Outputs	V_{OL}	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA
"High" Level Input Current	All Inputs	I_{IH}	—	20	μA	V_{CC} = 5.25 V V_I = 2.7 V
"Low" Level Input Current	All Inputs	I_{IL}	—	−400	μA	V_{CC} = 5.25 V V_I = 0.4 V
Short Circuit Output Current	All Outputs	I_{OS}	−40	−120	mA	V_{CC} = 5.25 V
Supply Current		I_{CC}	—	120	mA	V_{CC} = 5.25 V

AC Characteristics

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

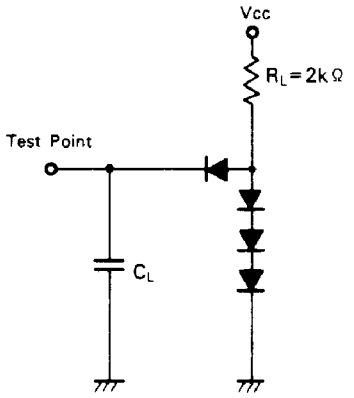
No.	Item	Symbol	Reference Figure#	Min	Max	Unit
1	INCLK Cycle Time	t_C	11	30	—	ns
2	INCLK High Level Pulse Width	t_{HW}	11	12	—	ns
3	INCLK Low Level Pulse Width	t_{LW}	11	12	—	ns
4	INCLK Rise Time	t_R	11	—	5	ns
5	INCLK Fall Time	t_F	11	—	5	ns
6	2CLK Delay Time	t_{2CLKD}	11	—	15	ns
7	MCYC Setup Time	t_{MCYCS}	11	10	—	ns
8	MCYC Hold Time	t_{MCYCH}	11	0	—	ns
9	$\overline{\text{HSYNC}}$ Setup Time	t_{HSS}	11	15	—	ns
10	$\overline{\text{HSYNC}}$ Hold Time	t_{HSH}	11	0	—	ns
11	$\overline{\text{DISP1}}$ Setup Time	t_{DISPS}	11	20	—	ns
12	MRD Setup Time	t_{MRDS}	11	15	—	ns
13	MRD hold Time	t_{MRDH}	11	5	—	ns
14	$\overline{\text{DRAW}}$ Setup Time	t_{DRAWS}	11	15	—	ns
15	$\overline{\text{DRAW}}$ Hold Time	t_{DRAWH}	11	5	—	ns
16	$\overline{\text{AS}}$ Setup Time	t_{ASS}	11	20	—	ns
17	$\overline{\text{AS}}$ Pulse Width	t_{ASW}	11	25	—	ns
18	Memory Address Setup Time	t_{AS}	11	25	—	ns
19	Memory Address Hold Time	t_{AH}	11	0	—	ns
20	$\overline{\text{CUD1}}$ Setup Time	t_{CUDS}	11	5	—	ns
21	$\overline{\text{VSYNC}}$ Setup Time	t_{VSS}[1]	17	5	—	ns
22	Attribute Code Delay Time	t_{ACS}	20	—	100	ns
23	Attribute Code Hold Time	t_{ASH}	20	5	—	ns
24	$\overline{\text{RAS}}$ Delay Time	t_{RSD}	11	—	15	ns
25	$\overline{\text{RAS}}$ Precharge Time	t_{RSP}	11	3tc-10	—	ns
26	$\overline{\text{CS}}$ Delay Time 1	t_{CSDL}	11	—	15	ns
27	$\overline{\text{OE}}$ Delay Time 1	t_{OED1}	11	—	15	ns
28	2CLK Delay Time from $\overline{\text{OE}}$	t_{2CKD}	11	0	10	ns
29	Valid MAD0-MA19 to Valid Low Address Delay Time	t_{RAD}	11	—	25	ns
30	Column Address Delay Time	t_{CAD}	11	5	25	ns
31	FD Setup Time	t_{FDS}	11	8	—	ns
32	FD Hold Time 1	t_{FDH1}	11	5	—	ns
33	FD Hold Time 2	t_{FDH2}	11	2	—	ns
34	Valid FD to Valid MAD Delay	t_{MADV}	11	—	10	ns
35	Read Data Turn on Time	t_{RDTV}	11	0	—	ns
36	Read Data Hold Time	t_{RDH}	11	3	—	ns

AC Characteristics (cont)

(V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

No.	Item	Symbol	Reference Figure#	Min	Max	Unit
37	$\overline{WE}$ Delay Time	t_{WED}	14	—	25	ns
38	$\overline{WE}$ Low Pulse Width	t_{WLW}	14	tc-15	—	ns
39	$\overline{WE}$ High Pulse Width	t_{WHW}	14	tc-15	—	ns
40	$\overline{CE}$ low to $\overline{WE}$ Pulse Width	t_{CWEW}	14	tc-15	—	ns
41	Draw Write Data Setup Time	t_{WDS}	14	15	—	ns
42	FD Delay Time 1	t_{FDD1}	14	—	20	ns
43	FD Delay Time 2	t_{FDD2}	14	—	20	ns
44	$\overline{WE}$/$\overline{CS}$ Low to FD Hold Time	t_{WFDHW}	14	tc-10	—	ns
45	$\overline{WE}$/$\overline{CS}$ Low to Address Hold	t_{WAHW}	14	tc-5	—	ns
46	FD Hold Time	t_{FDHW}	14	0	—	ns
47	FD Turn Off Time	t_{FDTI}	14	—	50	ns
48	VSYNC/2 Delay Time	t_{VS2D}	11	—	25	ns
49	DOTCLK Delay Time	t_{DCD}	11	—	15	ns
50	VIDEO Delay Time	t_{VD}	11	−5	5	ns
51	$\overline{BL2IRQ}$ Delay Time	t_{IRQD}	20	—	10	ns
52	$\overline{IRQCLR}$ to$\overline{BL2IRQ}$ Clear Delay Time	t_{IRQCD}	20	—	20	ns
53	SHFTEN Delay Time	t_{SFTEND}	11	−5	5	ns

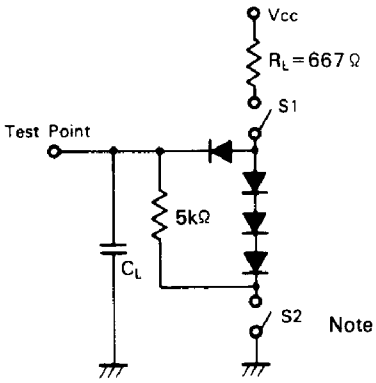
Test Circuit



Note: All diodes are 1S2074Ⓗ's or the equivalent.

Signal	C_L (pF)
2CLK	
DOTCK	
VSYNC/2	
$\overline{RAS}$	
$\overline{CS}$	
$\overline{WE}$	40
$\overline{OE}$	
FA0-FA9	
VIDEOA-VIDEOD	
SHFTEN	
$\overline{BL2IRQ}$	

(a) Totem Pole Output



Note: All diodes are 1S2074Ⓗ's or the equivalent.

Signal	C_L (pF)
MAD0-MAD15	40
FD0-FD7	

(b) Three State Output

Reference

Display Data Fetch	Memory Chip	Cycle Mode	Figure No.
4 Fetch/1 MCYC	1 Chip	Drawing Read Cycle	11
		Drawing Write Cycle	14
		Display Cycle	17
		Refresh & Attribute Cycle	20
	2 Chips	Drawing Read Cycle	12
		Drawing Write Cycle	15
		Display Cycle	17
		Refresh & Attribute Cycle	20
	4 Chips	Drawing Read Cycle	13
		Drawing Write Cycle	16
		Display Cycle	18
		Refresh & Attribute Cycle	20
16 Fetch/2 MCYC	1 Chips	Drawing Read Cycle	11
		Drawing Write Cycle	14
		Display Cycle	19
		Refresh & Attribute Cycle	20
	2 Chips	Drawing Read Cycle	12
		Drawing Write Cycle	15
		Display Cycle	19
		Refresh & Attribute Cycle	20

Timing Chart

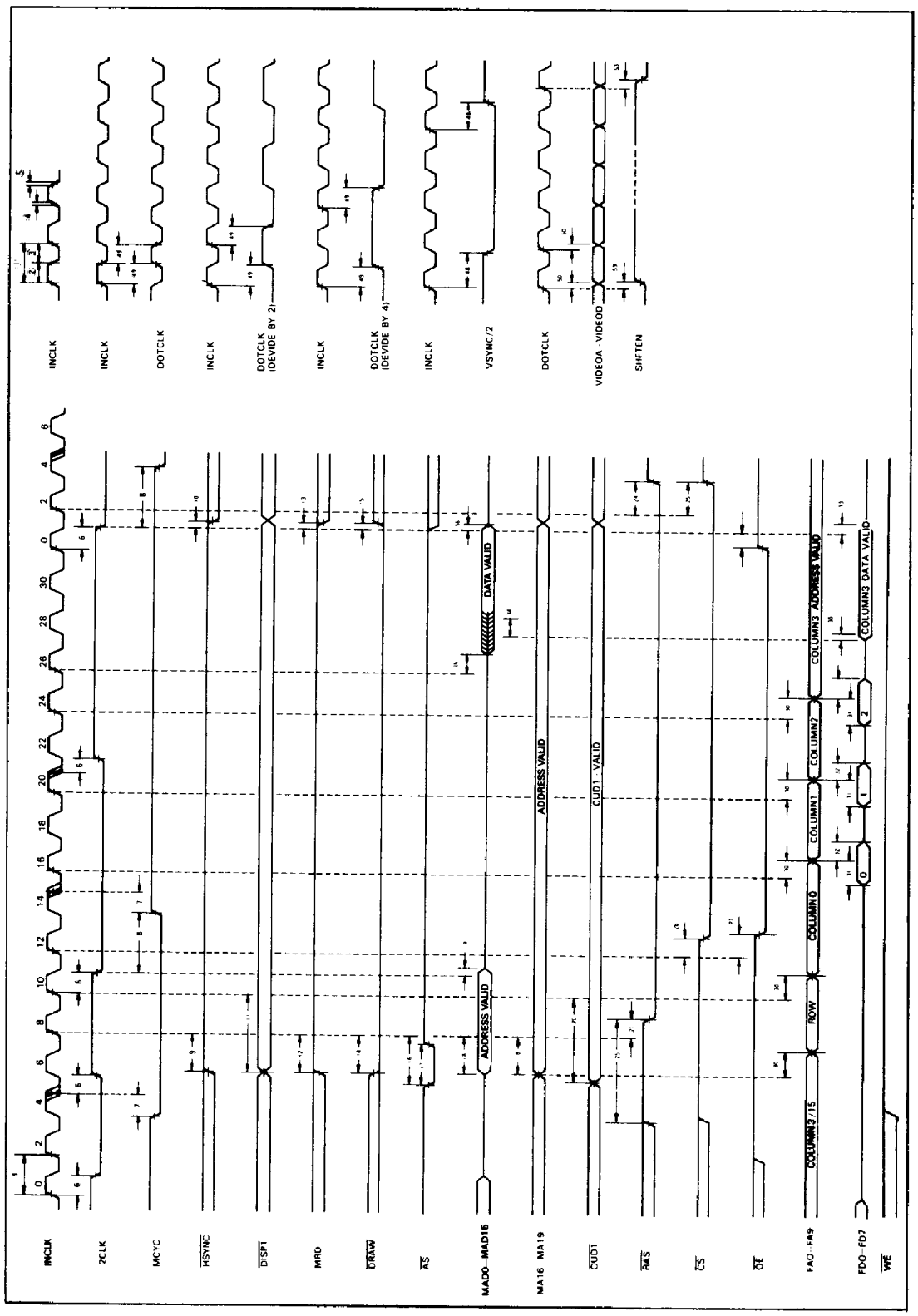


Figure 11. 1MCYC Draw Read (1 Chip)

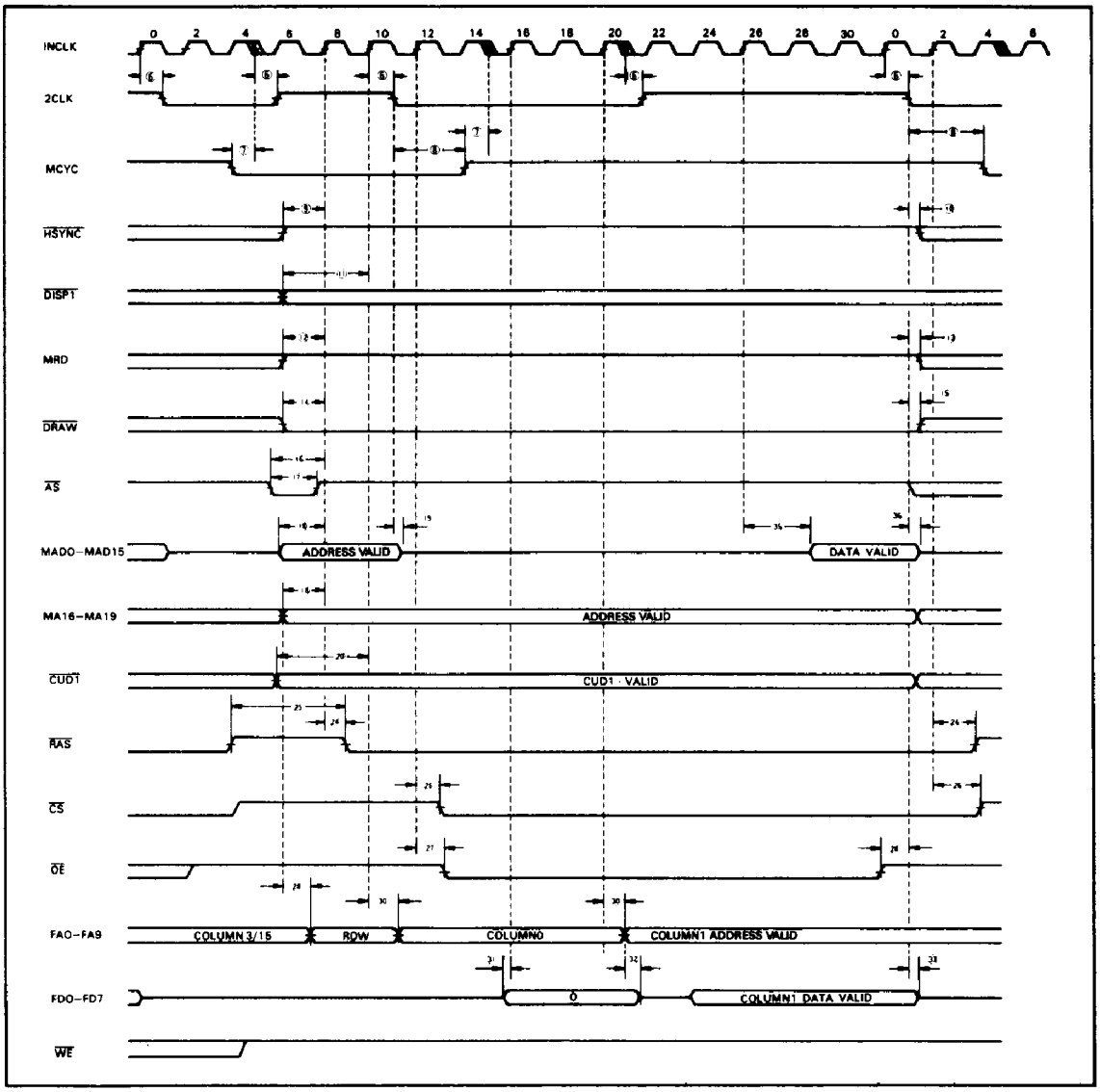


Figure 12. 1MCYC Draw Read (2 Chip)

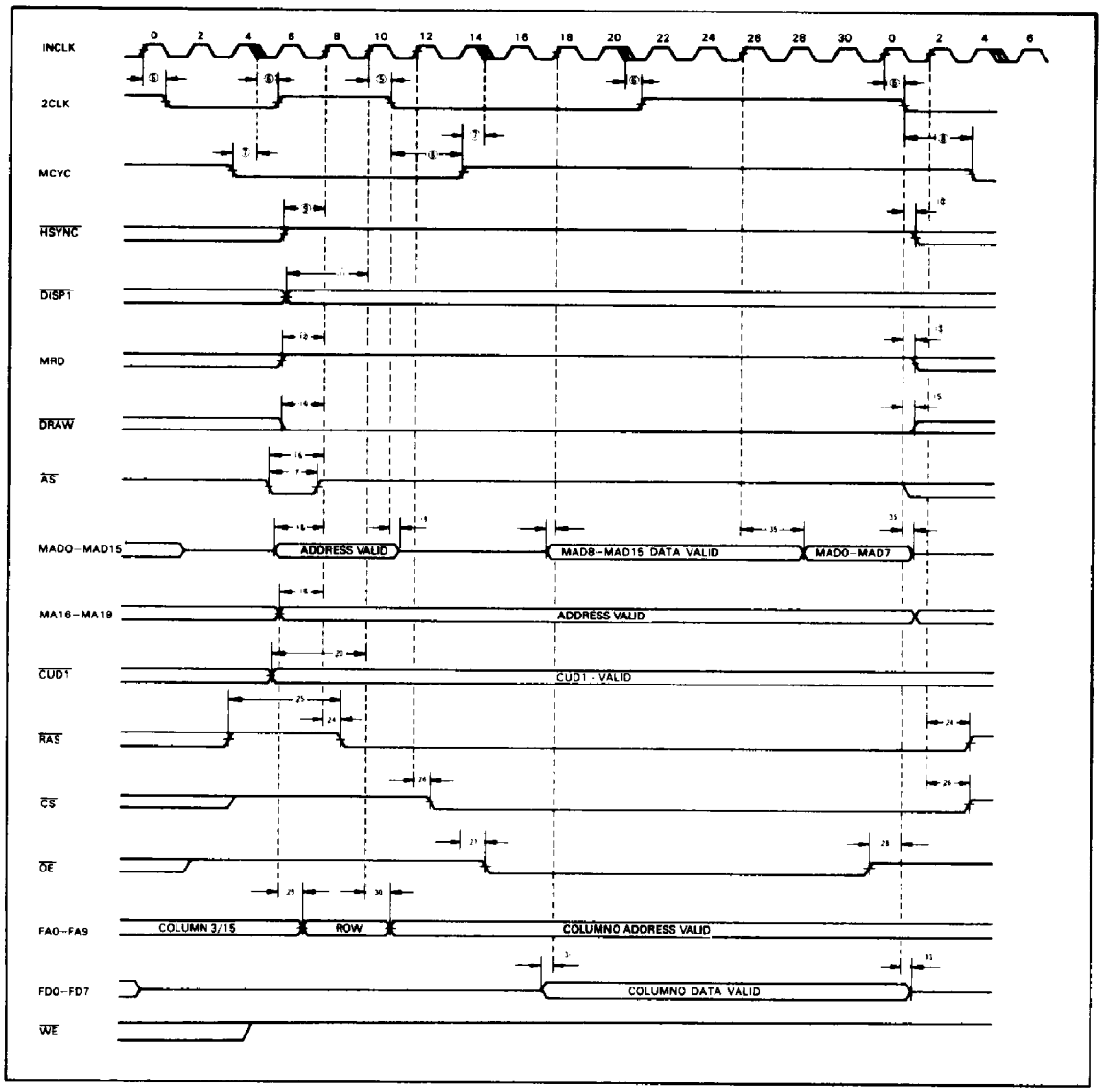


Figure 13. 1MCYC Draw Read (4 Chip)

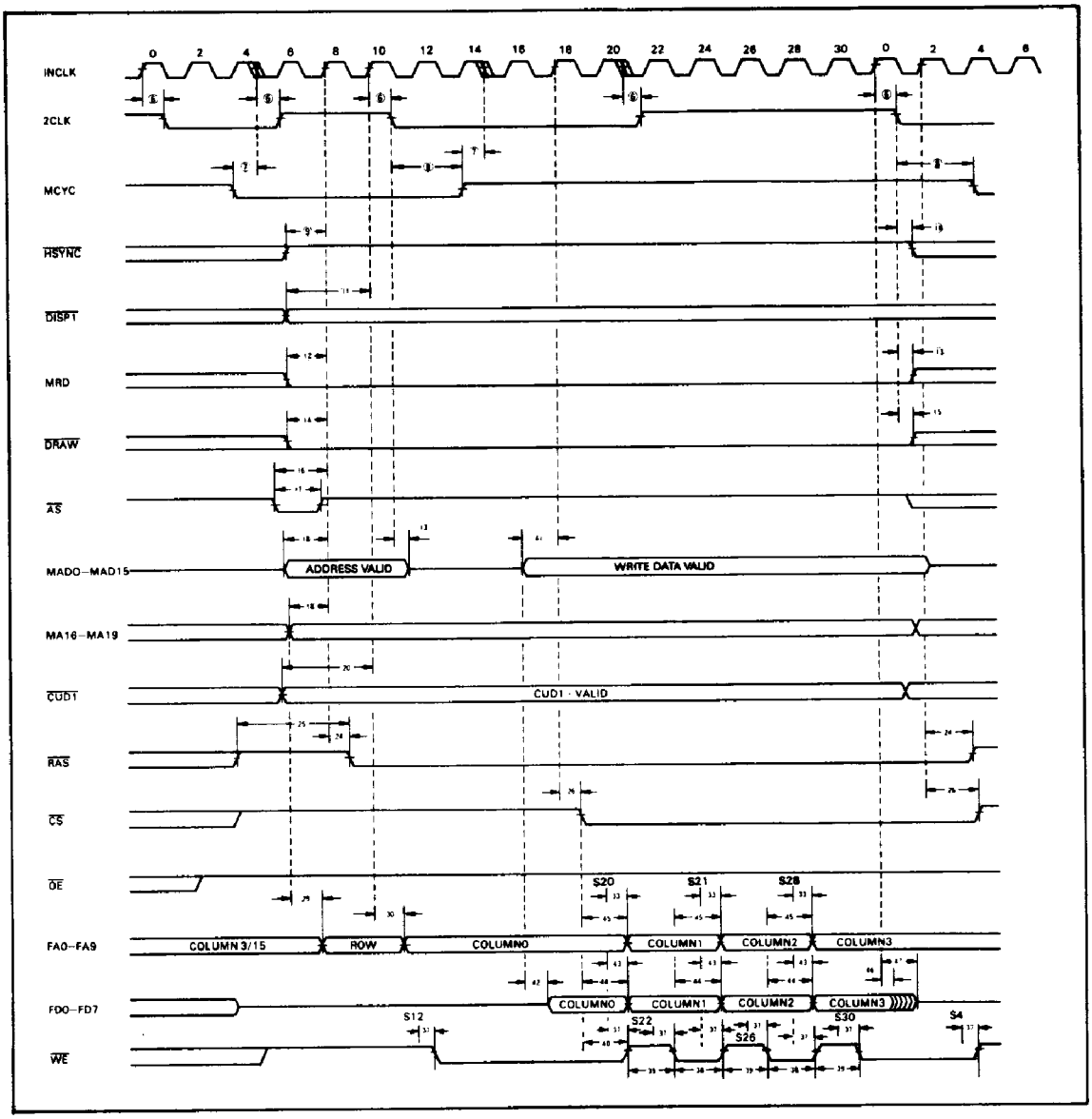


Figure 14. 1MCYC Draw Write (1 Chip)

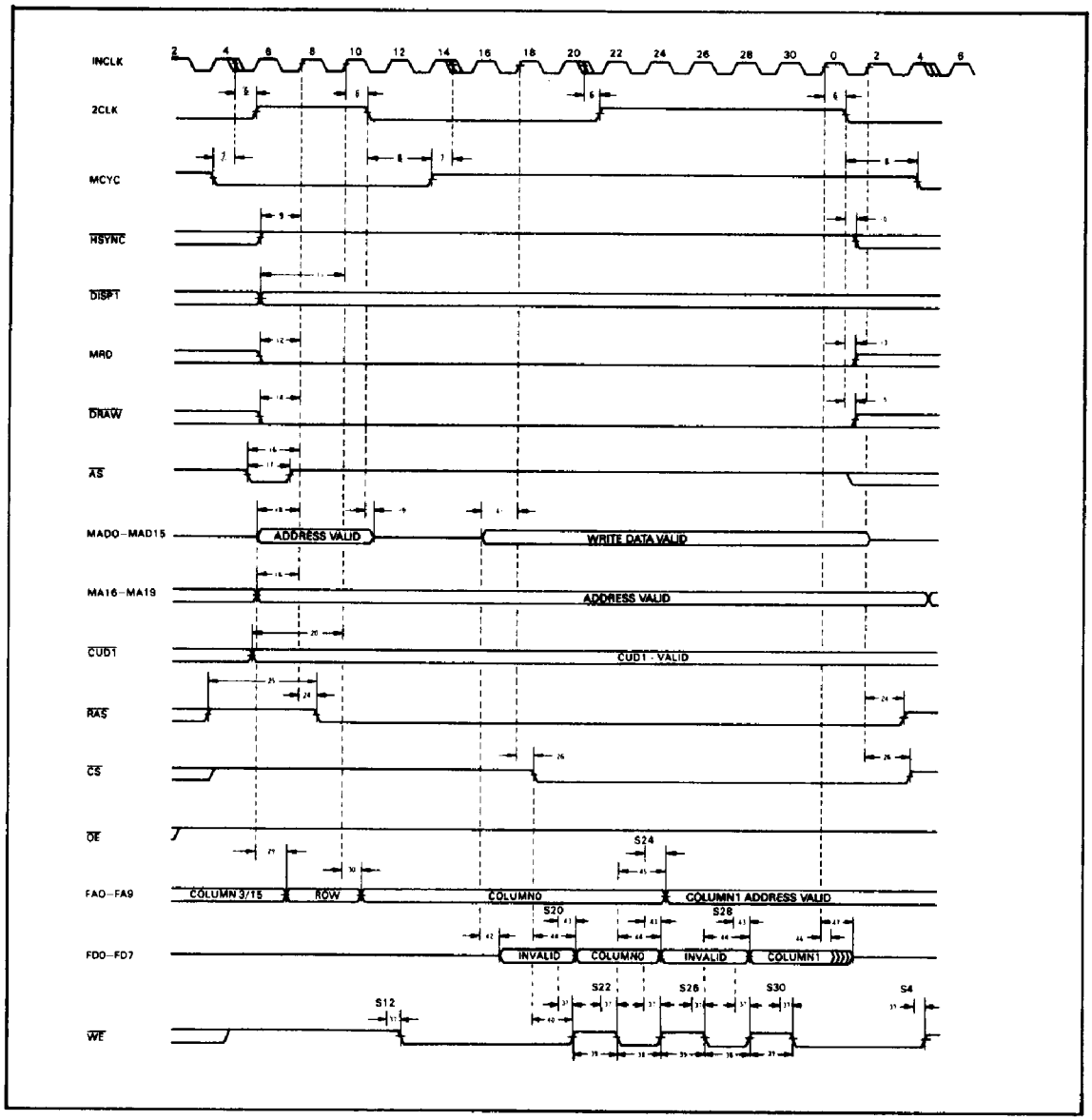


Figure 15. 1MCYC Draw Write (2 Chip)

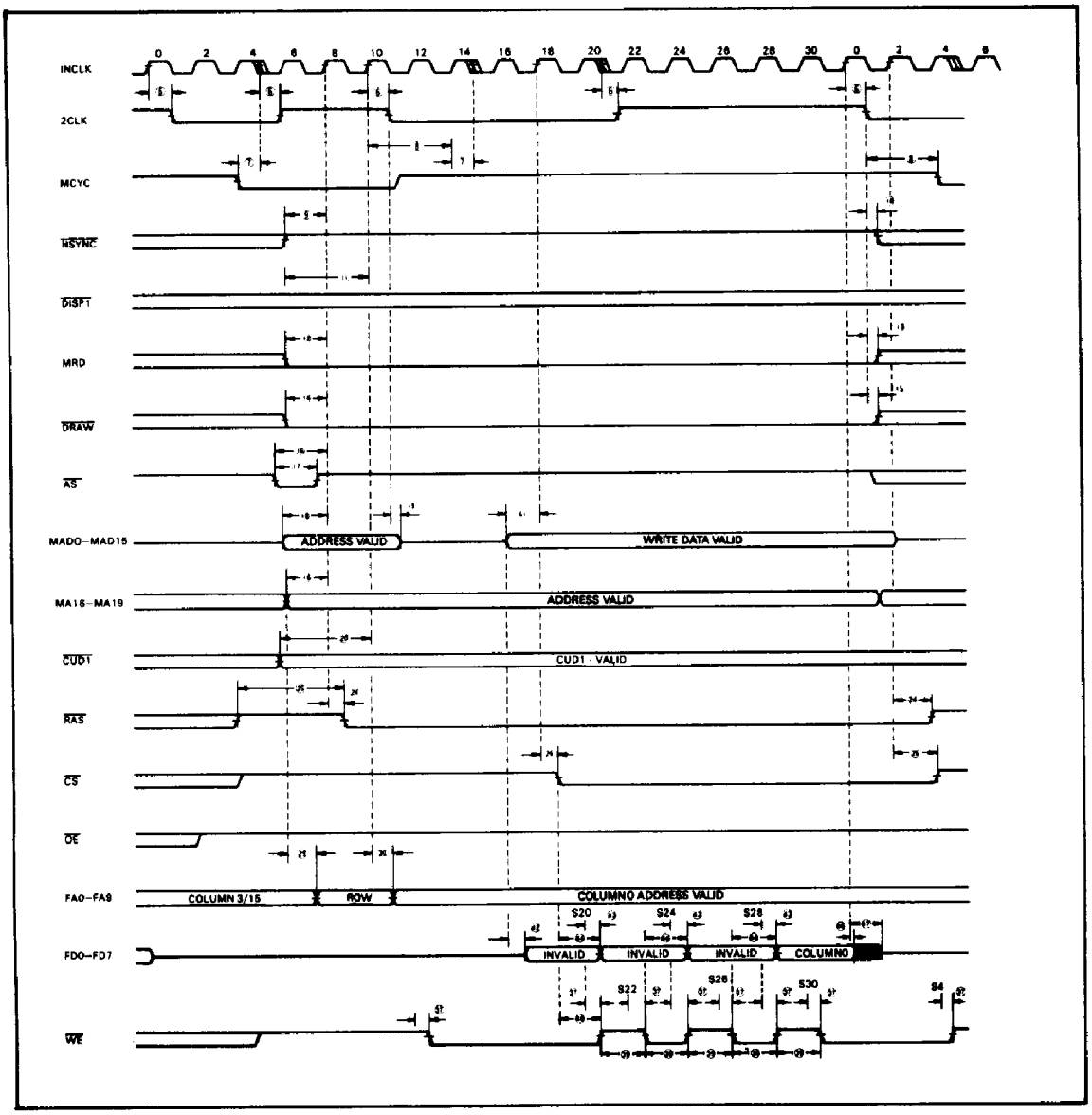


Figure 16. 1MCYC Draw Write (4 Chip)

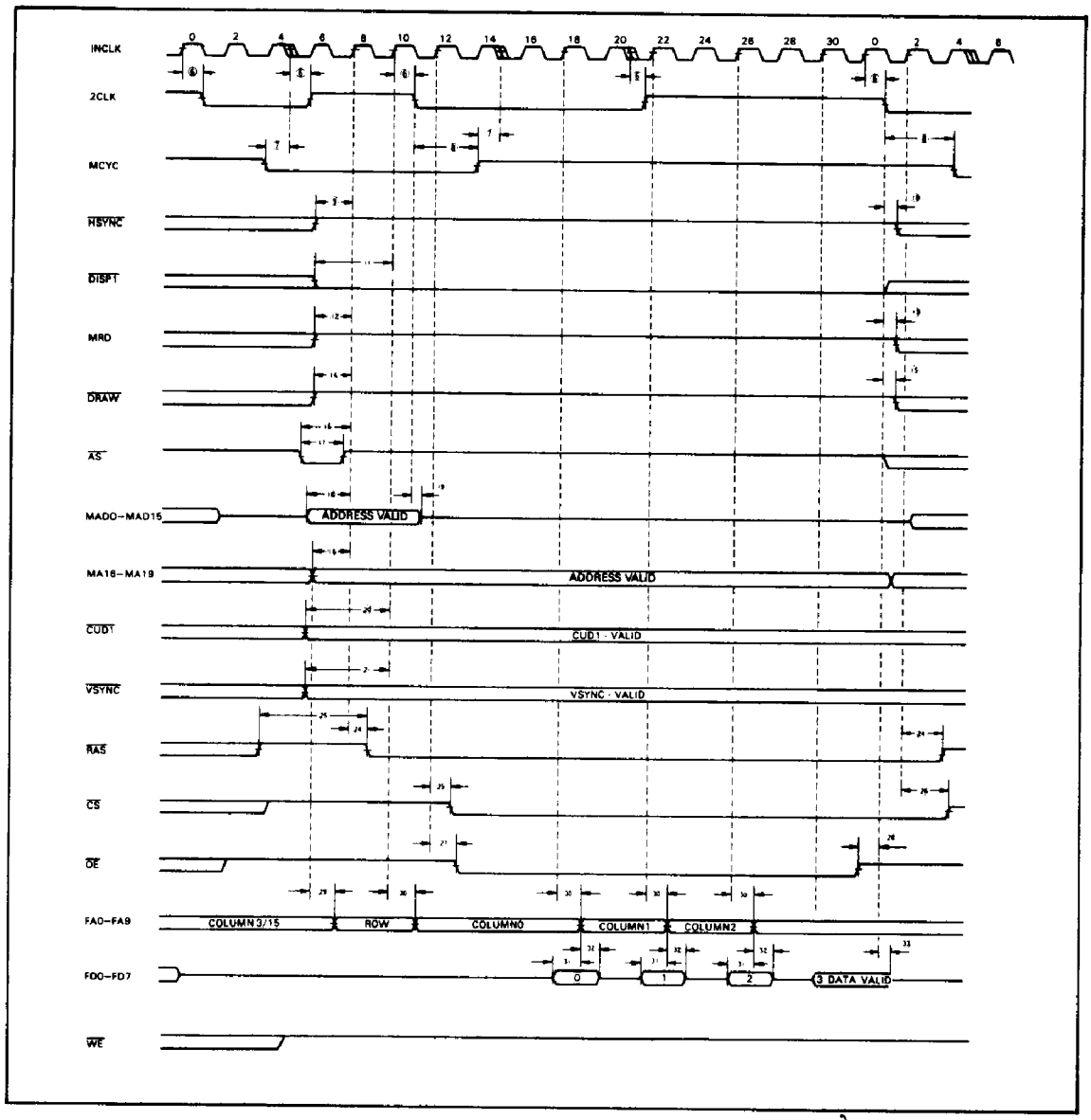


Figure 17. 1MCYC Display Read (1 or 2 Chip)

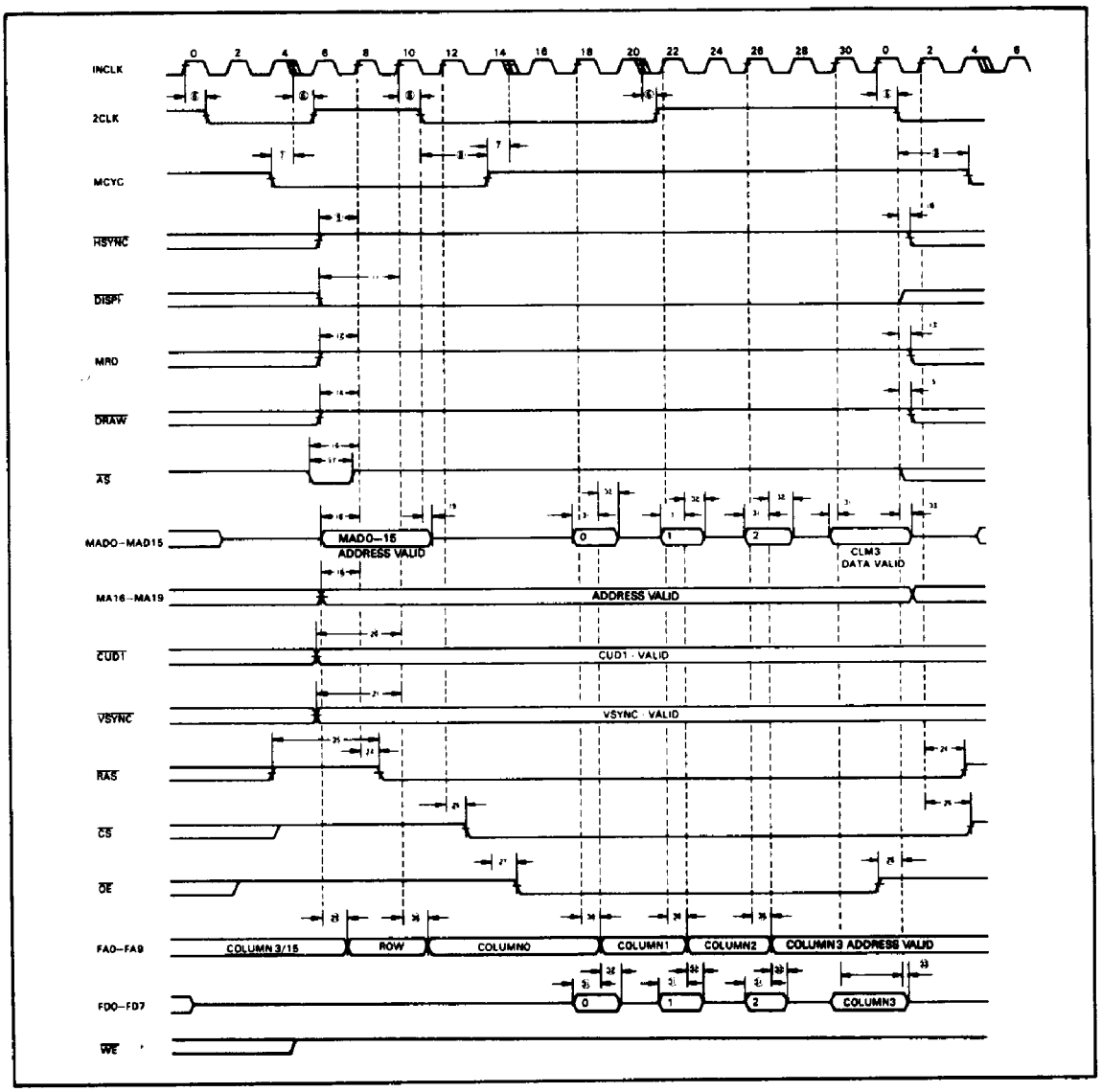


Figure 18. 1MCYC Display Read (4 Chip)

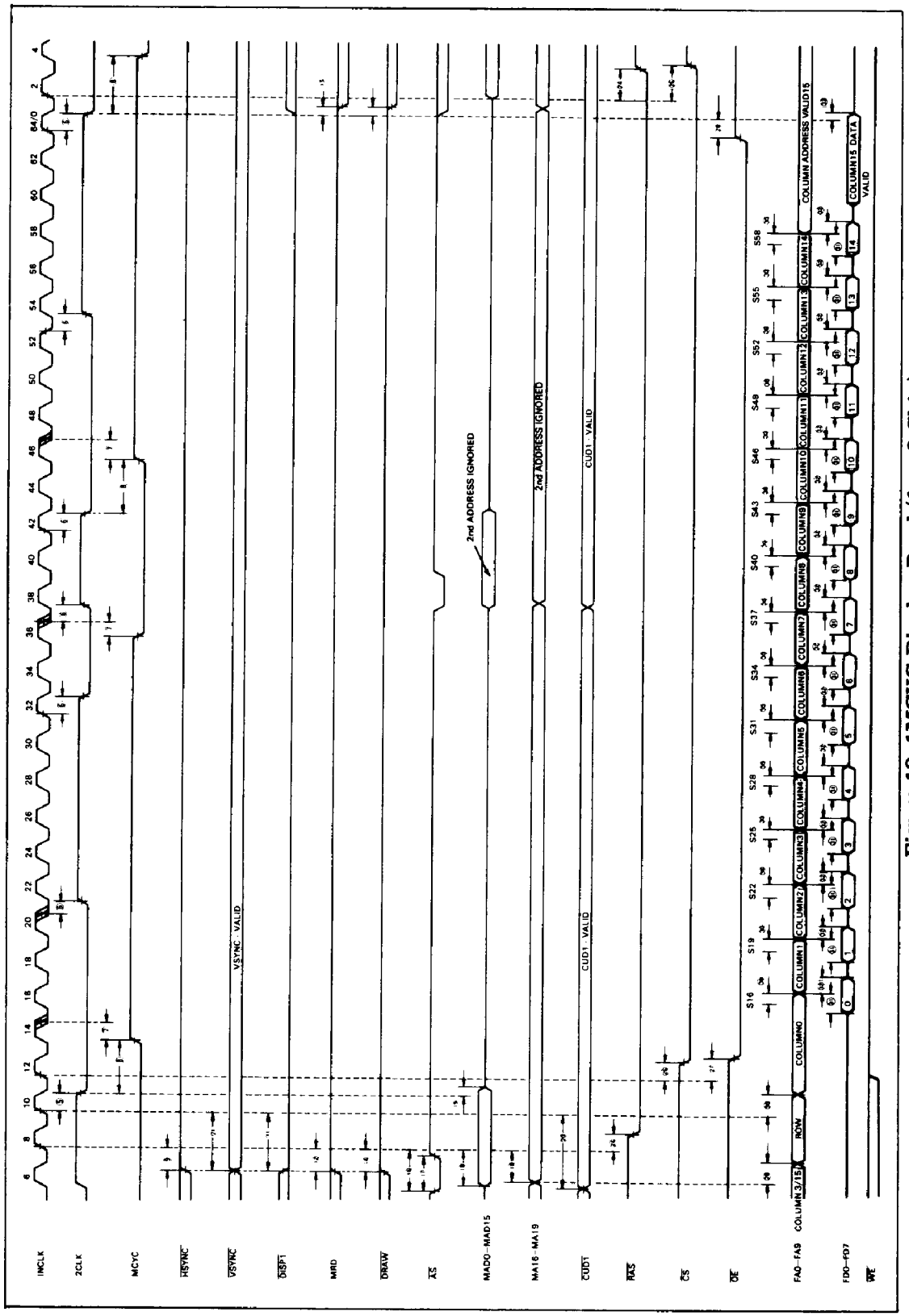


Figure 19. 1MCYC Display Read (1 or 2 Chip)

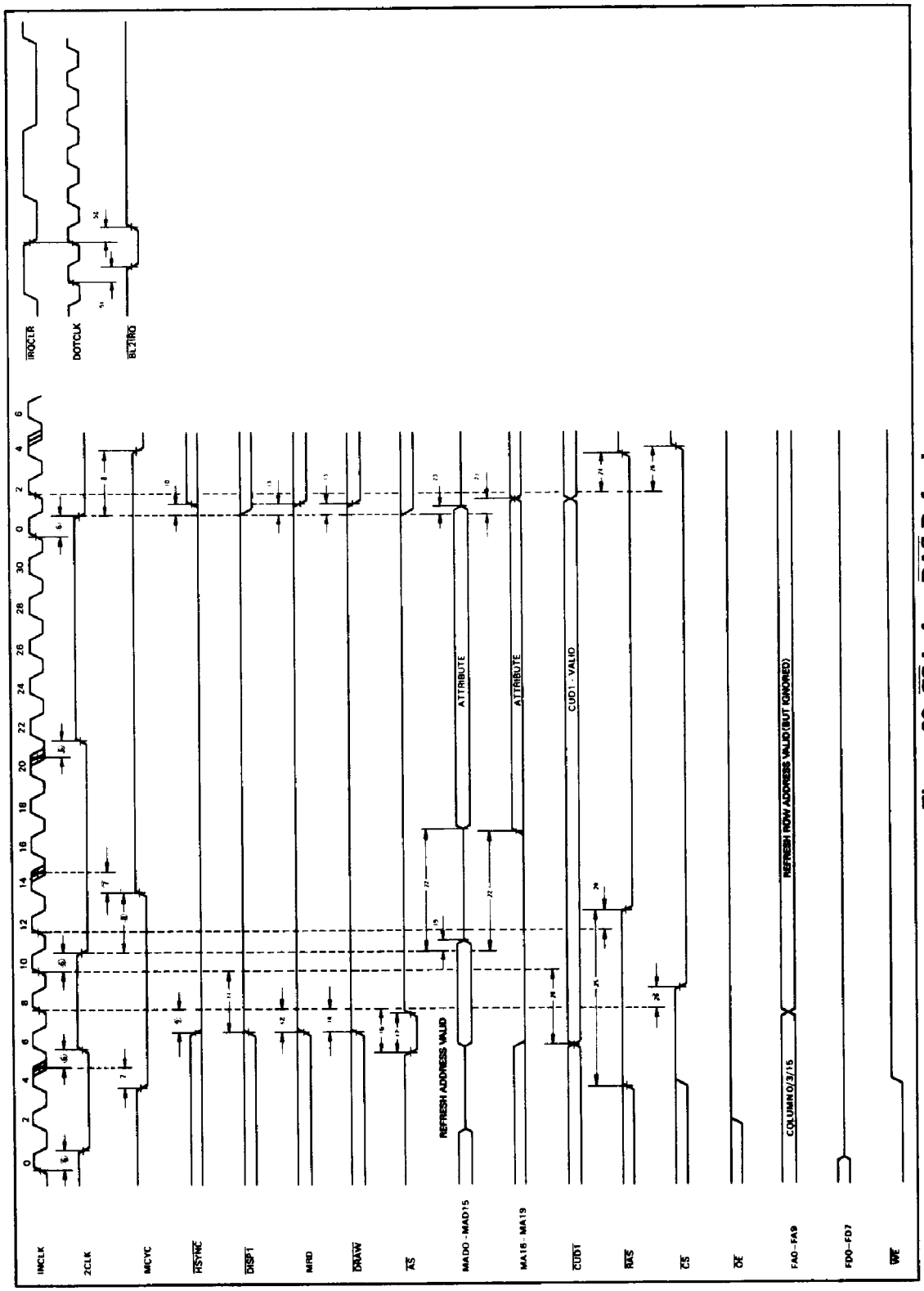


Figure 20. $\overline{CS}$ before $\overline{RAS}$ Refresh

Refer to application note (No. ADE-507-001) for detail of this product.