IC MEDIA
The Leader in CMOS Image Sensors

ICM320T

3.2 Megapixel QXGA Digital Color CMOS Image Sensor

Preliminary Data Sheet V1.0

General Description

The ICM320T is a high resolution, low power, small form factor device 3.2Megapixel digital color CMOS image sensor. The ICM320T is based on IC Media's high performance, wide acceptance angle 2.575µm TopazPixel™ technology. The ICM320T supports a 1/2.7" optical format with short track lengths of less than 7.0mm. High responsivity, low noise and image quality enhancing filters results in excellent image quality even in low light conditions.

The 2,048x1536 pixel array operates at up to 16fps at full QXGA resolution, and at progressively higher frame rates at 1/4 sub-sampled (1024x768) and 1/16 sub-sampled (512x384) resolutions. Low power consumption and few required external discrete devices makes the ICM320T ideal for small form factor, battery-operated mobile consumer devices. It consumes only 70mW at 15fps at QXGA and standby current is 8µA.

The ICM320T image sensor's registers are programmed through an efficient, two-wire serial control interface (SIF) enabling flexible control of the sensor's operating modes. It outputs 10-bit raw Bayer (RGB) pixel samples synchronized to the associated pixel clock (PCLK) as well as vertical and horizontal synchronization signals (VSYNC/HSYNC).

Feature Overview

- Wide acceptance angle pixel architecture enabling compact camera module form factors
- Very low active and stand-by power consumption
- Very good low light sensitivity
- Automatic dark level offset compensation
- Image enhancing noise cancellation filters
- Fast global reset mechanical shutter support
- High frame rate at full image resolution
- Excellent color reproduction for vibrant pictures
- Low complexity, two-wire serial control interface
- On-chip 11-bit column analog-to-digital converters with correlated double sampling
- Programmable exposure time, frame rate, sub-sampling, window size, analog and digital gain, horizontal and vertical image inversion, and dead pixel removal

Applications

- Cellular phone cameras
- Personal digital assistants
- Digital still cameras and camcorders
- Notebook and desktop PC cameras
- Video telephony and conferencing equipment
- Security systems
- Industrial and environmental systems

Key Performance Parameters

Parameter	Typical Value
Optical format	1/2.7 inches
Active pixels	2,048 x 1,536
Physical pixels	2,122 x 1,556
Pixel size	2.575 µm x 2.575 µm
Sensor area	5.27mm x 3.96mm
Responsivity	1.4 V/Lux-sec
Dynamic range	58 dB
Signal-to-noise ratio (SNR)	43 dB
Dark signal	5mV/sec
Programmable Gain	Analog: Up to 4x
	Digital: 1/256 to 64x for individual Bayer pattern pixels
Exposure time	Minimum: 34 µs
	Maximum: ~ 126 s
Frame rate	Up to 16 fps QXGA
Subsampling	1/4-rate: 1,024x768
	1/16-rate: 512x384
Input clock frequency	6 to 64 MHz
Power supply	2.8 V (analog)
	1.8 V (digital core)
	1.8-3.3 V (digital I/O)
Power consumption	70 mW (16fps@64 MHz)
Power down mode power	8 µA
Operating temperature	-20°C to +70°C
Packaging	Bare die in wafer form
	48-pin CLCC14.22

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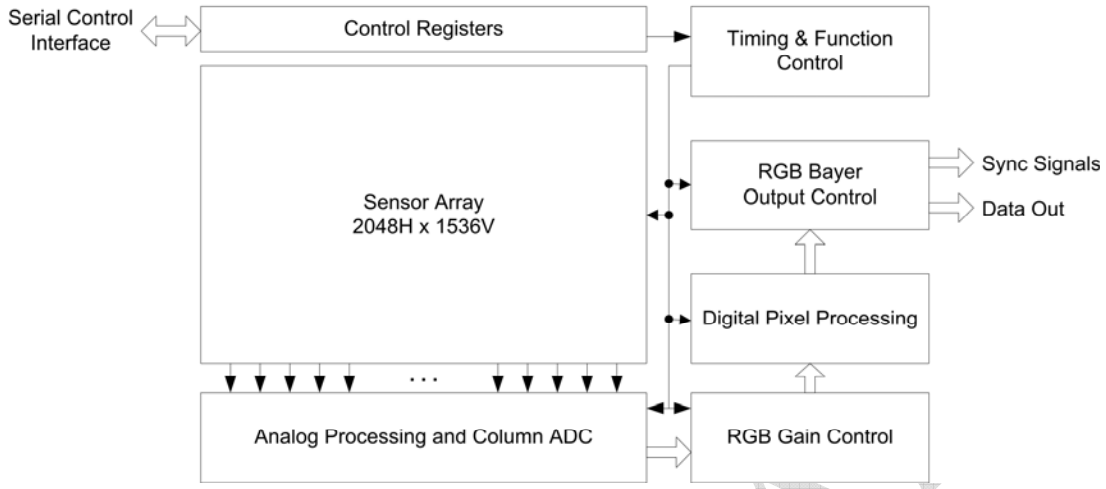

Figure 1. System Block Diagram

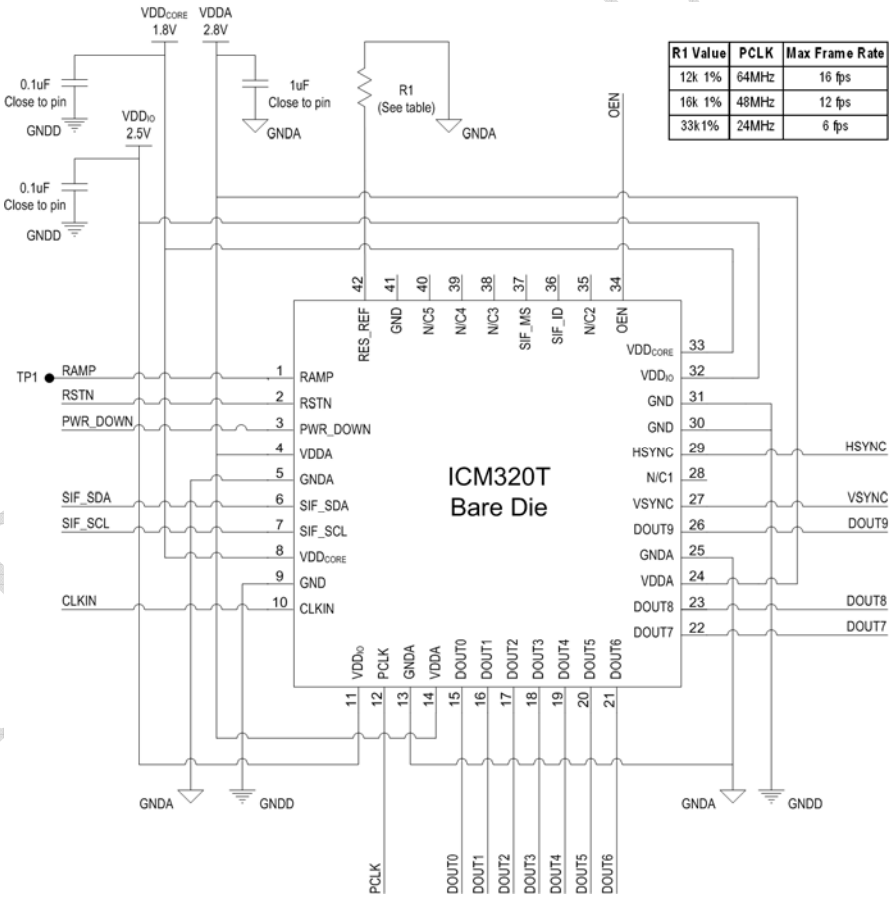

Figure 2. Cell Phone Camera Module COB Application Circuit

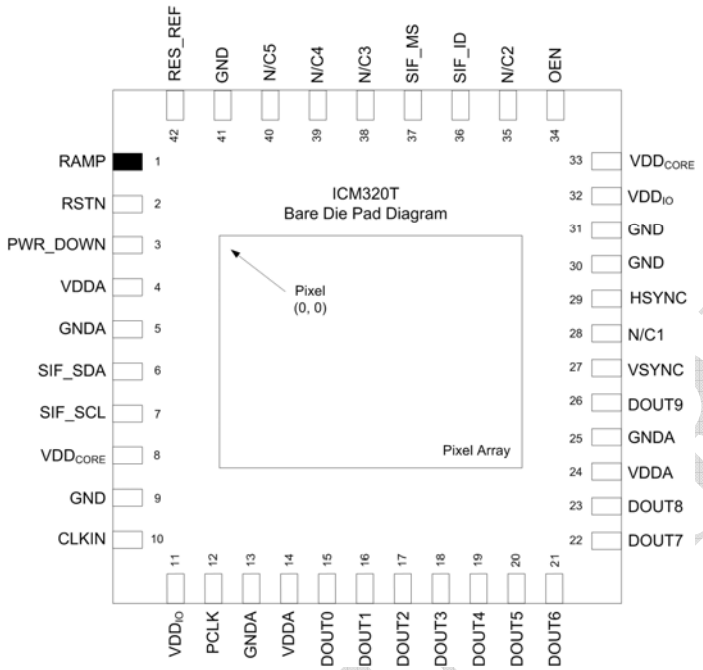

Figure 3. ICM320T Bare Die Pad Diagram

Table 1. ICM320T Bare Die Pad Assignments

Pad	Name	Class*	Function
1	RAMP	A, O	Analog ramp output
2	RSTN	D, I	Chip reset, active low
3	PWR_DOWN	D, I, N	Power down control, 0: power down, 1: active
4, 14, 24	VDDA	P	Sensor analog power (2.8V)
5, 13, 25	GNDA	P	Sensor analog ground
6	SIF_SDA	D, I/O	SIF data
7	SIF_SCL	D, I/O	SIF clock
8, 33	VDD_{CORE}	P	Sensor digital core power (1.8V)
9, 30, 31, 41	GND	P	Sensor digital ground
10	CLKIN	D, I	Clock input
11, 32	VDD_{IO}	P	Sensor I/O power (1.8-3.3V)
12	PCLK	D, O	Pixel clock output
15	DOUT [0]	D, O	Data output bit 0
16	DOUT [1]	D, O	Data output bit 1
17	DOUT [2]	D, O	Data output bit 2
18	DOUT [3]	D, O	Data output bit 3
19	DOUT [4]	D, O	Data output bit 4
20	DOUT [5]	D, O	Data output bit 5
21	DOUT [6]	D, O	Data output bit 6
22	DOUT [7]	D, O	Data output bit 7

Table 1. ICM320T Bare Die Pad Assignments (continued)

Pad	Name	Class*	Function
23	DOUT [8]	D, O	Data output bit 8
26	DOUT [9]	D, O	Data output bit 9
27	VSYNC	D, O	Vertical sync signal
28	N/C1	N/A	Reserved. Do not connect.
29	HSYNC	D, O	Horizontal sync signal
34	OEN	D, I	Output enable. 0: enable, 1: disable
35	N/C2	N/A	Reserved. Do not connect.
36	SIF_ID	D, I, N	LSB of SIF slave address
37	SIF_MS	D, I, N	SIF master/slave selection. 0: slave, 1: master (auto load from EEPROM after reset)
38	N/C3	N/A	Reserved. Do not connect.
39	N/C4	N/A	Reserved. Do not connect.
40	N/C5	N/A	Reserved. Do not connect.
42	RES_REF	A, I	Resistor to ground: 12 kΩ @ for up to 16fps QXGA (64MHz PCLK) 16 kΩ @ for up to 12fps QXGA (48MHz PCLK) 33 kΩ @ for up to 6fps QXGA (24MHz PCLK)

* **Class Codes:** A – analog signal, D – digital signal, I – input, O – output, P – power or ground, U – internal pull-up, N – internal pull-down, N/C – no connection.

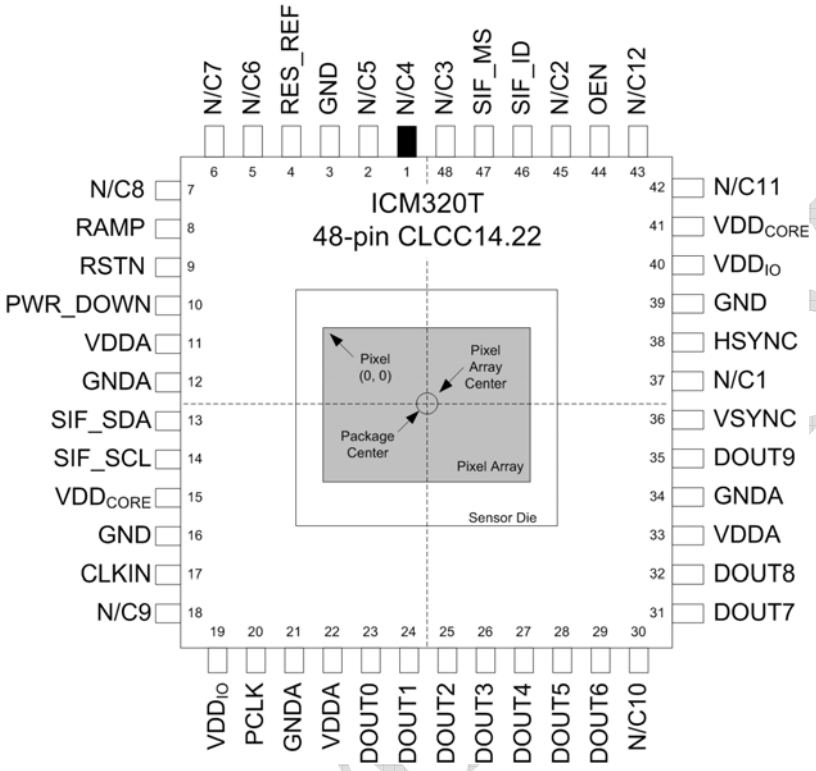

Figure 4. ICM320T 48-Pin CLCC14.22 Package

Functional Description

The ICM320T is a single-chip digital color-imaging device. It includes a 2048x1536 pixel sensor array, 2122 column-level ADCs, and correlated double sampling (CDS) circuitry. Writing into the SIF interface, which can address the register file consisting of 8-bit registers, sets all the programmable parameters. The output format is 10-bit raw Bayer RGB data, together with horizontal and vertical synchronization signals.

Image Sensor Array

The image array consists of 2122x1556 pixels. Each pixel has a light-sensitive photo diode and a set of control and transfer transistors. At the beginning of the pixel exposure cycle, a row of pixels is pre-charged to its maximum value. Then the row is exposed to light for several lines worth of time and sampled by the ADC. A CDS process subtracts the reset value (sampled right after sampling the current signal) from the signal value.

The sensor output is approximately proportional to the amount of received light, ranging from 0 to 1024. There are several dummy rows and columns surrounding the array; 64 on the left side and 10 on the top, right and bottom sides. The outer 60 of the 64 dummy pixels on the left side and outer 6 of the 10 dummy pixels on the top, right and bottom sides are covered with dark filters. The remaining dummy pixels are active pixels covered by Red, Green, and Blue color filters in a Bayer pattern. These pixels can be used for color interpolation.

The 2048x1536 (QXGA) size active signal pixel array, pixel (64, 10) through pixel (2111, 1545), is also covered by an array of Red, Green, and Blue color filters in a Bayer pattern. See Figure 5 for a detailed layout of the sensor array.

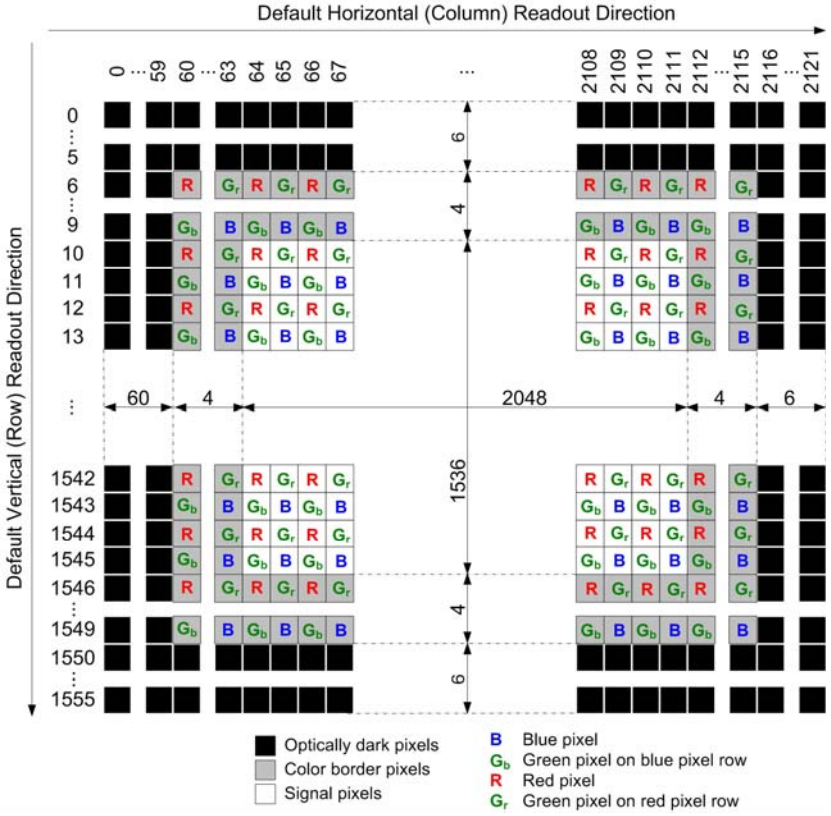

Figure 5. Image Sensor Array

Exposure Time

To accommodate different illumination requirements, you can change the exposure time on the ICM320T by adjusting registers 0x1C and 0x1D. The exposure time is measured in terms of the time to read out one line of data.

The time for processing one line is equal to the pixel clock period times the frame width. The frame width is stored in registers 0x0C and 0x0D. The exposure time for one full resolution default line width of 2200 pixel clocks is 34 μs when the pixel clock is 64 MHz.

Digital Gain Control

The ICM320T digital gain control feature is one of the methods you can use to control image quality. Adjusting the digital gain is generally used for minor changes, either to balance color or to adjust the overall image luminance. The gain range is from 1/256 to 8 of the four Bayer pattern pixels.

Gain changes require changes to two types of registers; the per Bayer color channel gain value registers 0x20-0x28, and the magnitude of change register 0x52[3:0].

Analog Gain Control

The ICM320T supports up to 4x analog gain control for low light operation. Four analog gain settings are programmable using register 0x28. The default value 0x00, corresponds to 1x gain, which is used for normal light. Other settings are 0x81: 2x gain, 0x92: 3x gain and 0xA3: 4x gain. Modified analog gain settings are activated by writing 0x1 into register 0x00[7].

Analog Gain Calibration

The analog gain can be calibrated by adjusting the maximum analog input and the maximum ADC output so that they have the same dynamic range. To enable automatic gain calibration, write 0x1 into register 0x00[1].

Pixel Timing and Function Control

The ICM320T has a software-controlled pixel analog data path. This feature allows fine-tuning of the sensor's performance and makes the sensor highly adaptable to a wide range of applications. The pixel analog data path timing is controlled by the default settings or by downloading a pixel configuration table. Register 0x02[4] makes the selection. Pixel configuration tables are sequentially downloaded into registers 0x04, 0x05, and 0x06 while incrementing the 0x03 address pointer.

Subsampling Schemes

The ICM320T supports subsampling for viewfinder and other reduced data rate output modes. It supports sub-sampled resolutions in the 1/4-rate 1024x768 and 1/16-rate 512x384 formats. The 1/4-rate mode maximum frame rate is twice the maximum full resolution frame rate. The peak 1/16-rate frame rate is four times the maximum full resolution frame rate. Subsampling modes are selected through register 0x52[7:4].

Dark Level Compensation

The ICM320T supports automatic dark level compensation with programmable offset. The automatic dark level compensation algorithm supports user programmable hysteresis to prevent oscillation of automatic exposure algorithms in companion devices. The hysteresis parameters are set using register 0x3B[2:0]. The algorithm in enabled by register 0x3B[7].

Dead Pixel Filtering

The ICM320T supports dead pixel filtering for both full QXGA resolution and sub-sampled 1/4-rate and 1/16-rate resolutions. The filter is only applied to pixels outside the high and low dead pixel filter thresholds defined in registers 0x42 through 0x45. The filter is enabled and disabled using register 0x51[3].

Pixel Noise Filtering

The ICM320T implements pixel noise suppression filtering for improved image quality under low light conditions for both full QXGA resolution and sub-sampled 1/4-rate and 1/16-rate resolutions. The pixel noise suppression filter implements a two or four pixel averaging across adjacent pixels of the same color space in sub sampled resolutions. Register 0x51[2:0] is used to enable and disable two pixel or four pixel averaging respectively.

Power Supply Noise Filtering

The ICM320T implements a power supply noise filter for removal of power supply induced row noise for improved low light image quality. The row noise filter can be automatically enabled when analog gain is applied, or manually controlled. Register 0x3B[5] is used to select manual or automatic mode. Manual control of the filter is done through register 0x3B[6]. The row noise filter can be programmed to a residual image offset value. This value is set through register 0x3C.

Fast Global Reset

The ICM320T implements a fast global reset feature in support of low cost mechanical shutters. With fast global reset, the ICM320T image sensor array can be reset in 1.5ms @ 5fps (PCLK=24 MHz). An example fast global reset image capture sequence is described in Figure 6.

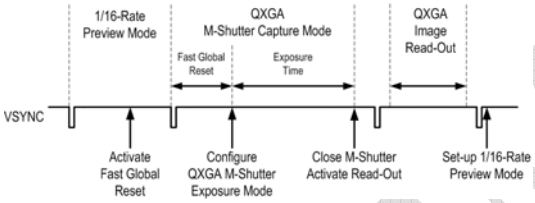

Figure 6. Fast Global Reset

Output Data Format

During normal operation, the output format is 10-bit raw data on the DOUT[9:0] data pins. In addition to the data pins, the chip also outputs VSYNC, HSYNC, and PCLK. The length and polarity of the VSYNC and HSYNC signals can be adjusted through registers 0x01[2:1] for polarity; 0x18 and 0x19 for HSYNC length; 0x1A and 0x1B for VSYNC length . The line and frame timing can be adjusted through registers 0x0C-0x0F.

Pixel Clock

The pixel clock, PCLK, is a multiple of the external clock. Although the output data is 10 bits, the internal ADC is 11 bits to minimize quantization noise. Therefore, the ADC clock is running at twice the frequency of the PCLK.

When the clock frequency changes, the RSET resistor on the RES_REF pin as well as the initialization file may also need to be changed. The value of the RSET resistor is inversely proportional to the ADC clock frequency. At 128 MHz ADC clock, the RSET is 12 kΩ; at 96 MHz ADC clock, it is 16 Ω; at 48 MHz ADC clock, it is 33 kΩ.

Power Down Mode

When the PWR_DOWN pin is de-asserted, the chip goes into power down mode. In this state, the internal clock is stopped. The PWR_DOWN pin is not synchronized with the device clock. The power down takes effect immediately. On the assertion of the PWR_DOWN pin, the sensor must wait at least 10 µs to leave the power down mode to prevent the sensor from operating in an unstable state.

Output Pin State Control

The state of the video output pins PCLK, VSYNC, HSYNC, DOUT[9:0] is controlled by the OEN pin or SIF register 0x4A[5:0]. Upon power on reset or hard reset, the video pin output state is determined by the configuration or the OEN pin. If the OEN pin is asserted (active low), the video outputs are enabled. If the OEN pin is de-asserted, the video output pins are tri-stated.

SIF register 0x4A[5:0] can be used to override the video pin output states independent of the OEN pin configuration. The video output pins are divided into three categories; CLK (PCLK), SYNC (VSYNC, HSYNC) and DATA (DOUT[9:0]). The output state for each output pin category can be independently controlled.

Serial Control Interface (SIF)

The ICM320T sensor is fully compatible with the I2C interface. Register programming is through the SIF interface (SIF_SCL and SIF_SDA pins). The default address for the 7-bit SIF device is 0x20. The SIF_ID pin can configure the last bit of the device address. The ICM320T can operate in either SIF master mode or in slave mode right after power up, depending on the pull-up or pull-down of the SIF_MS pin.

When the SIF_MS pin is pulled down during power up, the ICM320T's SIF interface is

operated as a SIF slave device, waiting to be controlled by an external SIF master such as a microprocessor. When SIF_MS is pulled-up during power up, the SIF interface is first acting as a SIF master device trying to read from an external SIF EEPROM. After that, the SIF interface returns to slave mode.

SIF Registers

Table 2. SIF Registers Descriptions

<table>
<tr><th>Bit Description</th><th>Default</th><th>Affected by Latent Register</th><th>Frame Boundary Update</th></tr>
<tr><td colspan="4">0x00 PART CONTROL</td></tr>
<tr><td>Processing control
[0] 0: Normal mode. 1: Single frame mode.

[1] Slope adjustment enable

[2] Exposure time control. Writing a ‘1’ will activate the new value set in 0x1C and 0x1D, when read back from it. A ‘0’ means that the exposure time change is finished. A ‘1’ means that the exposure time change is still in progress.

[6:3] Frame rate for different ADC clock frequencies.
<table>
<tr><th rowspan="2">Value</th><th colspan="3">ADC clock frequency</th></tr>
<tr><th>48 MHz</th><th>96 MHz</th><th>128 MHz</th></tr>
<tr><td>0x0</td><td>6 fps</td><td>12 fps</td><td>16 fps</td></tr>
<tr><td>0x1</td><td>3 fps</td><td>6 fps</td><td>8 fps</td></tr>
<tr><td>0x2</td><td>2 fps</td><td>4 fps</td><td>5 fps</td></tr>
<tr><td>0x3</td><td>1 fps</td><td>2 fps</td><td>2.3 fps</td></tr>
<tr><td>0x4</td><td>0.85 fps</td><td>1.7 fps</td><td>1.9 fps</td></tr>
<tr><td>0x5</td><td>0.6 fps</td><td>1.2 fps</td><td>1.0 fps</td></tr>
<tr><td>0x6</td><td>0.4 fps</td><td>0.8 fps</td><td>0.5 fps</td></tr>
<tr><td>0x7</td><td>0.2 fps</td><td>0.4 fps</td><td></td></tr>
</table>
[7] Latent change. Writing a ‘1’ means that the changed latent registers now start taking effect. When the entire operation is done, the read back value of this bit will change from ‘1’ to ‘0’.</td><td>0x00</td><td>Y</td><td>Y</td></tr>
</table>

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x01 TIMING CONTROL (LSB) **0x02 TIMING CONTROL (MSB)**			
Timing control [0] Column count enable, set to 0 when filling register file, set to 1 when normal operation [1] HSYNC polarity 0: active low, 1: active high The DOUT[5] pin determines the initial value [2] VSYNC polarity 0: active low, 1: active high The DOUT[6] pin determines the initial value [3] Auto dark correction enable When this bit is set, register 0x3B will decode which auto-dark correction scheme will be used [4] Timing select, 0: register file timing, 1: default timing [6] Flash polarity, 0: active low, 1: active high [7] Blank polarity, 0: active low, 1: active high [8] IRST select, 0: from register file, 1: from IRST_NUMBER register [10] Capture: when in single frame mode, writing a 1 here will start a frame capture [11] Dead column removal mode, 0: color, 1: black-and-white [12] Out-of-array exposure pointer control, 0: point to row 487, 1: point to row 490 (a non-existent row) [13] Column stop, 0: sensor column counter stop at 649 when exceeding real array, 1: sensor column counter keeps counting.	0x0011	N	N
0x03 PIXEL CONFIGURATION TABLE INDEX			
[4:0] Index to the pixel configuration table register file.	0x00	N	N
0x04 PIXEL CONFIGURATION TABLE DATA (L) **0x05 PIXEL CONFIGURATION TABLE DATA (M)** **0x06 PIXEL CONFIGURATION TABLE DATA (H)**			
Reserved.	0x000000	N	N
0x07 PIXEL CONFIGURATION TABLE LENGTH			
[4:0] Pixel configuration table register file length	0x00	N	N
0x08 LOAD PIXEL CONFIGURATION TABLE DATA			
Writing into this register causes the pixel configuration table data in registers 0x04-0x06 to be written into the pixel configuration table entry that is indexed by register 0x03.	0x01	N	N
0x09 through 0x0B			
Reserved	0x0000	N	N
0x0C FRAME WIDTH (LSB) **0x0D FRAME WIDTH (MSB)**			
[10:0] Defines the frame width. The frame width must be more than AD_COL_BEGIN+ 2068.	0x0898 (2200)	Y	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x0E FRAME HEIGHT (LSB) **0x0F FRAME HEIGHT (MSB)**			
[15:0] Defines the frame height. The frame height must be more than AD_ROW_BEGIN + 1556.	0x071C (1820)	Y	Y
0x10 IMAGE READOUT CONTROL (LSB) **0x11 IMAGE READOUT CONTROL (MSB)**			
[9:0] Beginning of the active line in terms of column position. [10] Left-right mirror image enable. [11] Image flip up-down image.	0x0064 (100)	Y	Y
0x14 ROW START ADDRESS (LSB) **0x15 ROW START ADDRESS (MSB)**			
[15:0] The beginning of the active frame in terms of row position.	0x000A (10)	Y	Y
0x18 HSYNC PULSE WIDTH (LSB) **0x19 HSYNC PULSE WIDTH (MSB)**			
[10:0] Defines the HSYNC pulse width, which is the end of the horizontal sync in terms of column position.	0x0040 (64)	Y	Y
0x1A VSYNC PULSE WIDTH (LSB) **0x1B VSYNC PULSE WIDTH (MSB)**			
[15:0] Defines the VSYNC pulse width, which is the end of the vertical sync in terms of row position.	0x0003 (3)	Y	Y
0x1C EXPOSURE TIME CONTROL (LSB) **0x1D EXPOSURE TIME CONTROL (MSB)**			
[15:0] Exposure time in terms of number of rows.	0x071B (1819)	N	Y
0x20 GAIN BAYER CHANNEL 1 (LSB) **0x21 GAIN BAYER CHANNEL 1 (MSB)**			
[10:0] Bayer channel 1 gain coefficient. (Gr) in unsigned 3.8 (default) format.	0x0100 (256)	Y	Y
0x22 GAIN BAYER CHANNEL 2 (LSB) **0x23 GAIN BAYER CHANNEL 2 (MSB)**			
[10:0] Bayer channel 2 gain coefficient. (R) in unsigned 3.8 (default) format.	0x0100 (256)	Y	Y
0x24 GAIN BAYER CHANNEL 3 (LSB) **0x25 GAIN BAYER CHANNEL 3 (MSB)**			
10:0] Bayer channel 3 gain coefficient. (B) in unsigned 3.8 (default) format.	0x0100 (256)	Y	Y
0x26 GAIN BAYER CHANNEL 4 (LSB) **0x27 GAIN BAYER CHANNEL 4 (MSB)**			
[10:0] Bayer channel 4 gain coefficient. (Gb) in unsigned 3.8 (default) format.	0x0100 (256)	Y	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x28 ANALOG GAIN CONTROL			
[7:4] Analog gain settings for low light operation 0x00: 1x gain (default) 0x81: 2x gain 0x92: 3x gain 0xA3: 4x gain Others: Reserved	0x00	Y	Y
0x29 through 0x3A			
Reserved.			
0x3B ROW NOISE FILTER AND DARK LEVEL COMPENSATION			
[7]: Enable frame based auto dark correction 1: enable 0: disable [6]: Enable row noise filter 1: enable 0: disable Note: bit[7] should be set to '0' if row noise filter is enabled. [5]: Auto enable row noise filter 1: Automatic activation mode 0: Manual activation mode Setting this bit will turn on row noise filter automatically when analog sensor gain is applied [2:0]: Frame based auto dark correction hysteresis control 0: 4 frames 1: 8 frames 2: 16 frames	0x00	N	Y
0x3C ROW NOISE FILTER IMAGE OFFSET			
Image offset value when row noise filter is enabled.	0x0a	N	Y
0x3D FRAME BASED DARK COMPENSATION IMAGE OFFSET			
Image offset value for frame based dark level compensation.	0x00	N	Y
0x3E through 0x3F			
Reserved.			
0x40 DARK OFFSET SUBTRAHEND (LSB) **0x41 DARK OFFSET SUBTRAHEND (MSB)**			
[9:0] When auto dark correction is disabled, serve as the subtrahend for dark correction	0x0000	N	Y
0x42 HIGH DEAD PIXEL THRESHOLD (LSB) **0x43 HIGH DEAD PIXEL THRESHOLD (MSB)**			
[9:0] Apply dead pixel removal algorithm only to pixels above HighLimit	0x003FF (1023)	N	N

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x44 LOW DEAD PIXEL THRESHOLD (LSB) **0x45 LOW DEAD PIXEL THRESHOLD (MSB)**			
[9:0] Apply dead pixel removal algorithm only to pixels below LowLimit.	0x0000	N	N
0x46 through 0x49			
Reserved.			
0x4A VIDEO OUTPUT CONTROL			
[7] : Soft reset (auto clear) [6] : Reserved. [5]: Set PCLK pin output state during standby mode 1: PCLK set to Low ('0') during stand-by mode 0: PCLK tri-stated (Z') during stand-by mode [4]: Set SYNC pin output states during standby mode 1: HSYNC/VSYNC set to Low ('0') during stand-by mode 0: HSYNC/VSYNC tri-stated (Z') during stand-by mode [3]: Set DATA pin output states during standby mode 1: DOUT[9:0] set to Low ('0') during stand-by mode 0: DOUT[9:0] tri-stated (Z') during stand-by mode [2]: PCLK pin output state during video mode 1: PCLK output tri-stated 0: PCLK output active [1]: SYNC pin output state during video mode 1: HSYNC/VSYNC outputs tri-stated 0: HSYNC/VSYNC outputs active [0]: DATA pin output state during video mode 1: DATA[9:0] outputs tri-stated 0: DATA[9:0] outputs active	0x00	N	N
0x4B to 0x50			
Reserved.			

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x51 DEAD PIXEL AND AVERAGING FILTER CONTROL			
[0]: Column average for 1/4-rate subsampling (2-point average) 1: Enable 0: Disable [1]: Column average for 1/16-rate subsampling (4-point average) 1: Enable 0: Disable [2]: Row average for both sub-sampling modes 1: Enable 0: Disable [3]: Dead pixel filter for sub-sampling mode 1: Enable 0: Disable	0x00	N	Y
0x52 OUTPUT FORMAT CONTROL			
[3:0] Global digital gain 0x0: 1x gain (default) 0x1: 2x gain 0x2: 4x gain 0x3: 8x gain Others: 1x gain [7:4] Output format 0x0: Normal mode (default) 0x1: Reserved. 0x2: 1/16-rate subsampling mode (1024x768 format) 0x3: 1/4-rate subsampling mode (512x384 format) 0x4: Control signal 0x5: Sensor row 0x6: Sensor column Others: Normal mode	0x00	N	Y
0x53 to 0x81			
Reserved.			
0x82 DEVICE ID **0x83 DEVICE ID**			
[3:0] Sub ID. Can be configured using SIF [15:4] Device ID, default 0xB10. Can be configured using SIF.	0xB100 (45312)	N	N
0x84 FLASH START POSITION (LSB) **0x85 FLASH START POSITION (MSB)**			
[15:0] Flash begin position in terms of rows.	0x0614 (1556)	N	Y

Table 2. SIF Registers Descriptions (continued)

Bit Description	Default	Affected by Latent Register	Frame Boundary Update
0x86 FLASH END POSITION (LSB) **0x87 FLASH END POSITION (MSB)**			
[15:0] Flash end position in terms of rows	0x071C (1820)	N	Y
0x88 through 0x9C			
Reserved.			
0x9D MAXIMUM EXPOSURE TIME INCREASE (LSB) **0x9E MAXIMUM EXPOSURE TIME INCREASE (MSB)**			
[15:0] Maximum step size for exposure time increase.	0x0618 (1560)	Y	Y
0x9F through 0xB3			
Reserved			
0xB4 PLL CONFIGURATION (LSB) **0xB5 PLL CONFIGURATION (MSB)**			
PLL pre-divider (M), multiplier (N) and post-divider (R) settings for generation of the on-chip ADC clock (ADCLK) based on the input clock (CLKIN) frequency. The M, N and R settings must be such that the ADC clock is 2x the frequency of the desired output PCLK. The following equation is used to derive the ADCLK based on a given CLKIN and M, N and R settings: ADCLK = N x CLKIN / (M x R) [11:10]: PLL post divider (R) [9:8] : PLL pre-divider (M) [5:0] PLL multiplier (N)	0x0001 (1)	N	Y
0xB6 through 0xFF			
Reserved			

PLL N, R and M Settings

[5:0]		[11:10]		[9:8]	
0x0	N = 1	0x0	R = 1 (D)	0x0	M = 1 (D)
0x1	N = 2 (D)	0x1	R = 2	0x1	M = 2
0x2	N = 3	0x2	R = 3	0x2	M = 3
0x3	N = 4	0x3	R = 4	0x3	M = 4
0x4	N = 8				
0x5	N = 16				

* Reserved bits must *not* be changed

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Specification		Rating
Supply voltage	V_{DDA}	3.6 V
	V_{DD}	2.1 V
	V_{DDIO}	3.6V
Input voltage		-0.3 V to V_{DDIO} +0.3V
Output voltage		-0.3 V to V_{DDIO} +0.3V
Storage temperature		0 to 65°C
ESD rating	Human body model [1]	2,000 V
	Machine model [2]	200 V
Latch-up protection [3]		125 mA
Convection or IR reflow temperature [4]		240°C for 20 seconds

Notes: [1] EIA/JESD22-A114
[2] EIA/JESD22-A115
[3] EIA/JESD78
[4] IPC/JEDEC-J-STD-020C

Electrical Characteristics

DC Characteristics

(V_{DDC}=1.8V, V_{DDIO}=2.5V, V_{DDA}=2.8V, T_A=25°C)

Table 4. DC Characteristics

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
V_{DDA}	Absolute Power Supply	-0.3		3.6	V
V_{INA}	Absolute Input Voltage	-0.3		V_{DDIO} + 0.3	V
V_{OUTA}	Absolute Output Voltage	-0.3		V_{DDIO} + 0.3	V
T_{STG}	Storage Temperature	0	25	65	°C
V_{DDA}	Analog Operating Power Supply	2.7	2.8	2.9	V
V_{DDC}	Digital Core Operating Power Supply	1.7	1.8	2.1	V
V_{DDIO}	Digital I/O Operating Power Supply	1.8	2.5	3.3	V
V_{IN}	Operating Input Voltage	0		V_{DDIO}	V
I_{DDA}	Analog Supply Current (15 fps @ 64 MHz)		14		mA
I_{DDC}	Digital Core Supply Current (15 fps @ 64 MHz)		12		mA
I_{DDIO}	Digital I/O Supply Current (15 fps @ 64 MHz)		4		mA
I_{IL}	Input Low Current	-1		1	µA
I_{IH}	Input High Current	-1		1	µA
I_{OZ}	Tri-state Leakage Current	-10		10	µA
C_{IN}	Input Capacitance		3		pF
C_{OUT}	Output		3		pF

Table 4. DC Characteristics (continued)

Symbol	Parameter	Rating			Unit
		Minimum	Typical	Maximum	
	Capacitance				
C_{BID}	Bi-directional Buffer Capacitance		3		pF
V_{IL}	Input Low Voltage			0.3 * V_{DDIO}	V
V_{ILS}	Schmitt Input Low Voltage		1.1		V
V_{IH}	Input High Voltage	0.7 * V_{DDIO}			V
V_{IHS}	Schmitt Input High Voltage		1.8		V
V_{OL}	Output Low Voltage			0.4	V
V_{OH}	Output High Voltage	0.7 * V_{DDIO}			V
R_L	Input Pull-up/down Resistance		12		KΩ

AC Characteristics

Table 5. AC Characteristics

Parameter	Minimum	Typical	Maximum	Condition	Pin
Setup time	No input pin needed for Setup and Hold time requirements.				
Hold time	SDA/SCL are subject to I2C protocol.				
Rise time			TBD	25pf load	PCLK, HSYNC, VSYNC, DOUT[10:0]
Fall time			TBD	25pf load	PCLK, HSYNC, VSYNC, DOUT[10:0]
Clock duty	40	50	60		%
DCG range		16			

Sensor Timing

The following sections discuss the timing requirements and formats for the ICM320T image sensor. Note that the timing requirements are related to the pixel clock and the format depends on the subsampling mode.

Reset Timing

The reset timing reset signal RSTN must be asserted for more than two stable clock cycles. In addition, the VDD voltage ramp must be above 90% of its specified value for more than two stable clock cycles as shown in Figure 7.

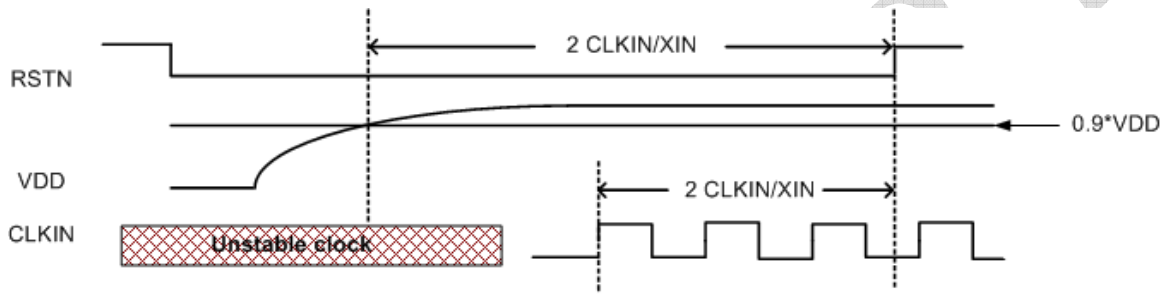

Figure 7. Reset Timing

Pixel Output Timing

The pixel data and timing output signals are DOUT [9:0], PCLK, VSYNC, and HSYNC. Data should be latched at the rising edge of the PCLK. The VSYNC and HSYNC signals are asserted and de-asserted at the falling edge of the PCLK. See Figure 8.

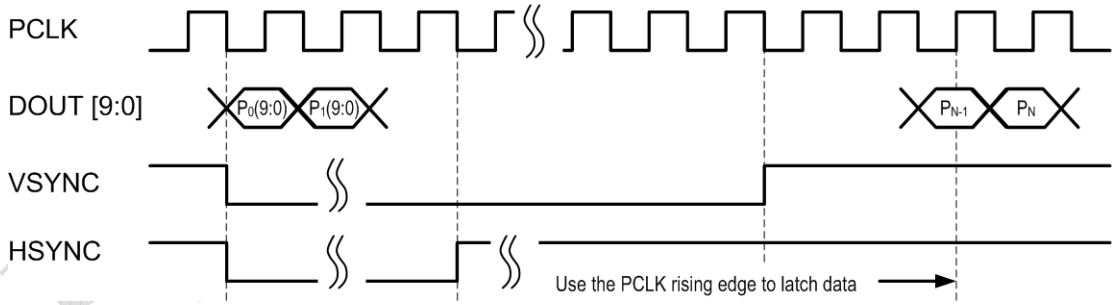

Figure 8. Pixel Output Timing

QXGA Full Resolution Mode Line Timing

For the default QXGA line timing, a line starts when the HSYNC signal is de-asserted. The HSYNC signal will be low for 64 PCLK clock cycles. After 100 PCLK clock cycles, DOUT [9:0] will output ten cycles of dummy pixel data followed by 2048 cycles of image data and ten cycles of dummy pixel data. Another 32 cycles later, the HSYNC signal will be de-asserted to start a new line. See Figure 9.

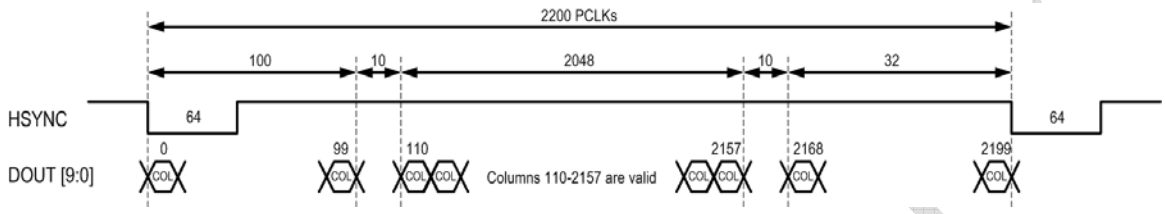

Figure 9. Default QXGA Line Timing for 2200 PCLKs

QXGA Full Resolution Mode Frame Timing

For the default QXGA frame timing, the timing unit for the frame is derived from one line-time unit, which is 2200 PCLKs. Frame timing starts when the VSYNC signal is de-asserted. The VSYNC signal will be low for three line-time units. Sixteen line-time units from the start of the frame, DOUT [9:0] will output ten lines of dummy pixel data, followed by 1536 lines of image data and another ten lines of dummy pixel data. 248 lines after the image pixel data, the VSYNC signal will be de-asserted again to start a new frame. See Figure 10.

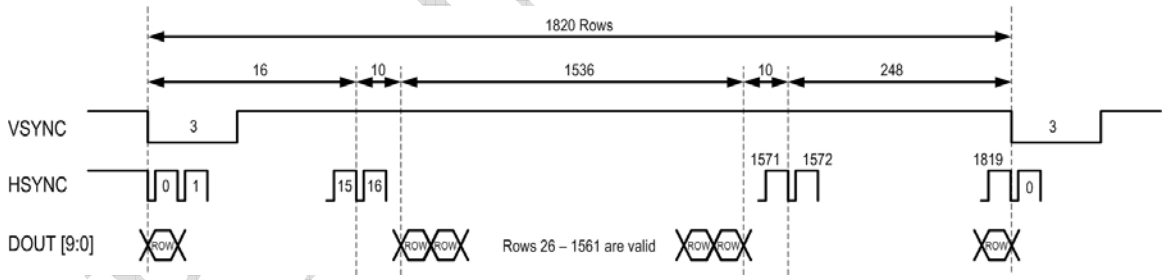

Figure 10. Default QXGA Frame Timing – Change Registers 0x4/0x15 to 0x0010 (H)

1/4-Rate Subsampling Mode Line Timing

For the default 1/4-rate (1024x768) line timing, a line starts when the HSYNC signal is de-asserted. The HSYNC signal will be low for 32 PCLK clock cycles. After 50 PCLK clock cycles, DOUT [9:0] will output five cycles of dummy pixel data, followed by 1024 cycles of image data and another five cycles of dummy pixel data. Sixteen cycles after the last dummy pixel data, the VSYNC signal will be de-asserted again to start a new line. See Figure 11.

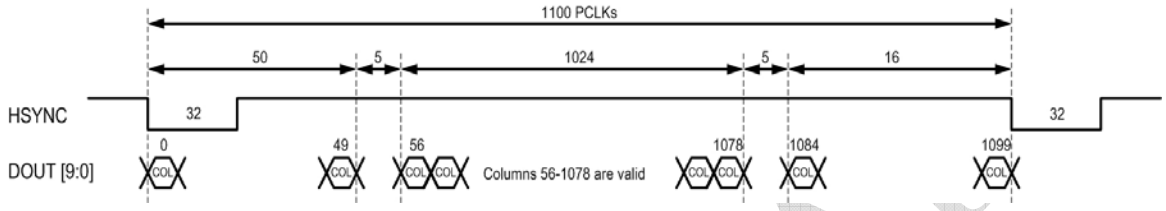

Figure 11. Default 1/4-Rate Line Timing for 1100 PCLKs

1/4-Rate Subsampling Mode Frame Timing

For the default 1/4-rate (1024x768)frame timing, the timing unit for the frame is derived from one line-time unit, which is 1100 PCLKs. The frame timing starts when the VSYNC signal is de-asserted. The VSYNC signal will be low for three line-time units. Eight line-time units from the start of the frame, DOUT [9:0] will output five lines of dummy pixel data, followed by 240 lines of image data and another five lines of dummy pixel data. Two lines after the last dummy pixel data, the VSYNC signal will be de-asserted again to start a new frame. See Figure 12.

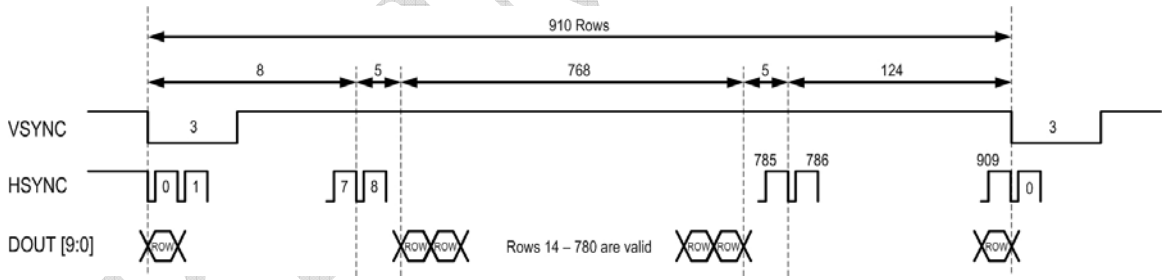

Figure 12. Default 1/4-Rate Frame Timing – Change Registers 0x14/0x15 to 0x0010 (H)

1/16-Rate Subsampling Mode LineTiming

For the default 1/16-rate (512x384) line timing, a line starts when the HSYNC signal is de-asserted. The HSYNC signal will be low for 16 PCLK clock cycles. After 25 PCLK clock cycles, DOUT [9:0] will output three cycles of dummy pixel data, followed by 512 cycles of image data and another three dummy pixel data. Seven clock cycles later, the HSYNC signal will be de-asserted to start a new line. See Figure 13.

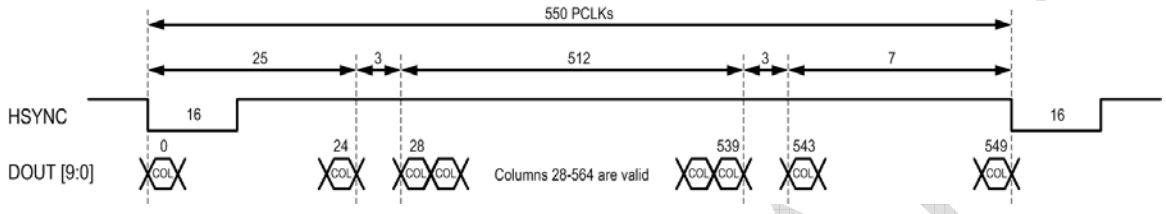

Figure 13. Default 1/16-Rate Line Timing for 570 PCLKs

1/16-Rate Subsampling Mode Frame Timing

For the default 1/16-rate (512x384) frame timing, the timing unit for the frame is derived from one line-time unit, which is 550 PCLKs. The frame timing starts when the VSYNC signal is de-asserted. The VSYNC signal will be low for three line-time units. Four line-time units from the start of the frame, DOUT [9:0] will output three lines of dummy pixel data followed by 384 lines of image data and another three lines of dummy pixel data. Eleven (11) clock cycles later, the VSYNC signal will be de-asserted again to start a new frame. See Figure 14.

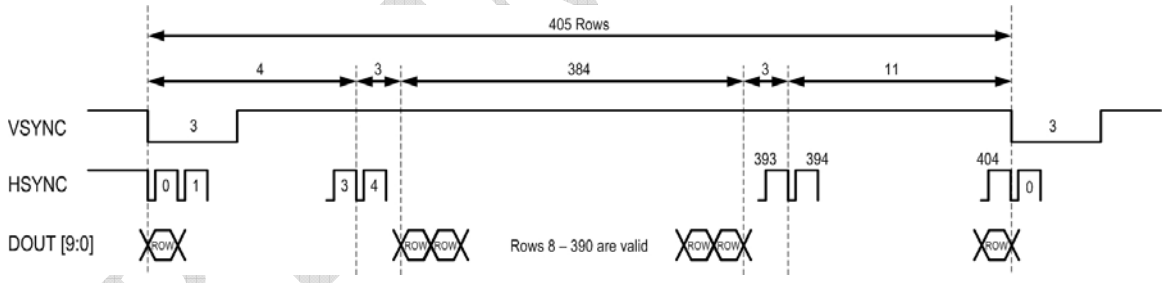

Figure 14. Default 1/16-Rate Frame Timing - Change Registers 0x14/0x15 to 0x0010 (H)

Mechanical Information

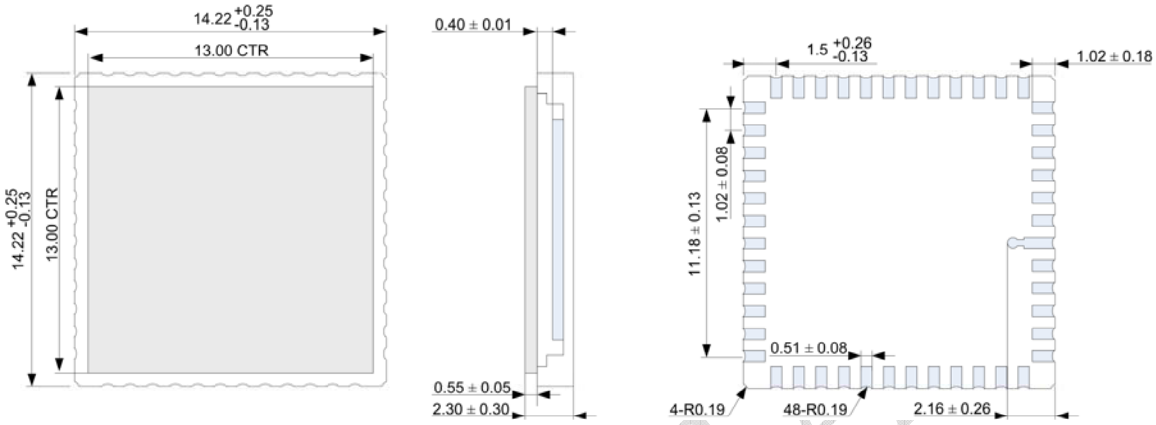

Figure 15. 48-pin CLCC14.22 Mechanical Drawing

Ordering Information

Table 6. Ordering Information

Description	Part Number
Bare die in wafer form – no grinding, wafer thickness of 740±25µm	ICM320TNAda
Bare die in wafer form – back grinding, wafer thickness of 300±12.5µm	ICM320TGAda
48-Pin CLCC14.22 package, (for evaluation only)	ICM320Tca

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