



GENERAL DESCRIPTION



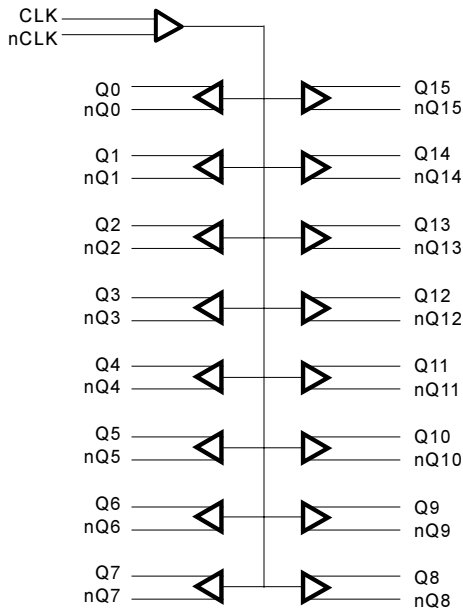
The ICS8501 is a low skew, 1-to-16 Differential Current Mode Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8501 is designed to translate any differential signal levels to small swing differential current mode(DCM) output levels. An external reference resistor is used to set the value of the current supplied to an external load load/termination resistor. The load resistor value is chosen to equal the value of the characteristic line impedance of 50Ω. The ICS8501 is characterized at an operating supply voltage of 3.3V.

The small swing outputs, accurate crossover voltage and duty cycle makes the ICS8501 ideal for interfacing to today's most advanced microprocessors.

FEATURES

- 16 small swing DCM outputs
- Translates any differential input signal(PECL, HSTL, LVDS, DCM) to DCM levels without external bias networks
- Translates single ended input levels to DCM levels with a resistor bias network on the nCLK input
- Translates single ended input levels to inverted DCM levels with a resistor bias network on the CLK input
- $V_{oh(max)} = 1.2V$
- $40\% \leq V_{crossover} \leq 60\% \text{ of } V_{oh}$
- $45\% \leq \text{Duty Cycle} \leq 55\%$
- Output frequency up to 500MHz
- 100ps output skew
- 3.3V operating supply
- 48 lead low-profile QFP(LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature

BLOCK DIAGRAM



PIN ASSIGNMENT

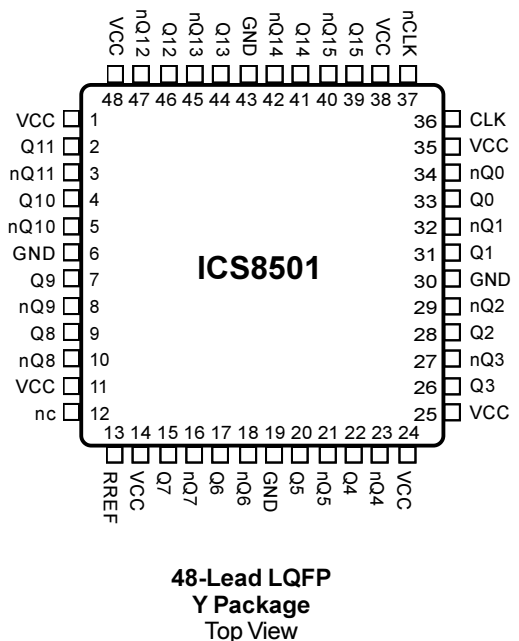




TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
1, 11, 14, 24, 25, 35, 38, 48	VCC	Power	Power supply pin. Connect to 3.3V.
2, 3	Q11, nQ11	Output	Differential output. Differential current mode interface levels.
4, 5	Q10, nQ10	Output	Differential output. Differential current mode interface levels.
6, 19, 30, 43	GND	Power	Power supply pin. Connect to ground.
7, 8	Q9, nQ9	Output	Differential output. Differential current mode interface levels.
9, 10	Q8, nQ8	Output	Differential output. Differential current mode interface levels.
12	nc	Unused	No connection.
13	RREF	Input	Reference current input. Used to set the output current. Connect to 475Ω resistor to ground.
15, 16	Q7, nQ7	Output	Differential output. Differential current mode interface levels.
17, 18	Q6, nQ6	Output	Differential output. Differential current mode interface levels.
20, 21	Q5, nQ5	Output	Differential output. Differential current mode interface levels.
22, 23	Q4, nQ4	Output	Differential output. Differential current mode interface levels.
26, 27	Q3, nQ3	Output	Differential output. Differential current mode interface levels.
28, 29	Q2, nQ2	Output	Differential output. Differential current mode interface levels.
36	CLK	Input	Non inverting differential clock input. Any differential input interface levels.
37	nCLK	Input	Inverting differential clock input. Any differential input interface levels.
39, 40	Q15, nQ15	Output	Differential output. Differential current mode interface levels.
41, 42	Q14, nQ14	Output	Differential output. Differential current mode interface levels.
44, 45	Q13, nQ13	Output	Differential output. Differential current mode interface levels.
46, 47	Q12, nQ12	Output	Differential output. Differential current mode interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance			2		pF
CPD	Power Dissipation Capacitance (per output)	VCC = 3.465V, f=250MHz		4.6		pF
ROUT	Output Impedance			14		KΩ

TABLE 3. FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0 thru Q15	nQ0 thru nQ15		
0	1	0	1	Differential to Differential	Non Inverting
1	0	1	0	Differential to Differential	Non Inverting
0	Biased; NOTE 1	0	1	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	1	0	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	1	0	Single Ended to Differential	Inverting
Biased; NOTE 1	1	0	1	Single Ended to Differential	Inverting

NOTE 1: Single ended use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS and LVTTTL levels the recommended input bias network is a resistor to VCC, a resistor of equal value to ground and a 0.1μF capacitor from the input to ground. The resulting switch point is approximately VCC/2 ± 300mV.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VCC+0.5 V
Outputs	-0.5V to VCC+0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any conditions beyond those listed in the *DC Electrical Characteristics* or *AC Electrical Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4. DC ELECTRICAL CHARACTERISTICS, VCC = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VCC	Operating Supply Voltage		3.135	3.3	3.465	V
VPP	Peak-to-Peak Input Voltage		0.31		1.3	V
VCMR	Common Mode Input Voltage; NOTE 1	LVPECL Levels	1.8		2.4	V
		DCM, HSTL, LVDS, SSTL Levels	0.31		1.3	V
I _{IH}	Input High Current	CLK, nCLK VIN = VCC			5	µA
I _{IL}	Input Low Current	CLK, nCLK VIN = 0V	-5			µA
ICC	Operating Supply Current				70	mA
IOH	Output Current; NOTE 2	3.135V ≤ VCC ≤ 3.465V	11	14	17	mA
VOH	Output High Voltage	RREF = 475Ω, RLOAD = 50Ω	0.6	0.71	1.2	V
VOL	Output Low Voltage	RREF = 475Ω, RLOAD = 50Ω		0	0.05	V

NOTE 1: Common mode input voltage for LVPECL is defined as the minimum VIH. The LVPECL values noted in Table 4A are for VCC = 3.3V. VCMR for LVPECL will vary 1:1 with VCC. Common mode input voltage for DCM, HSTL, LVDS and SSTL is defined as the crossover voltage. See Figure 1A and 1B.

NOTE 2: IOH is the current per output being supplied to the load and should be included in the total supply current calculation. Therefore ICC(total) is equal to IOH times 16 plus ICC.

TABLE 5. AC ELECTRICAL CHARACTERISTICS, VCC = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f _{MAX}	Maximum Input Frequency	Measured at the -3dB rolloff of the peak-to-peak output voltage			500	MHz
tp _{LH}	Propagation Delay, Low-to-High	0 < f ≤ 250MHz	2		3	ns
tp _{HL}	Propagation Delay, High-to-Low	0 < f ≤ 250MHz	2		3	ns
tsk(o)	Output Skew; NOTE 3	Measured on at VOX			100	ps
tsk(pp)	Part-to-Part Skew; NOTE 4	Measured on at VOX			650	ps
t _R	Output Rise Time	20% to 80%	175		700	ps
t _F	Output Fall Time	20% to 80%	175		700	ps
t _{PW}	Output Pulse Width		t _{CYCLE} /2 - 0.3	t _{CYCLE} /2	t _{CYCLE} /2 + 0.3	ns
VOX	Output Crossover Voltage		40% VOH		60% VOH	V

NOTE 1: All parameters measured at 250MHz unless noted otherwise.

NOTE 2: RREF equals 475Ω. Outputs terminated with 50Ω resistor connected to ground.

NOTE 3: Defined as skew across outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.



FIGURE 1A, 1B, 1C - INPUT CLOCK WAVEFORMS

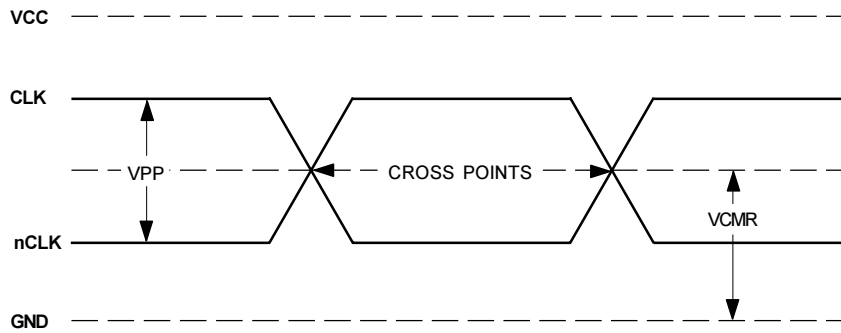


FIGURE 1A - DCM, LVDS, HSTL, SSTL DIFFERENTIAL INPUT LEVELS

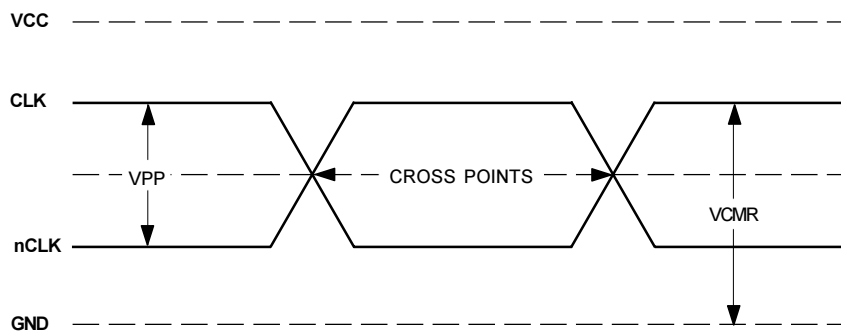


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

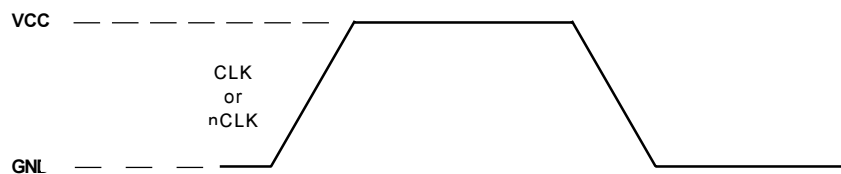


FIGURE 1C - LVCMOS AND LVTTTL SINGLE ENDED INPUT LEVEL



FIGURE 2A - TIMING WAVEFORMS

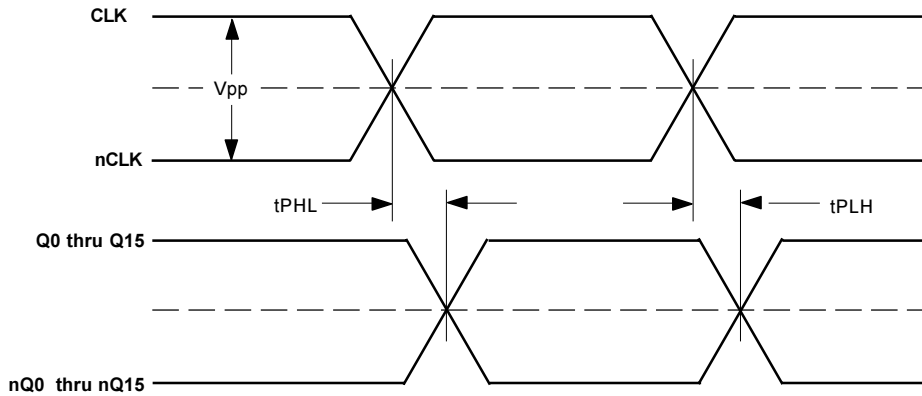


FIGURE 3A - PROPAGATION DELAYS
 $f_{in} = 250\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 200\text{ps}$

FIGURE 3A - OUTPUT SKEW DEFINITION & WAVEFORMS

Output Skew - Skew between any outputs. Outputs operating at the same temperature, supply voltages and with equal load conditions.

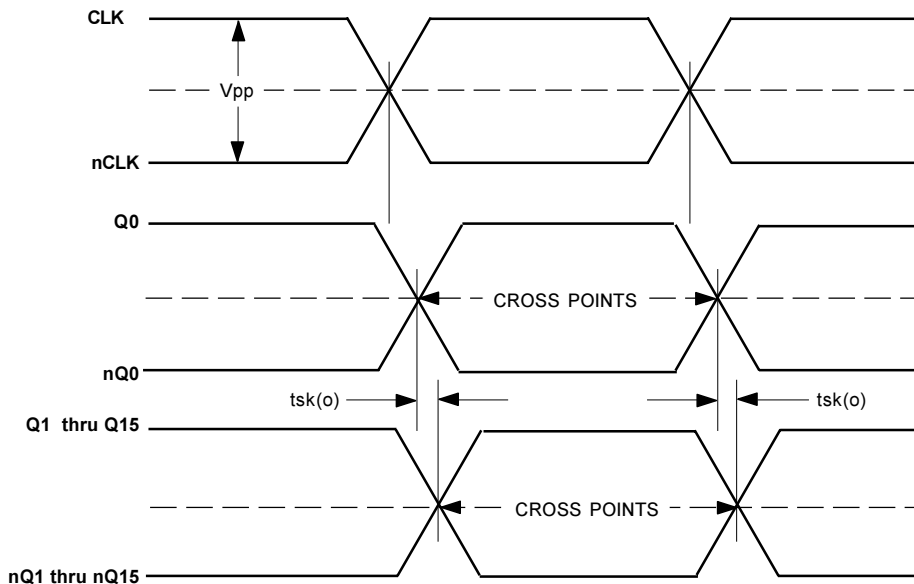


FIGURE 3A - OUTPUT SKEW
 $f_{in} = 250\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 200\text{ps}$



FIGURE 3B - PART-TO-PART SKEW DEFINITION & WAVEFORMS

Part-to-Part Skew - Skew between any outputs on different parts. Outputs operating at the same temperature, supply voltages and with equal load conditions.

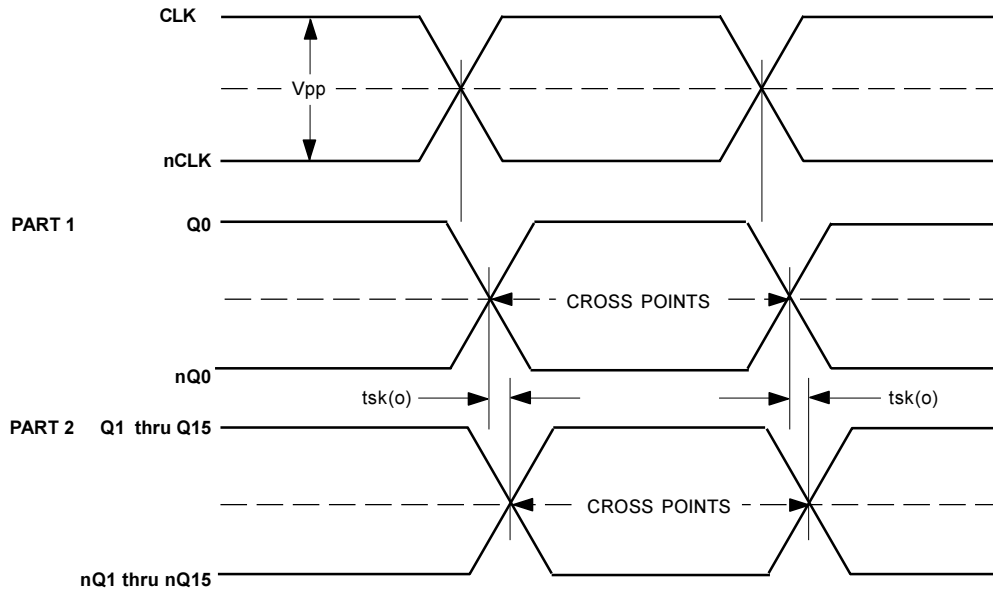
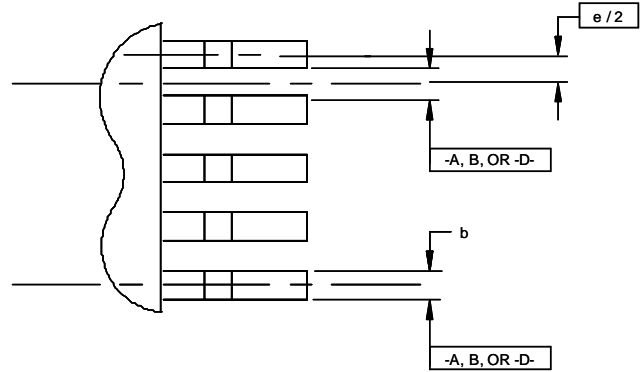
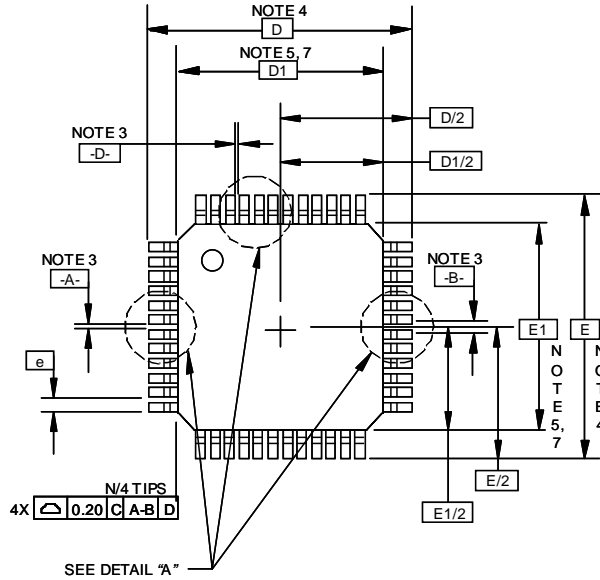


FIGURE 3B - PART-TO-PART SKEW

$f_{in} = 250\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 200\text{ps}$

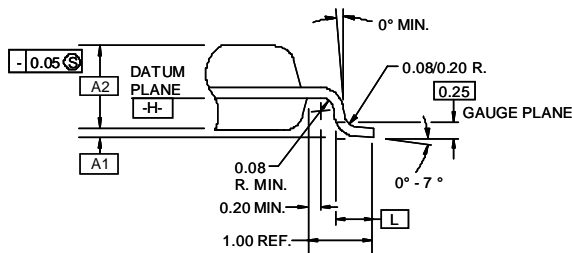
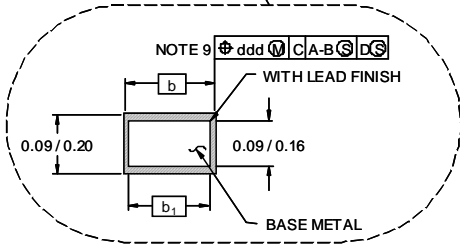
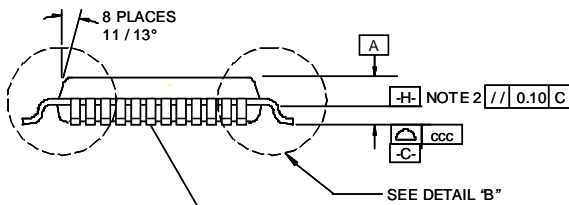


PACKAGE OUTLINE AND DIMENSIONS - Y SUFFIX



NOTES:

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS -A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC AT DATUM PLANE -H-.
4. TO BE DETERMINED AT SEATING PLACE -C-.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
6. "N" IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-.
8. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
10. CONTROLLING DIMENSION: MILLIMETER.
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-026, VARIATION BBC.
12. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE.



SYMBOL	JEDEC VARIATION			NOTE
	ALL DIMENSIONS IN MILLIMETERS			
	BBC			
	MIN.	NOM.	MAX.	
A			1.60	12
A ₁	0.05		0.15	
A ₂	1.35	1.40	1.45	
D	9.00 BSC.			4
D ₁	7.00 BSC.			7, 8
E	9.00 BSC.			4
E ₁	7.00 BSC.			7, 8
L	0.45	0.60	0.75	9
N	48			
e	0.5 BSC.			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	



**Integrated
Circuit
Systems, Inc.**

ICS8501

LOW SKEW 1-TO-16 DIFFERENTIAL CURRENT MODE FANOUT BUFFER

ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8501BY	ICS8501BY	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8501BYT	ICS8501BY	48 Lead LQFP on Tape and Reel	2000	0°C to 70°C

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