

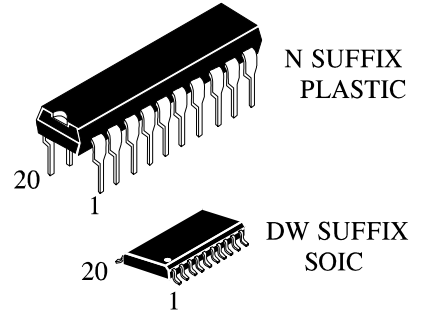
IN74ACT534

OCTAL 3-STATE INVERTING D FLIP-FLOP High-Speed Silicon-Gate CMOS

The IN74ACT534 is identical in pinout to the LS/ALS534, HC/HCT534. The IN74ACT534 may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

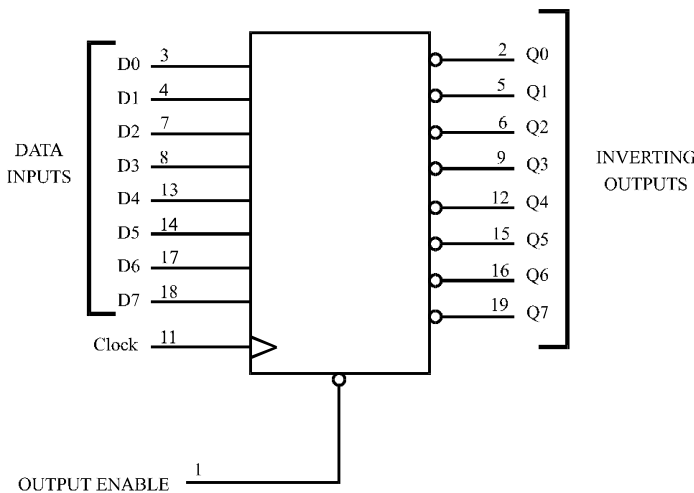
Data meeting the setup time is clocked, in inverted form, to the outputs with the rising edge of the Clock. The Output Enable input does not affect the states of the flip-flops, but when Output Enable is high, the outputs are forced to the high impedance state. Thus, data may be stored even when the outputs are not enabled.

- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A; 0.1 μ A @ 25°C
- Outputs Source/Sink 24 mA



ORDERING INFORMATION
 IN74ACT534N Plastic
 IN74ACT534DW SOIC
 $T_A = -40^\circ$ to 85° C for all packages

LOGIC DIAGRAM



PIN ASSIGNMENT

| | | | |
|---------------|-----|----|----------|
| OUTPUT ENABLE | 1 ● | 20 | V_{CC} |
| Q0 | 2 | 19 | Q7 |
| D0 | 3 | 18 | D7 |
| D1 | 4 | 17 | D6 |
| Q1 | 5 | 16 | Q6 |
| Q2 | 6 | 15 | Q5 |
| D2 | 7 | 14 | D5 |
| D3 | 8 | 13 | D4 |
| Q3 | 9 | 12 | Q4 |
| GND | 10 | 11 | CLOCK |

FUNCTION TABLE

| Inputs | | Output | |
|---------------|-------|--------|-----------|
| Output Enable | Clock | D | Q |
| L | | H | L |
| L | | L | H |
| L | L,H, | X | no change |
| H | X | X | Z |

X = don't care
 Z = high impedance

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MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|------------------------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| V_{OUT} | DC Output Voltage (Referenced to GND) | -0.5 to $V_{CC} + 0.5$ | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Sink/Source Current, per Pin | ± 50 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP+ SOIC Package+ | 750 500 | mW |
| Tstg | Storage Temperature | -65 to +150 | $^{\circ}C$ |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) | 260 | $^{\circ}C$ |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

+Derating - Plastic DIP: - 10 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

SOIC Package: - 7 mW/ $^{\circ}C$ from 65 $^{\circ}$ to 125 $^{\circ}C$

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|---|--|----------------|-------------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{IN}, V_{OUT} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_J | Junction Temperature (PDIP) | | 140 | $^{\circ}C$ |
| T_A | Operating Temperature, All Package Types | -40 | +85 | $^{\circ}C$ |
| I_{OH} | Output Current - High | | -24 | mA |
| I_{OL} | Output Current - Low | | 24 | mA |
| t_r, t_f | Input Rise and Fall Time * (except Schmitt Inputs) | $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 5.5 \text{ V}$ | 0 10 8.0 | ns/V |

* V_{IN} from 0.8 V to 2.0 V

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V _{CC} V | Guaranteed Limits | | Unit |
|--------------------|--|---|--|-------------------|---------------|------|
| | | | | 25 °C | -40°C to 85°C | |
| V _{IH} | Minimum High-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} -0.1 V | 4.5 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage | V _{OUT} = 0.1 V or V _{CC} -0.1 V | 4.5 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | |
| V _{OH} | Minimum High-Level Output Voltage | I _{OUT} ≤ -50 μA | 4.5 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | |
| | | | *V _{IN} =V _{IH} or V _{IL} I _{OH} =-24 mA I _{OH} =-24 mA | 4.5 | 3.86 | |
| | | | 5.5 | 4.86 | 4.76 | |
| V _{OL} | Maximum Low-Level Output Voltage | I _{OUT} ≤ 50 μA | 4.5 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | |
| | | | *V _{IN} = V _{IH} or V _{IL} I _{OL} =24 mA I _{OL} =24 mA | 4.5 | 0.36 | |
| | | | 5.5 | 0.36 | 0.44 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} =V _{CC} or GND | 5.5 | ±0.1 | ±1.0 | μA |
| ΔI _{CC} T | Additional Max. I _{CC} /Input | V _{IN} =V _{CC} - 2.1 V | 5.5 | | 1.5 | mA |
| I _{OZ} | Maximum Three-State Leakage Current | V _{IN} (OE)= V _{IH} or V _{IL} V _{IN} =V _{CC} or GND V _{OUT} =V _{CC} or GND | 5.5 | ±0.5 | ±5.0 | μA |
| I _{OLD} | +Minimum Dynamic Output Current | V _{OLD} =1.65 V Max | 5.5 | | 75 | mA |
| I _{OHD} | +Minimum Dynamic Output Current | V _{OHD} =3.85 V Min | 5.5 | | -75 | mA |
| I _{CC} | Maximum Quiescent Supply Current (per Package) | V _{IN} =V _{CC} or GND | 5.5 | 8.0 | 80 | μA |

* All outputs loaded; thresholds on input associated with output under test.

+Maximum test duration 2.0 ms, one output loaded at a time.

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AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | | | Unit |
|-----------|--|-------------------|------|---------------|------|------|
| | | 25 °C | | -40°C to 85°C | | |
| | | Min | Max | Min | Max | |
| f_{max} | Maximum Clock Frequency (Figure 1) | | | 120 | | ns |
| t_{PLH} | Propagation Delay, Clock to Q (Figure 1) | 2.5 | 11.5 | 2.0 | 12.5 | ns |
| t_{PHL} | Propagation Delay, Clock to Q (Figure 1) | 2.0 | 10.5 | 2.0 | 12.0 | ns |
| t_{PZH} | Propagation Delay, Output Enable to Q (Figure 2) | 2.5 | 12.0 | 2.0 | 12.5 | ns |
| t_{PZL} | Propagation Delay, Output Enable to Q (Figure 2) | 2.0 | 11.0 | 2.0 | 11.5 | ns |
| t_{PHZ} | Propagation Delay, Output Enable to Q (Figure 2) | 1.5 | 12.5 | 1.0 | 13.5 | ns |
| t_{PLZ} | Propagation Delay, Output Enable to Q (Figure 2) | 1.5 | 10.5 | 1.0 | 10.5 | ns |
| C_{IN} | Maximum Input Capacitance | 4.5 | | 4.5 | | pF |

| | | | | |
|----------|-------------------------------|--------------------------------------|--|----|
| C_{PD} | Power Dissipation Capacitance | Typical @25°C, $V_{CC}=5.0\text{ V}$ | | pF |
| | | 40 | | |

TIMING REQUIREMENTS ($V_{CC}=5.0\text{ V} \pm 10\%$, $C_L=50\text{pF}$, Input $t_r=t_f=3.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limits | | Unit |
|----------|--|-------------------|---------------|------|
| | | 25 °C | -40°C to 85°C | |
| t_{su} | Minimum Setup Time, Data to Clock (Figure 3) | 3.5 | 4.0 | ns |
| t_h | Minimum Hold Time, Clock to Data (Figure 3) | 1.0 | 1.5 | ns |
| t_w | Minimum Pulse Width, Clock (Figure 1) | 3.5 | 3.5 | ns |

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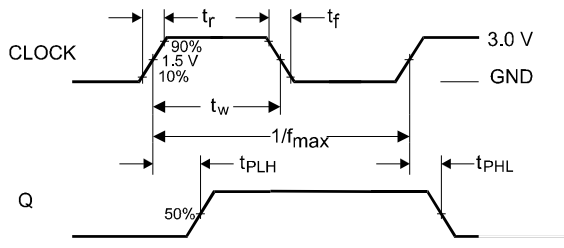


Figure 1. Switching Waveforms

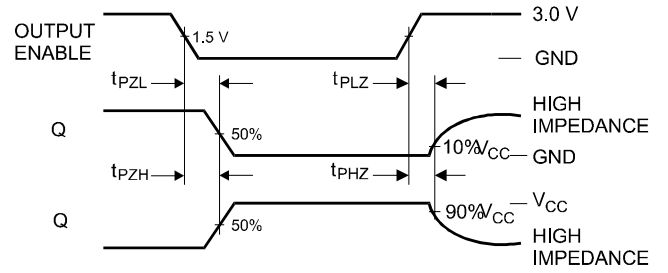


Figure 2. Switching Waveforms

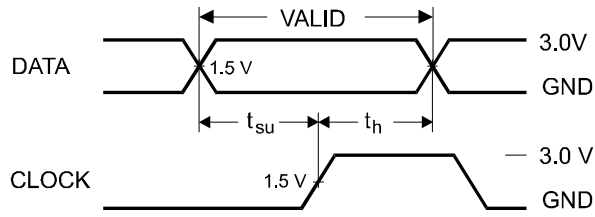


Figure 3. Switching Waveforms

EXPANDED LOGIC DIAGRAM

