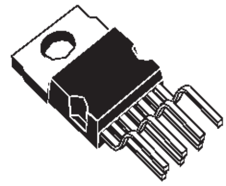
L4937N

DUAL MULTIFUNCTION VOLTAGE REGULATOR

- STANDBY OUTPUT VOLTAGE PRECISION 5V ± 2%
- OUTPUT 2 TRACKED TO THE STANDBY OUTPUT
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE
- VERY LOW QUIESCENT CURRENT, LESS THAN 250μA, IN STANDBY MODE
- OUTPUT CURRENTS : I_{01} = 50mA, I_{02} = 500mA
- VERY LOW DROPOUT (max 0.4V/0.6V)
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- POWER-ON RESET CIRCUIT SENSING THE STANDBY OUTPUT VOLTAGE
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- THERMAL SHUTDOWN AND SHORT CIRCUIT PROTECTIONS



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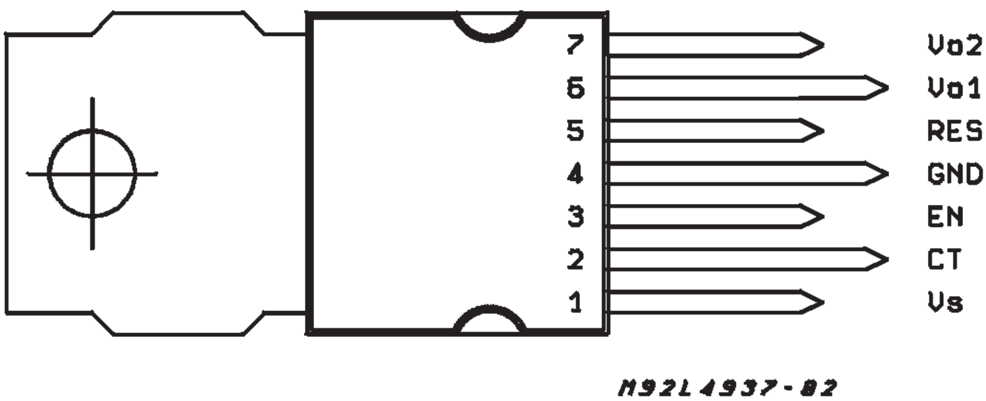
ORDERING NUMBER : L4937N

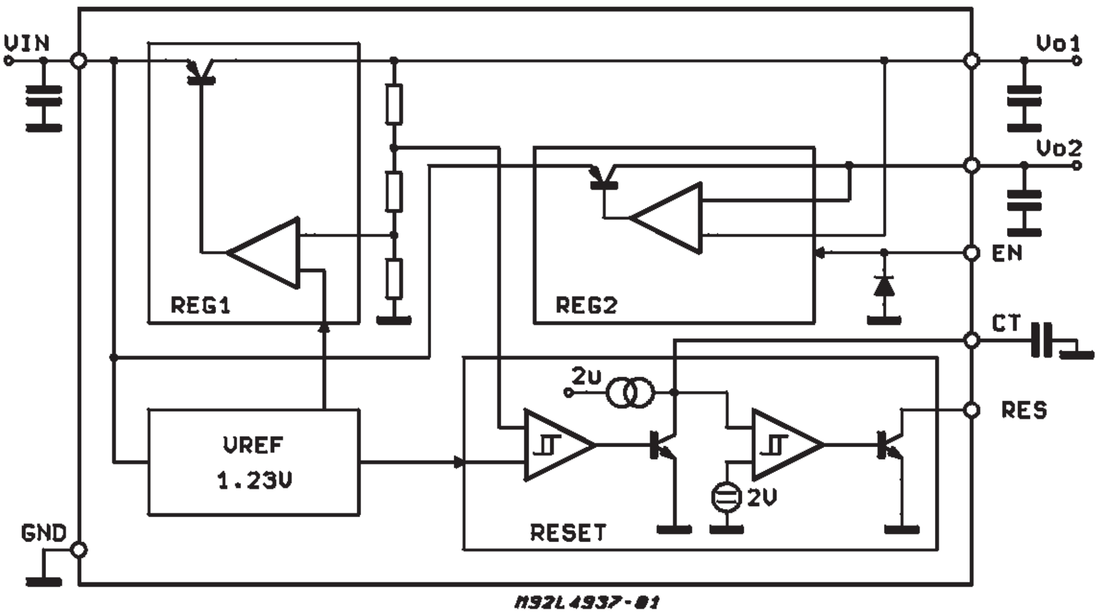
DESCRIPTION

The L4937N is a monolithic integrated dual voltage regulators with two very low dropout outputs and additional functions such as power-on reset and input voltage sense. It is designed for supplying microcomputer controlled systems specially in automotive applications.

PIN CONNECTION (top view)



BLOCK DIAGRAM



THERMAL DATA

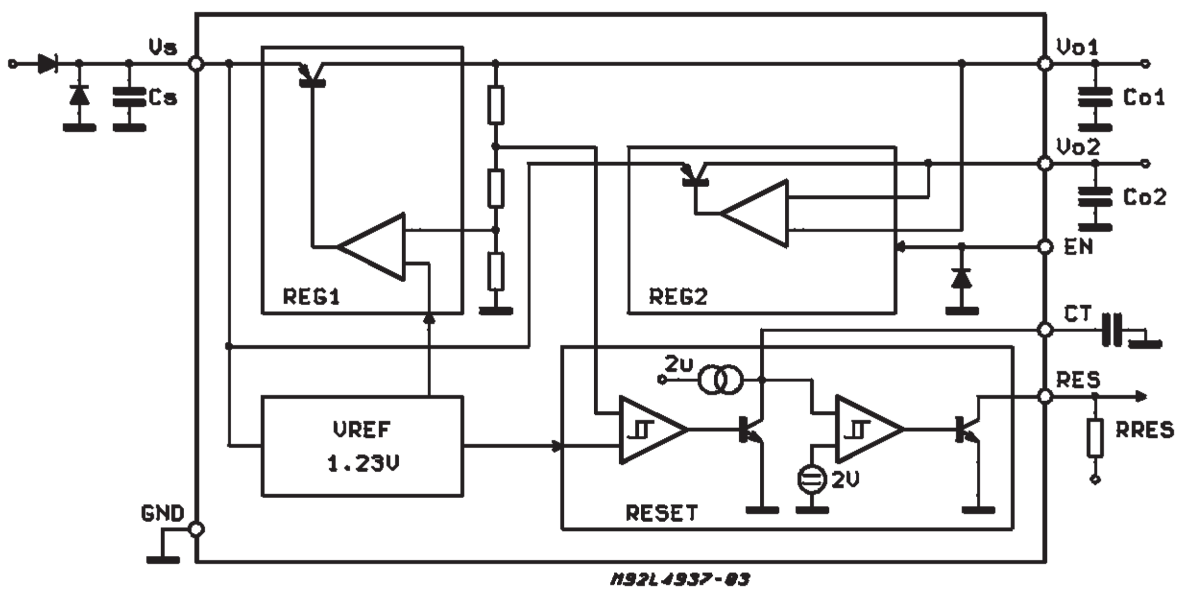
Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case Max.	3	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	28	V
	Transient Supply Voltage (T < 1s)	40	V
T_j, T_{stg}	Junction and Storage Temperature Range	–55 to 150	°C
I_{EN}	Enable Input Current ($V_{EN} \leq 0.3V$)	± 1	mA
V_{EN}	Enable Input Voltage	V_S	
V_{RES}	Reset Output Voltage	20	V
I_{RES}	Reset Output Current	5	mA
P_D	Power Dissipation (T_A = 80°C, $R_{th\ heatsink}$ = 9°C/W)	5	W

Note : The circuit is ESD protected according to MIL–STD–883C.

APPLICATION CIRCUIT



$C_S \geq 1\mu F$; $C_{01} \geq 6\mu F$; $C_{02} \geq 10\mu F$, ESR < 10Ω at 10KHz

ELECTRICAL CHARACTERISTICS (V_S = 14V; –40°C ≤ T_j ≤ 125°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage				25	V
V_{O1}	Standby Output Voltage	6V ≤ V_S ≤ 25V 1mA ≤ I_{O1} ≤ 50mA	4.90	5.00	5.10	V
V_{O2} - V_{O1}	Output Voltage 2 Tracking Error (note 1)	6V ≤ V_S ≤ 25V 5mA ≤ I_{O2} ≤ 500mA Enable = LOW	–25		+25	mV
V_{DP1}	Dropout Voltage 1	I_{O1} = 10mA I_{O1} = 50mA		0.1 0.2	0.25 0.4	V V
V_{IO1}	Input to Output Voltage Difference in Undervoltage Condition	VS = 4V, I_{O1} = 35mA			0.4	V
V_{DP2}	Dropout Voltage 2	IO2 = 100mA I_{O2} = 500mA		0.2 0.3	0.3 0.6	V V
V_{IO2}	Input to Output Voltage Difference in Undervoltage Condition	VS = 4.6V, I_{O2} = 350mA			0.6	V
$V_{OL\,1.2}$	Line Regulation	6V ≤ V_S ≤ 25V I_{O1} = 1mA; I_{O2} = 5mA			20	mV
V_{OLO1}	Load Regulation 1	1mA ≤ I_{O1} ≤ 50mA			25	mV
V_{OLO2}	Load Regulation 2	5mA ≤ I_{O2} ≤ 500mA			50	mV
I_{LIM1}	Current Limit 1	V_{O1} = 4.5V V_{O1} = 0V (note 2)	55 25	100 50	200 100	mA mA
I_{LIM2}	Current Limit 2	VO2 = 0V	550	1000	1700	mA
I_{QSB}	Quiescent Current Standby Mode (output 2 disabled)	I_{O1} = 0.3mA; T_J < 100°C V_{EN} ≥ 2.4V V_S = 14V V_S = 3.5V		210 340	290 850	µA µA
I_Q	Quiescent Current	I_{O1} = 50mA I_{O1} = 500mA			30	mA

ENABLE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{ENL}	Enable Input LOW Voltage (output 2 active)		–0.3		1.5	V
V_{ENH}	Enable Input HIGH Voltage		2.4		7	V
V_{ENhyst}	Enable Hysteresis		30	75	200	mV
I_{EN}	Enable Input Current	0V < V_{EN} < 1.2V 2.5V < V_{EN} < 7V	–10 –1	–1.5 0	–0.5 +1	µA µA

ELECTRICAL CHARACTERISTICS (continued)

RESET

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{Rt}	Reset Low Threshold Voltage	V_S = 14V	V_{o1} -0.4	4.7	V_{o1} -0.1	V
V_{Rth}	Reset Threshold Hysteresis		50	100	200	mV
t_{RD}	Reset Pulse Delay	C_T = 100nF; t_R > 100µs	55	100	180	ms
t_{RR}	Reset Reaction Time	C_T = 100nF	1	10	50	µs
V_{RL}	Reset Output LOW Voltage	R_{RES} = 10KΩ to V_{01} $V_S \geq$ 1.5V			0.4	V
I_{LRES}	Reset Output HIGH Leakage	V_{RES} = 5V			1	µA
V_{CTth}	Delay Comparator Threshold			2.0		V
$V_{CTth, hyst}$	Delay Comparator Threshold Hysteresis			100		mV

Note : 1 : V_{O2} connected to ADJ.V_{O2} can be set to higher values by inserting an external resistor divider.
2 : Foldback characteristic

FUNCTIONAL DESCRIPTION

The L4937N is based on the SGS-THOMSON Microelectronics modular voltage regulator approach. Several out-standing features and auxiliary functions are provided to meet the requirements of supplying the microprocessor systems used in automotive applications.

Furthermore the device is suitable also in other applications requiring two stabilized voltages.

The modular approach allows other features and functions to be realized easily when required.

STANDBY REGULATOR

The standby regulator uses an Isolated Collector Vertical PNP transistor as the regulating element. This structure allows a very low dropout voltage at currents up to 50mA. The dropout operation of the standby regulator is maintained down to 2V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. This feature avoids functional interruptions which could be generated by overvoltage pulses.

The typical curve of the standby output voltage as a function of the input supply voltage is shown in fig. 1.

The current consumption of the device (quiescent current) is less than 250µA when output 2 is disabled (standby mode). The dropout voltage is controlled to reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region.

The quiescent current is shown in fig. 2 as a function of the supply input voltage 2.

OUTPUT 2 VOLTAGE

The output 2 regulator uses the same output structure as the standby regulator, but rated for an output current of 500mA.

The output 2 regulator works in tracking mode with the standby output voltage as a reference voltage.

The output 2 regulator can be switched off via the Enable input.

Figure 1 : Output Voltage vs. Input Voltage.

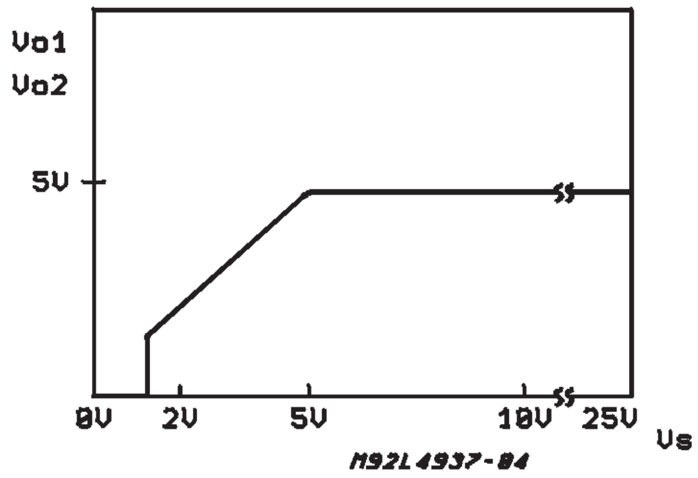
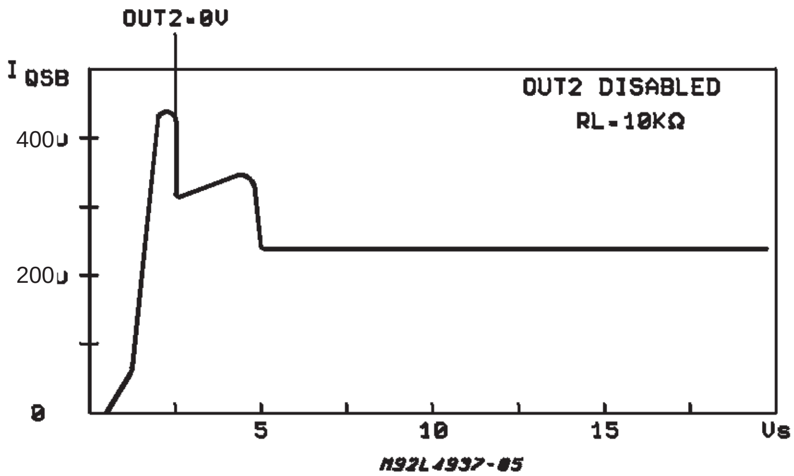


Figure 2 : Quiescent Current vs. Supply Voltage.



RESET CIRCUIT

The block circuit diagram of the reset circuit is shown in fig. 3. The reset circuit supervises the standby output voltage. The reset threshold of 4.7V is defined by the internal reference voltage and the standby output divider.

The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_T :

$$t_{RD} = \frac{C_T \times 2V}{2\mu A}$$

The reaction time of the reset circuit depends on the discharge time limitation of the reset capacitor C_T and is proportional to the value of C_T.

The reaction time of the reset circuit increases the noise immunity. In fact, if the standby output voltage drops below the reset threshold for a time shorter than the reaction time t_{RR}, no reset output variation occurs. The nominal reset delay is generated for standby output voltage drops longer than the time necessary for the complete discharging of the capacitor C_T. This time is typically equal to 50µs if C_T = 100nF. The typical reset output waveforms are shown in fig.

Figure 3 : Block Diagram of the Reset Circuit.

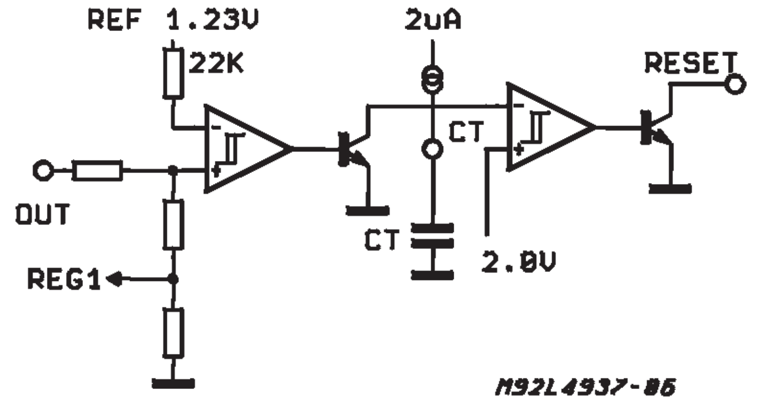
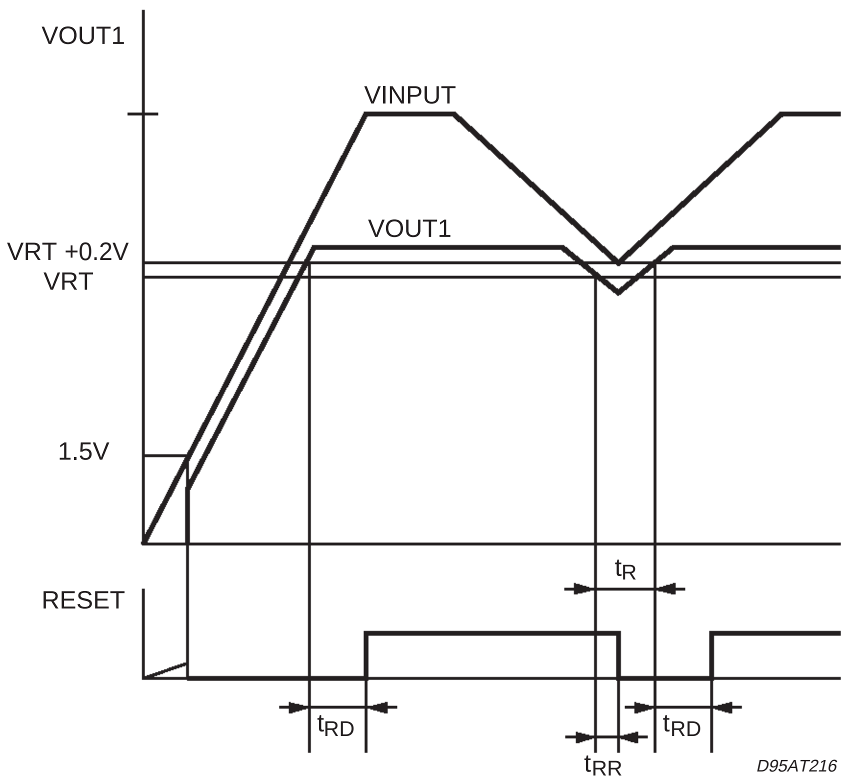
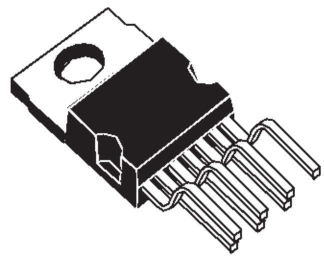


Figure 4 : Typical Reset Output Waveforms.



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
E1	0.7		0.97	0.028		0.038
F	0.6		0.8	0.024		0.031
F1			0.9			0.035
G	2.34	2.54	2.74	0.095	0.100	0.105
G1	4.88	5.08	5.28	0.193	0.200	0.205
G2	7.42	7.62	7.82	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L	16.7	16.9	17.1	0.657	0.668	0.673
L1		14.92			0.587	
L2	21.24	21.54	21.84	0.386	0.848	0.860
L3	22.27	22.52	22.77	0.877	0.891	0.896
L4			1.29			0.051
L5	2.6	2.8	3	0.102	0.110	0.118
L6	15.1	15.5	15.8	0.594	0.610	0.622
L7	6	6.35	6.6	0.236	0.250	0.260
L9		0.2			0.008	
M	2.55	2.8	3.05	0.100	0.110	0.120
M1	4.83	5.08	5.33	0.190	0.200	0.210
V4	40° (typ.)					
Dia	3.65		3.85	0.144		0.152

OUTLINE AND MECHANICAL DATA



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