



Dolby Pro Logic Surround Decoder



Overview

The LV1050M is a Dolby Pro Logic surround effect signal-processing Bi-CMOS IC that in addition to LV1018 and LA2787 function, realizes virtual surround processing with the use of 5.1ch input signal. This IC can implement a Dolby Pro Logic surround system and various digital surround system in just one chip.

Functions and Features

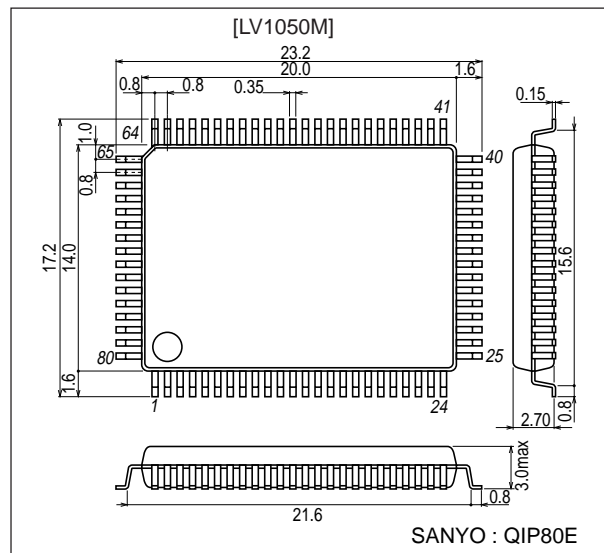
- Adaptive matrix.
- Center mode control (Normal/Phantom/Wide).
- 4ch/3ch logic control.
- Auto balance (ON/OFF).
- Prologic off-mode (Bypass/Full Bypass).
- On-chip memory (8k bit S-RAM).
- Variable delay time.
 - Dolby surround mode : 15, 20, 25, or 30ms.
 - Simulated surround mode: 7.5, 15, 20, 25, 30, 40 or 50ms.
- Modified B type noise-reduction.
- Center trim, surround trim (LS-ch, RS-ch) and LFE trim (0 to -31dB in -1dB steps).
- Input and output filter.
 - Output : 7kHz L.P.F in dolby surround mode.
 - 5kHz L.P.F in simulated surround mode.
- Built-in VDD.
- Simulated surround function.
 - Fixed matrix : L+R, L-R.
 - Front addition : 0, -2, -4 and -6 dB inverted and non inverted addition.
 - Reverb function.
- Rear-channel monaural/stereo switching.
 - Rear addition : 0, -2, -4 and -6 dB inverted and noninverted addition .

- Pseudo-tap function.
- Built-in input switch for the L, C, R, LS, RS, and LFE channels.
- Virtual surround function (VDS 2 modes, VDD 1 mode).
- Simulated surround function for Dolby Digital.
- Input and output muting function.
- Reference level : 300 mVrms.
- Operating supply voltage : 8 to 10V.
- Package : QIP80E.

Note : Dolby and Double D Symbol are registered trademarks of Dolby Laboratories Licensing Corporation. This IC is available only to licensees of Dolby Laboratories Licensing Corporation. San Francisco, C94103-4813, USA, from whom licensing and application information must be obtained.

Package Dimensions

unit : mm
3174-QIP80E



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LV1050M

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	VCC max		10.5	V
Allowable power dissipation	Pd max	Ta ≤ 70°C *with board	1400	mW
Operating temperature	Topr		-20 to +70	°C
Storage temperature	Tstg		-40 to +150	°C

Note : *When mounted on a 114.3 mm X 76.1 mm, t = 1.6 mm fiberglass epoxy printed circuit board.

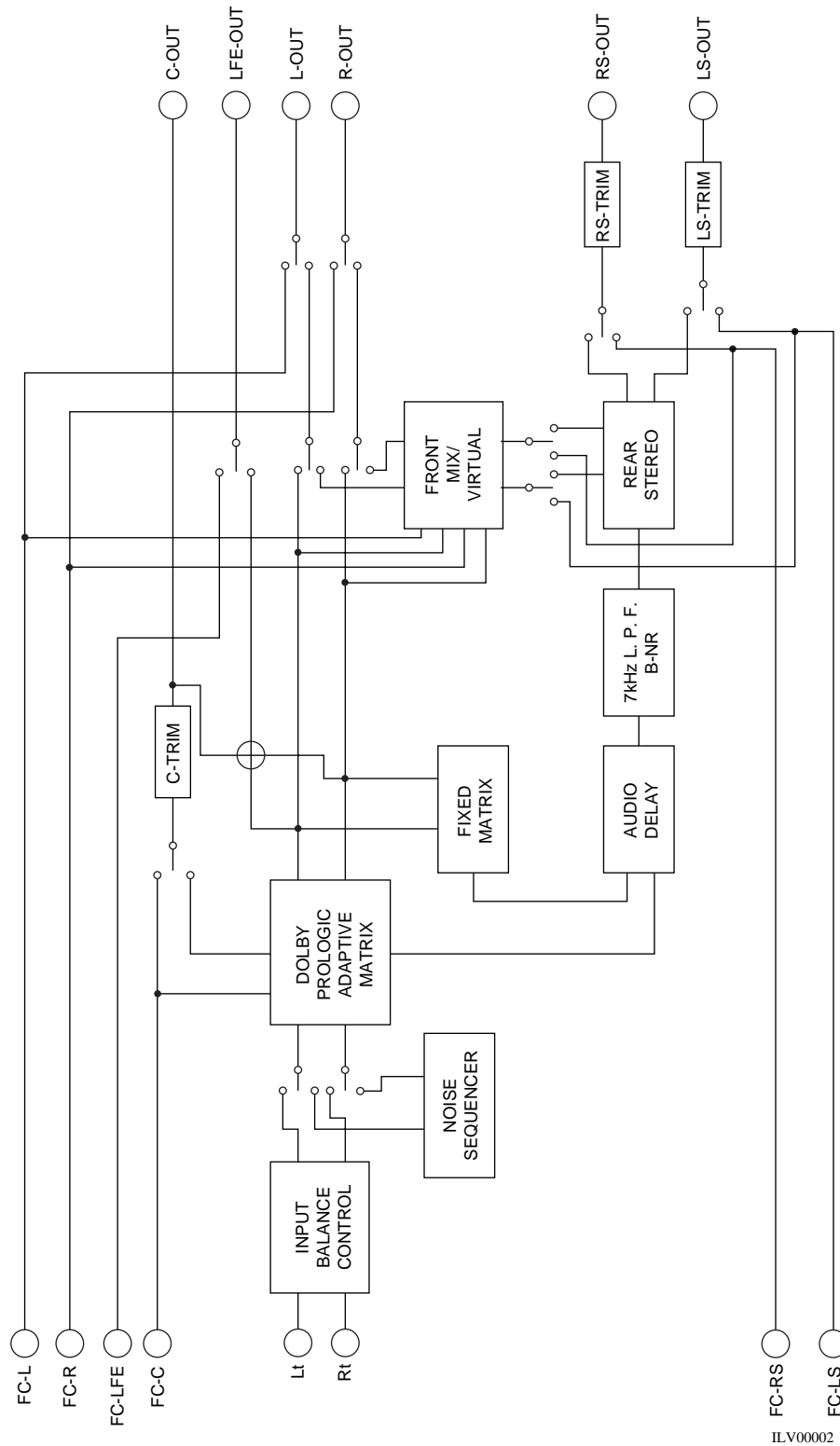
Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	VCC		9	V
Operating supply voltage range	VCCopg		8 to 10	V
Control input high level			3.5 to 5.5	V
Control input low level			0 to 1.5	V
Dolby level	VO Dolby		300	mVrms

Electrical Characteristics at Ta = 25°C, VCC = 9 V, f = 1 kHz, VIN = 300 mV (L, R inputs), VIN = 212 mV (C,S inputs), center and surround trim = 0 dB. Unless otherwise specified : in pro logic on mode and with the 400 Hz to 30 kHz bandpass filter used.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	ICC			120	135	mA
Cch output level	VOC		-2	0	2	dB
Output level deviation (Reference to the center output)	VOA		-0.5	0	0.5	dB
Lch matrix rejection	Rj, L		25	35		dB
Cch matrix rejection	Rj, C		25	35		dB
Rch matrix rejection	Rj, R		25	35		dB
Sch matrix rejection	Rj, LS, RS		25	35		dB
Total harmonic distortion L, R, C	THD			0.02	0.05	%
Total harmonic distortion S	THD			0.1	0.7	%
S/N Lch	S/N, L	CCIR/ARM, Rg = 10 kΩ	65	76		dB
S/N Cch	S/N, C		65	77		dB
S/N Rch	S/N, R		65	76		dB
S/N Sch	S/N, LS,RS		60	72		dB
Lch signal handling	SH, L	VCC = 8.5 V, f = 1 kHz, THD = 1% (L,C,R), THD = 3% (LS, RS)	15	16		dB
Cch signal handling	SH, C		15	18		dB
Rch signal handling	SH, R		15	16		dB
Sch signal handling	SH, LS, RS		15	16		dB
Noise sequencer output	VN		50	70	90	mV
Pro Logic off S/N (Full Bypass mode)	S/N off L,R		80	90		dB
Pro Logic off total harmonic distortion	THD off L,R			0.007	0.03	%
NR frequency characteristics	Dec1	0dB, 1kHz, VCC = 8.5 V, f = 1 kHz, THD = 1% (L,C,R), THD = 3% (LS, RS)	-1.5	0.0	1.5	dB
	Dec2	-20dB, 1kHz, VCC = 8.5 V, f = 1 kHz, THD = 1% (L,C,R), THD = 3% (LS, RS)	-24.0	-22.5	-21.0	dB
	Dec3	0dB, 5kHz, VCC = 8.5 V, f = 1 kHz, THD = 1% (L,C,R), THD = 3% (LS, RS)	-1.5	0.0	1.5	dB
	Dec4	-20dB, 5kHz, VCC = 8.5 V, f = 1 kHz, THD = 1% (L,C,R), THD = 3% (LS, RS)	-23.3	-21.8	-20.3	dB
	Dec5	-40dB, 5kHz, VCC = 8.5 V, f = 1 kHz, THD = 1% (L,C,R), THD = 3% (LS, RS)	-46.8	-45.3	-43.8	dB
Virtual Dolby Surround S/N	S/N v L, R	CCIR/ARM, Rg=10 kΩ	55	64		dB

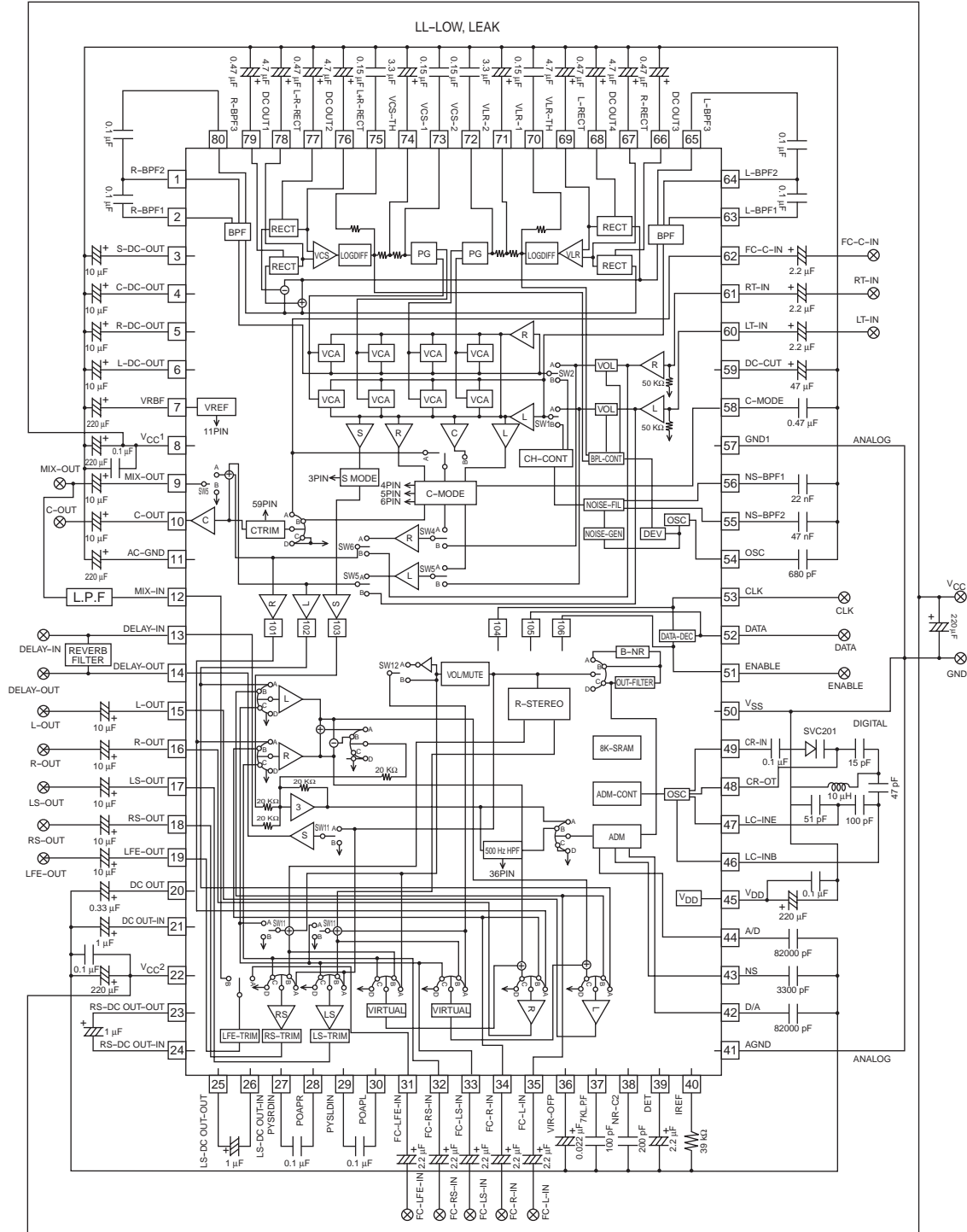
Block Diagram



ILV00002

LV1050M

Sample Application Circuit



ILV00007

Notes on LV1050M Usage

- Power is supplied to the matrix and steering control circuit in the LV1050M Dolby Prologic surround decoder from VCC1 (pin8) and GND1 (pin57). Power is supplied to the delay line circuit in the surround block from VCC2 (pin22) and GND2 (pin41), and power is supplied to the digital circuit blocks from VDD (pin45) and VSS (pin50).
- One Point that requires care is that mutual interactions (due to, for example, common impedances) between these power supply lines may influence the signals being processed, if this happens, phenomena such as sounds not being moved smoothly may occur.
- To prevent such phenomena from occurring, observe the following recommendations.
 - Design the printed circuit board layout so that all VCC and ground lines are as short and as wide as possible.
 - Connect all VCC and ground lines to the power supply independently.
 - Connect capacitors (about 220µF) between each of the VCC and ground pairs as close to the IC pins as possible.

Note : A sample power supply line layout is presented in the above diagram for reference.