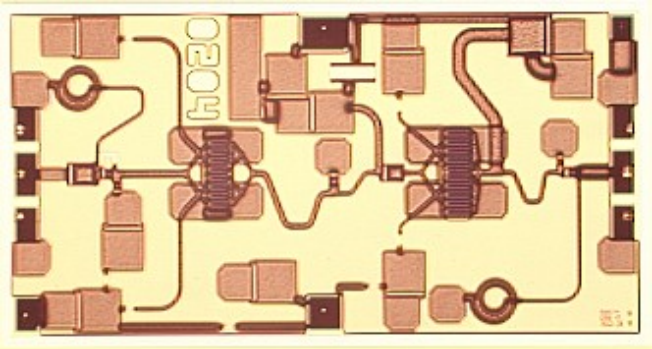
Amplifier, Power, 1.0W 6.5-12.5 GHz

MAAPGM0037-DIE
903241 —
Preliminary Information

Features

- **1.0 Watt Saturated Output Power Level**
- **Variable Drain Voltage (4-10V) Operation**
- **MSAG™ Process**



Description

The MAAPGM0037-Die is a 2-stage 1.0 W power amplifier with on-chip bias networks. This product is fully matched to 50 ohms on both the input and output. It can be used as a power amplifier stage or as a driver stage in high power applications.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate (MSAG™) Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.

Primary Applications

- **Instrumentation**
- **Test Equipment**
- **Electronic Warfare**

Electrical Characteristics: T_B = 40°C[1], Z_0 = 50Ω, V_{DD} = 8V, V_{GG} = -1.8V, P_{in} = 20 dBm

Parameter	Symbol	Typical	Units
Bandwidth	f	6.5-12.5	GHz
Output Power	P_{OUT}	30	dBm
Power Added Efficiency	PAE	27	%
1-dB Compression Point	P1dB	29	dBm
Small Signal Gain	G	13	dB
Input VSWR	VSWR	3:1	
Output VSWR	VSWR	2:1	
Gate Current	I_{GG}	< 2	mA
Drain Current	I_{DD}	< 500	mA
Output Third Order Intercept	TOI	37	dBm
Noise Figure	NF	8	dB
3rd Order Intermodulation Distortion Single Carrier Level = 21 dBm	IM3	30	dBc
5th Order Intermodulation Distortion Single Carrier Level = 21 dBm	IM5	43	dBc

1. T_B = MMIC Base Temperature

• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

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Maximum Operating Conditions [2]

Parameter	Symbol	Absolute Maximum	Units
Input Power	P_{IN}	25.0	dBm
Drain Supply Voltage	V_{DD}	+12.0	V
Gate Supply Voltage	V_{GG}	-3.0	V
Quiescent Drain Current (No RF)	I_{DQ}	470	mA
Quiescent DC Power Dissipated (No RF)	P_{DISS}	3.2	W
Junction Temperature	T_J	180	°C
Storage Temperature	T_{STG}	-55 to +150	°C

2. Operation outside of these ranges may reduce product reliability. Operation at other than the typical values may result in performance outside the guaranteed limits.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Drain Voltage	V_{DD}	4.0	8.0	10.0	V
Gate Voltage	V_{GG}	-2.4	-1.8	-1.5	V
Input Power	P_{IN}		20.0	23.0	dBm
Junction Temperature	T_J			150	°C
MMIC Base Temperature	T_B			Note 3	°C

3. Maximum MMIC Base Temperature = 150°C - 25.1°C/W * VDD * IDQ

Operating Instructions

This device is static sensitive. Please handle with care. To operate the device, follow these steps.

1. Apply V_{GG} = -1.8 V, V_{DD}= 0 V.
2. Ramp V_{DD} to desired voltage, typically 8.0 V.
3. Adjust V_{GG} to set I_{DQ}, (approximately @ –1.8 V).
4. Set RF input.
5. Power down sequence in reverse. Turn gate voltage off last.

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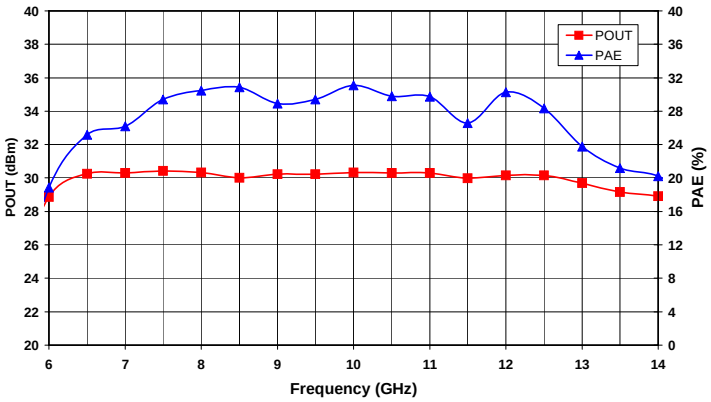

Figure 1. Output Power and Power Added Efficiency vs. Frequency at V_{DD} = 8V and P_{in} = 20 dBm.

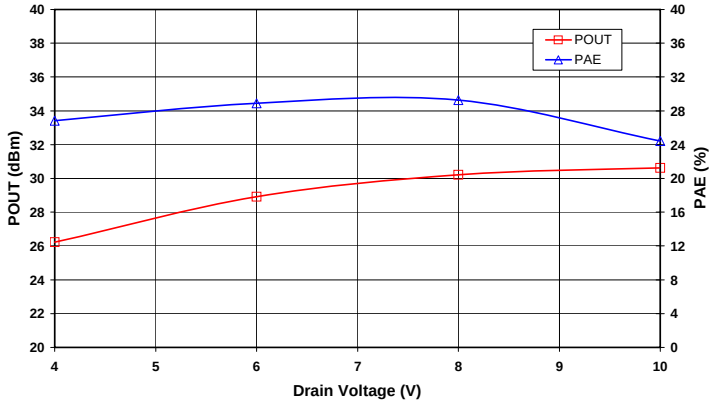

Figure 2. Saturated Output Power and Power Added Efficiency vs. Drain Voltage at f_o = 9.5 GHz.

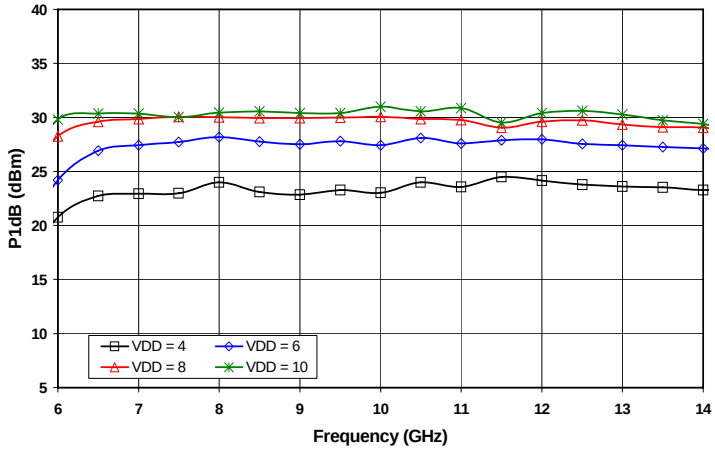

Figure 3. 1dB Compression Point vs. Drain Voltage

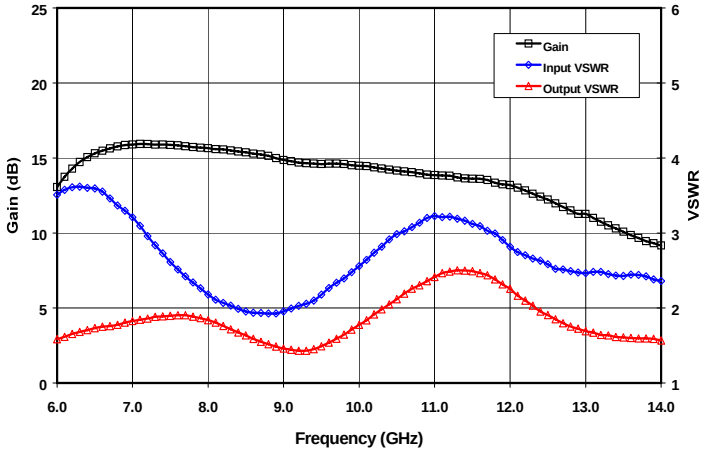

Figure 4. Small Signal Gain and VSWR vs. Frequency at VDD = 8V.

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Mechanical Information

Chip Size: 3.00 x 1.60 x 0.075 mm (118 x 63 x 3 mils)

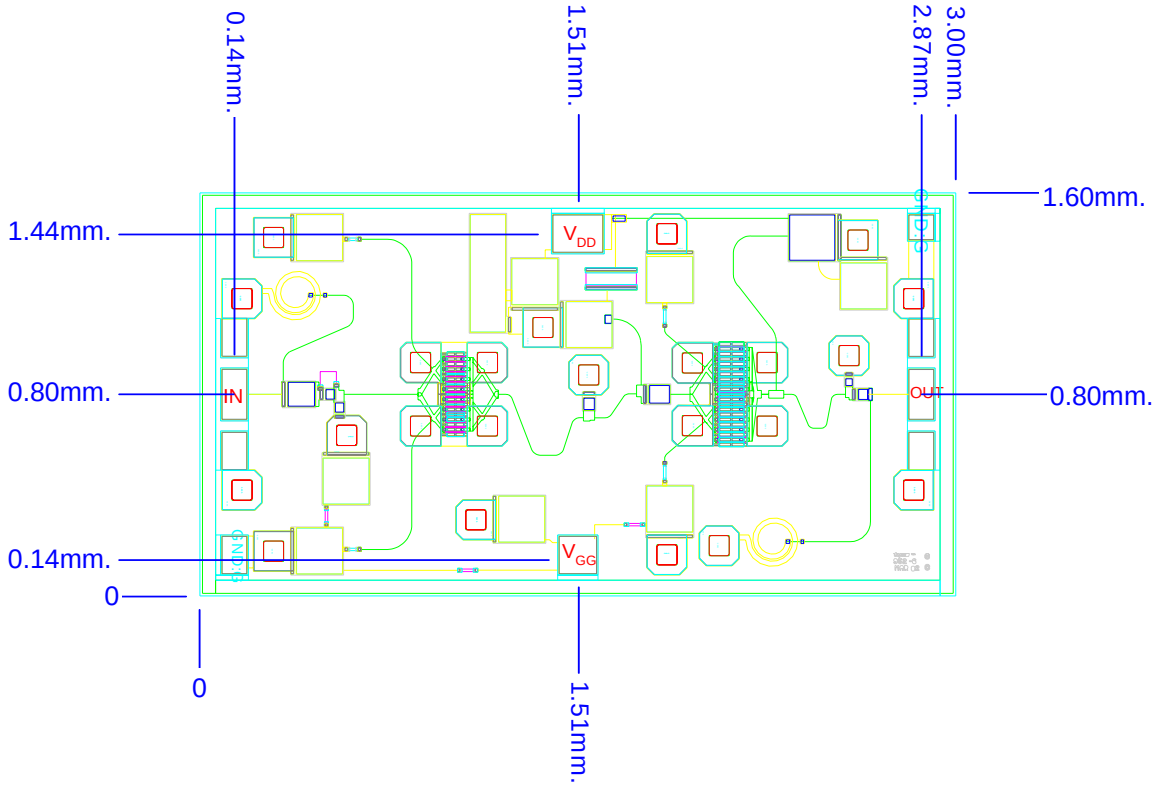

Figure 5. Die Layout

Bond Pad Dimensions

Pad	Size (µm)	Size (mils)
RF: IN, OUT	100 x 200	4 x 8
DC: V_{DD}	200 x 150	8 x 6
DC: V_{GG}	150 x 150	6 x 6

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Assembly and Bonding Diagram

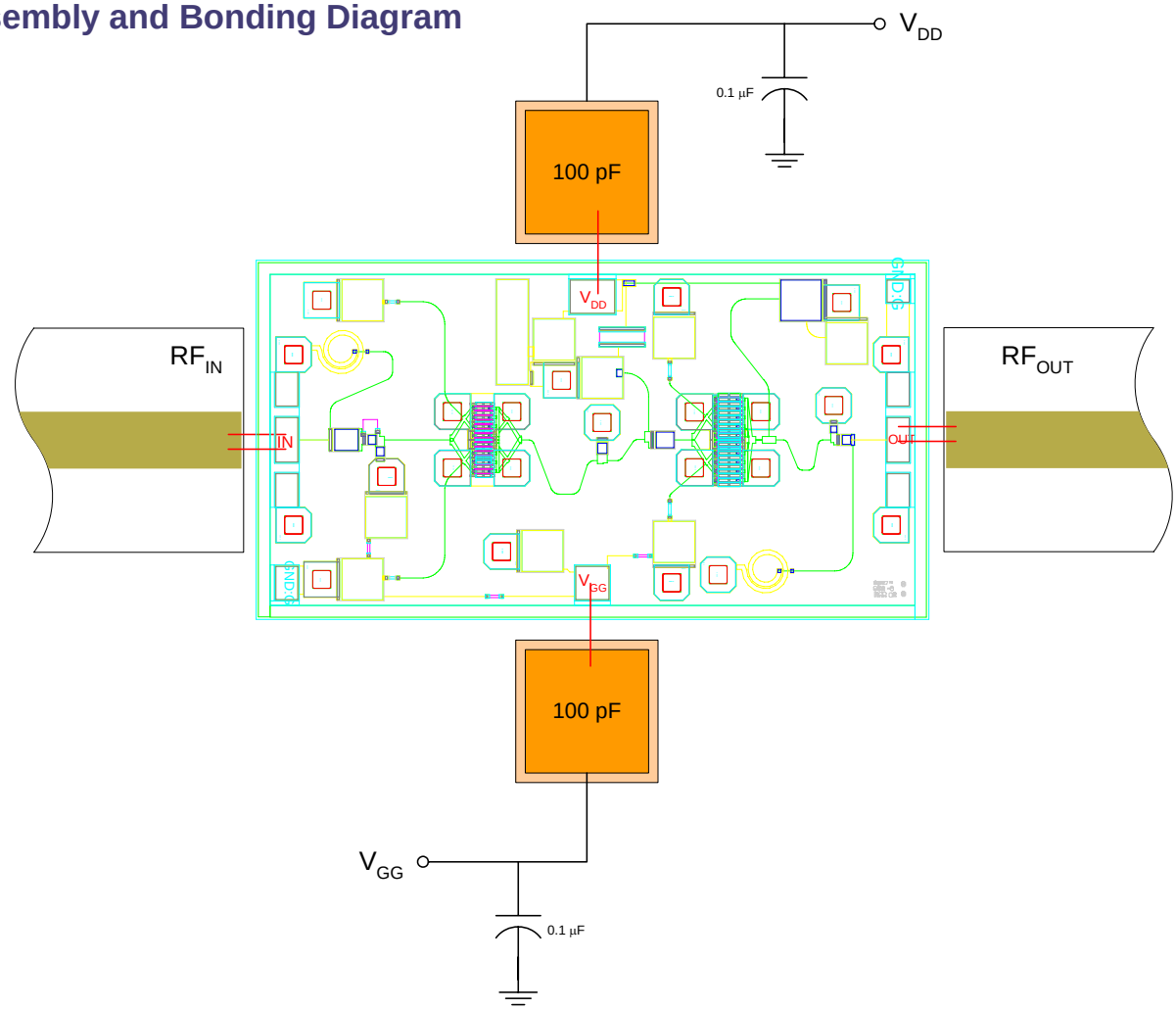

Figure 6. Recommended bonding diagram for pedestal mount.

Assembly Instructions:

Die attach: Use AuSn (80/20) 1 mil. preform solder. Limit time @ 300 °C to less than 5 minutes.

Wirebonding: Bond @ 160 °C using standard ball or thermal compression wedge bond techniques. For DC pad connections, use either ball or wedge bonds. For best RF performance, use wedge bonds of shortest length, although ball bonds are also acceptable.

Biasing Note: Must apply negative bias to V_{GG} before applying positive bias to V_{DD} to prevent damage to amplifier.

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