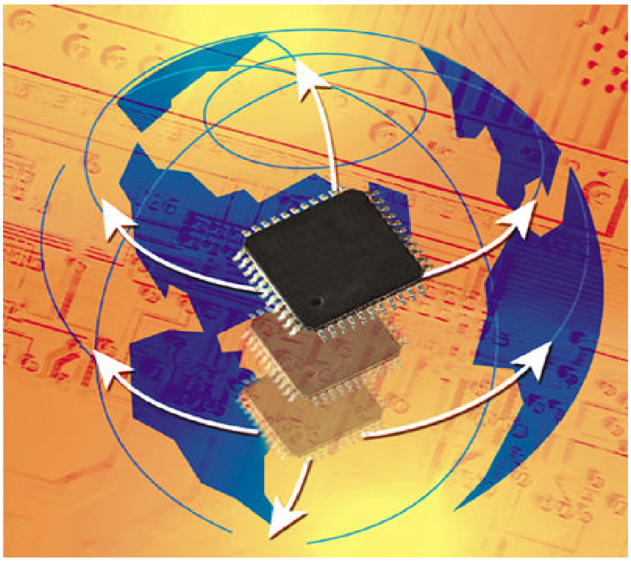
Qualification Package
MH1RT Sea of Gates
Radiation Tolerant 0.35 µm CMOS



MH1RT Sea of Gates
0.35 µm CMOS for Space Environment
QualPack

1. Table of Contents

2. General Information

Product Name:	MH1RT
Function:	ASIC Sea of Gates 1.6 million gates, 596 pins 200 KRAD Total Dose capability
Wafer Process:	CMOS 0.35µm Rad Tolerant, 4 metal levels
Available Package Types	PQFP, PowerQuad, L/TQFP,PLCC, PBGA, Super PBGA CPGA,CQFP, MQFPF, CLGA

Other Forms: Die, Wafer

Locations:

Process Development	Atmel Rousset, France Atmel Nantes, France
Product Development	Atmel Nantes, France
Wafer Plant	Atmel Rousset, France
QC Responsibility	Atmel Nantes, France
Probe Test	Atmel Nantes, France
Assembly	Atmel Grenoble, France (except plastic)
Final Test	Atmel Nantes, France
Lot Release	Atmel Nantes, France
Shipment Control	Atmel Nantes, France
Quality Assurance	Atmel Nantes, France
Reliability Testing	Atmel Nantes, France
Failure Analysis	Atmel Nantes, France

Quality Management
Atmel Nantes, France

Signed: Pascal LECUYER

3. Technology Information

3.1 Wafer Process Technology

Process Type (Name):	CMOS 0.35µm Rad Tolerant
Base Material:	Silicon Epi Substrate
Wafer Thickness (without back grinding)	725µm
Wafer Diameter	200mm
Number Of Masks	15
Gate Oxide	
Material	Silicon Dioxide
Thickness	70A (optical for 3.3V)
Polysilicon	
Number of Layers	1
Thickness	3200A
Metal	
Number of Layers	up to 4
Material:	Ti TiN AlCu
Layer 1/3 Thickness	400A + 800A + 5000A + 100A Ti + 1000A TiN
Upper layer Thickness	400A + 800A + 8000A + 250A TiN
Passivation	
Material	SiO2/Si3N4
Thickness	11000A / 10000A

3.2 Product Design

Pad size opening	80µm * 100µm
Logic Effective Channel Length	0.35µm
Gate Poly Width	0.35µm
Gate Poly Spacing	0.49µm
Metal 1 Width	0.42µm
Metal 1 Spacing	0.49µm
Metal 2 Width	0.56µm
Metal 2 Spacing	0.49µm
Metal 3 Width	0.56µm
Metal 3 Spacing	0.49µm
Metal 4 Width	0.56µm
Metal 4 Spacing	0.49µm
Contact Size	0.35µm
Contact Spacing	0.49µm
Via 1 Size	0.42µm
Via 2 Size	0.42µm

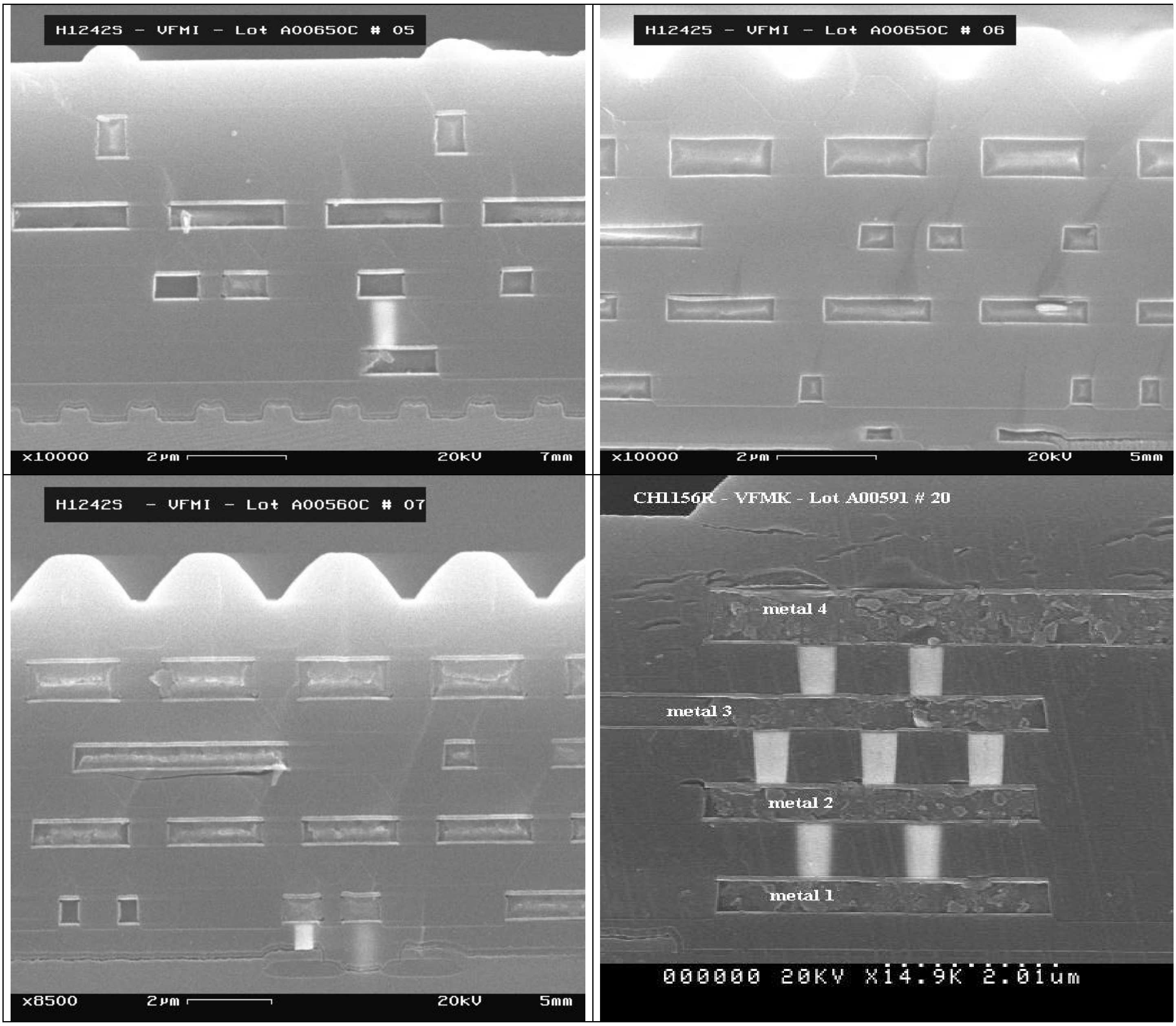
Test Vehicles:

Die Size:	5280*8130 (42.9mm²)
Pad Size	80µm * 100µm
Code:	EV29
Mask:	A5500
Number of metal levels:	3

Die Size:	13097*13097 (169.78mm²)
Pad Size	80µm * 100µm
Code:	DRAF (MH242S)
Mask:	A5544
Number of metal levels:	4

Die Size:	6601*6601 (30.9mm²)
Pad Size	90µm * 90µm
Code:	65809E
Mask:	A5552
Number of metal levels:	3

3.3 Cross Section



4. Qualification

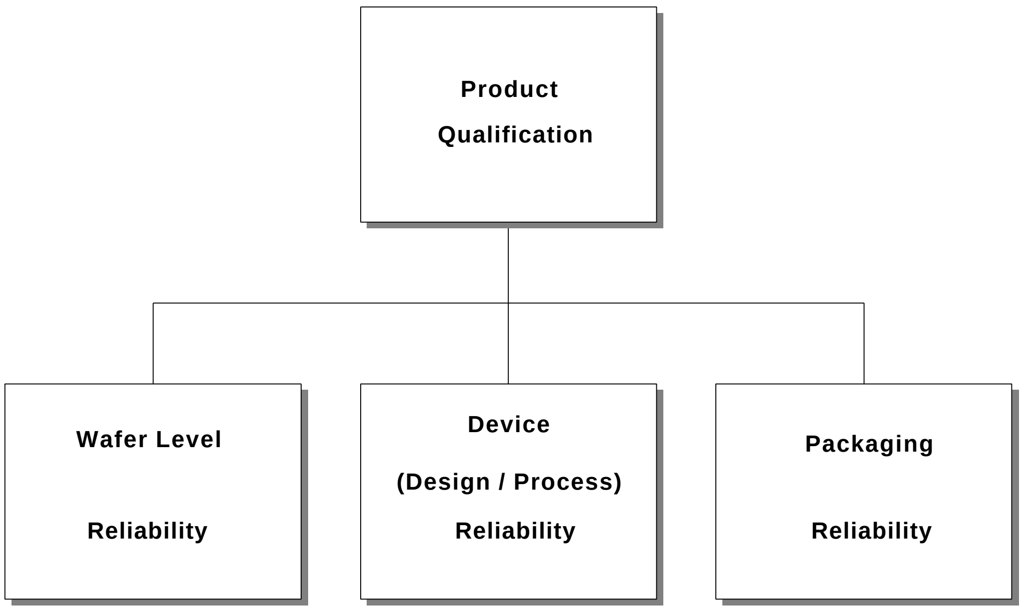
4.1 Qualification methodology

All product qualifications are split into three distinct steps as shown below. Before a product is released for use, successful qualification testing are required at wafer, device and package level.

Wafer Level Reliability consists in testing individually basic process modules regarding their well known potential limitations (Electromigration, Hot Carriers Injection, Oxide Breakdown, NVM Data Retention). Each test is performed using wafer process specific structures.

Device reliability is covering either dice design and processing aspects. The tests are performed on device under qualification, but generic data may also be considered for reliability calculation.

For each package type proposed in the Datasheet, it is verified that qualification data are available. If not qualification tests are carried out for the new package types. In addition, one package type is selected to verify packaging reliability of the device under qualification.



4.2 Qualification test methods

General Requirements for Hermetic CMOS ICs

Standard	Test Description	Acceptance
MIL-STD 883	**QCI Group C** **Electrical Life Test (Early Failure Rate)** 2000 hours 140°C	0/45 352h class B 0/45 700h class S
MIL-STD 883 Method 2016	**QCI Group D1** **Physical Dimensions**	0/15
MIL-STD 883 Method 2004 condition B2	**QCI GroupD2** **Lead Integrity**	0/3
MIL-STD 883 Method 1011 Method 1010 cond. C Method 1004	**QCI Group D3** **Thermal shocks** - 15 cycles **Temperature cycling** - 100 cycles **Moisture Resistance** - 240 hours	0/15
MIL-STD 883 Method 2002 Method 2007 Method 2001	**QCI Group D4** **Mechanical shocks** **Vibration at variable frequency** **Constant acceleration**	0/15
MIL-STD 883 Method 1009	**QCI Group D5** **Salt atmosphere**	0/15
MIL-STD 883 Method 1018	**QCI Group D6** **Internal vapor content**	0/3
MIL-STD 883 Method 2025	**QCI Group D7** **Lead finish adhesion**	0/15
MIL-STD 883 Method 2024	**QCI Group D8** **Lid torque**	0/5

4.3 Wafer Process Qualification

4.3.1 Wafer Level Reliability

This chapter contains all the information relative to the reliability of the 0.35um AT56K technology, from which the MH1RT library has been derived. Results presented in the following sections concern the reliability of the basic process steps which build up the technology.

4.3.2 Hot carrier qualification

Gate Oxides of 70 ang and 110 ang were subjected to stress to determine lifetimes due to Hot Carrier Injection.

The 70 ang oxide was subjected to a Vd = 3.6v for 10% IDSAT shift for a 10/.35um NMOS transistor. The DC results were .27 years which is equivalent to > 10 years for AC. (Source COS).

The 110 ang oxide was subjected to Vgs=3v and Vds=6v with a 0.6um gate length. Again the failure criterion was 10% IDSAT shift. The DC results were 1.1 years, which is equivalent to much greater than 10 years for AC (Source ES2).

Note: Spec = 0.2 years DC.

4.3.3 Electromigration

Electromigration testing was performed on six structures, which included Contact, Metal 1, Via 1, Metal 2, Via 2, and Metal 3. The conditions of the tests were 2E06 current density at an ambient temperature of 200C. The testing was terminated at 1017 hours. With the exception of Metal 2, there were no failures. In order to estimate a minimum life expectancy for the zero failure tests, time to first failure is calculated as if occurring at 1017 hours of stress time. The following table summarizes the results of this testing:

	Considered TF	Stress Temperature	Current Density J	Ea / n	Tf 0.1% (hrs)	Normalized Use Tf 0.1%
Contact	Tf 3.804% = 1017 hrs	195.49	2E06	0.66 / 2	272.72	654 Years
Metal 1	Tf 3.608% = 1017 hrs	203.68	2E06	0.66 / 2	279.36	670 Years
Via 1	Tf 3.608% = 1017 hrs	200.11	2E06	0.66 / 2	279.36	670 Years
Metal 2	MTF = 513.734 hrs	209.67	2E06	0.66 / 2	32.20	77 Years
Via 2	Tf 3.431% = 1017 hrs	200.97	2E06	0.66 / 2	285.85	685 Years
Metal 3	Tf 3.804% = 1017 hrs	212.77	2E06	0.66 / 2	272.72	654 Years

Source: ES2 - Serma Tech Report (2/19/99)

Note: Sample size for each structure = 20.

Additional Electromigration testing is ongoing. A sample of 15 devices with a straight line Metal 1 structure has been stressed for 300+ days at 200C and 3E06 Amps/cm^2. To date 8 devices have failed. The estimated normalized Tf, 0.1% failure point is 2000 years. In addition Metal 3 testing is ongoing. There has been only 2 failures out of 15 devices after 60+ days of testing. The testing is being performed at 3.5E06 Amps/cm2 at 250C.

	Stress Temperature	Ea / n	Current Density J	Tf 0.1% (hrs)	Normalized Use Tf 0.1%
Metal 1	200	0.6 / 2	3E06	102	2000 Years
Metal 3	250	0.6 / 2	3.5E06	ongoing	ongoing

Source: COS

Note: Sample size for each structure = 15.
Note: The above Normalized Use conditions are based on specified Operating Temperatures of 110C and Operating Current Densities of 2E05.

Time Dependent Dielectric Breakdown

Gate oxide testing was performed on both 70 and 110 ang. A total of 750 samples were tested using the 70 ang oxide and a total of 500 samples were tested using the 110 ang oxide.

Two tests were performed – the exponential current ramping test and the voltage ramping method. The following are the results of this testing:

QBd Results (0.1 A/Cm^2):

	Sample Size 70 ang	Sample Size 110 ang	% Defects below 1000 C/m2 70 ang	% Defects below 1000 C/m2 110 ang
Substrate Structure	750	500	0.4%	0%
Nwell Structure	750	500	0.4%	0%

Source: ES2

Note: Spec = 1.5%.

Ramping Voltage Results (2 V/s):

	Sample Size 70 ang	Sample Size 110 ang	Dola/Dolp 70 ang	Dola/Dolp 110 ang
Area Substrate Structure	750	500	0.09	0.43
Area Well Structure	750	500	0.13	0.43
Edge Substrate Structure	750	500	0.01	0.01
Edge Well Structure	750	500	0.01	0.01

Source: ES2

Note: Spec < 1.

4.3.4 Product Reliability Results

This section summarizes the cumulated AT56KRT technology reliability data.

Dynamic Operating Life Test

A total of 100 samples were life tested at 140°C . To date there have been no failures from this testing.
See results below:

PART NUMBER	LOT NUMBER	SAMPLE SIZE	TOTAL CKT HRS (K)	AMBIENT TEMP (°C)	Vcc (V)	FAILURES
EV29 MH1RT	E03624A	45	2000	140	3.7	0
65609E	A00422B	45	2000	140	3.7	0
DRAF MH1242	A00650B	10	2000	140	3.7	0

60% Confidence Estimate @ 50C & 0.6eV = 2.8 FITs
95% Confidence Estimate @ 50C & 0.6eV = 9.1 FITs

Early Failure Rate 48 hours @ 140°C, 100 devices from 3 lots / 0 Failure

4.4 Product Qualification

4.4.1 Device reliability

This section summarizes the cumulated qualification data of the MH1RT products.

Lots	Device Type/ Technology	Test Description	Step	Result	Comment
E03624A	EV29 MH1RT test vehicle	ESD	1000V 2000V 3000V 4000V	0/3 0/3 0/3 0/3	
E03624A	EV29 MH1RT test vehicle	Latch-up: Supply overvoltage Power injection	1.5*Vcc 50mW	0/5 0/5	
E03624A	EV29 MH1RT test vehicle Package: Side Braze 28	Operating Life Test	12h 500h 1000h 2000h	0/45 0/45 0/45 0/45	
A00422B	65609E 1MBIT SRAM SB32	Operating Life Test	0105h 0500h 1000h 2000h	0/45 0/45 0/45 0/45	
A00650B	DRAF MH1242 MQFPF 256	Operating Life Test	12h 80h 500h 1000h 2000h	0/10 0/10 0/10 0/10 0/10	

4.4.2 Packaging Reliability

This section summarizes the packaging reliability data of the MH1RT products.

Lots	Device Type/ Technology	Test Description	Step	Result	Comment
E03624A	EV29 MH1RT test vehicle Package: Side Braze 28	D3 Thermal Shocks D4 Mechanical Shocks	Elect. Visual Herm. Elect. Visual Herm.	0/15 0/15 0/15 0/15 0/15 0/15	
A00422F	65609E 1 MBIT SRAM MQFPF 32	D3 Thermal Shocks D4 Mechanical Shocks	Elect. Visual Herm. Elect. Visual Herm.	0/15 0/15 0/15 0/15 0/15 0/15	

4.5 Qualification status:

No failure noticed during MH1RT product qualification tests.

MH1RT ASIC Sea of Gates library has been qualified on March 2000.

MH1242 matrix tests allowed to extent the qualification domain up to the largest Sea of Gates size circuits.

4.6 Irradiation

4.6.1 Conditions and Chronology

The irradiation, according to the requirements of the MIL STD 883^{E} method 1019.5, and the Radiation Test Plan RTP085 is done using gamma rays from Cobalt 60 source using the EV29 test vehicle. The bias schematic is as defined in the radiation test plan. The temperature inside the irradiator chamber is 25°C.

In order to evaluate the influence of the internal bias of the device we decided to test 2 configurations. Half of the parts was initialized by loading the registers with 0 , the other half was initialized by loading the registers with 1.
The irradiation sequence was fully static following the bias conditions defined in the RTP85.

We affected the 18 parts following 5 distances in order to get 5 total dose set , which correspond to 5 dose rates during 20hours.

Total dose	Init at 0	Init at 0	Init at 0	Init at 1	Init at 1	Comment
100Krads	Sn1	Sn2		Sn3	Sn4	
200Krads	Sn5	Sn6		Sn7		
300Krads	Sn8	Sn9		Sn10	Sn11	
400Krads	Sn12	Sn13		Sn14		
500Krads	Sn15	Sn16	Sn17	Sn18		

The dosimetry has been controlled with a PTW probe referenced by the Laboratoire National Henri Becquerel with a 10% accuracy.

The chronology of events is listed in table 1. The parts (all leads in short circuit) are transferred to the test area after the end of the irradiation without bias.

The annealing sequence has been conducted as follows :

- Storage at ambient temperature under bias.
- Electrical measurements at ambiant temperature until recovery of electrical parameters.
  Overtest (half total dose additional irradiation):

Total dose	Init at 0	Init at 0	Init at 0	Init at 1	Init at 1	Comment
50Krads	Sn1	Sn2		Sn3	Sn4	
100Krads	Sn5	Sn6		Sn7		
150Krads	Sn8	Sn9		Sn10	Sn11	
200Krads	Sn12	Sn13		Sn14		
250Krads	Sn15	Sn16	Sn17	Sn18		

- Storage at 100°C under bias during 168 hours.
- Electrical measurements at ambient temperature.

4.6.2 Results

All the parts passed the functional test even after 500krads irradiation provided the power supply can deliver the requested current (range 2A)

A . **ICCSB** (in mA on the graphs) : It is the most sensitive parameter . The measurement is done following three conditions:
ICCSB00 the registers are loaded with 0
ICCSB10 the registers are loaded with a queue 01010…
ICCSB11 the registers are loaded with 1.
It has to be noticed that where the parts were irradiated with registers to 0 ICCSB00 is 0
All the other configuration exhibit a large increase of ICCSB higher than 1amp (The 3 first measurements were clamped to 250mA);
The 3 weeks ambient annealing shows a slow but significant recovery of the parameter .
The 2 last additional weeks of annealing was in dynamic mode (clk active in low frequency) and thus the recovery is fully achieved.
The additional half dose irradiation test confirms the previous behavior and the high temperature annealing leads to an almost full recovery of the parameter.

B. **Input leakages** (in uA on the graphs),
Only IIL is affected on the parts at 400krads and 500krads . This is recovered after annealing.

C.**Tpd** (TP8 given as an example in ns), **Input clamp voltages**
No significant change can be observed even after 500krads irradiation.

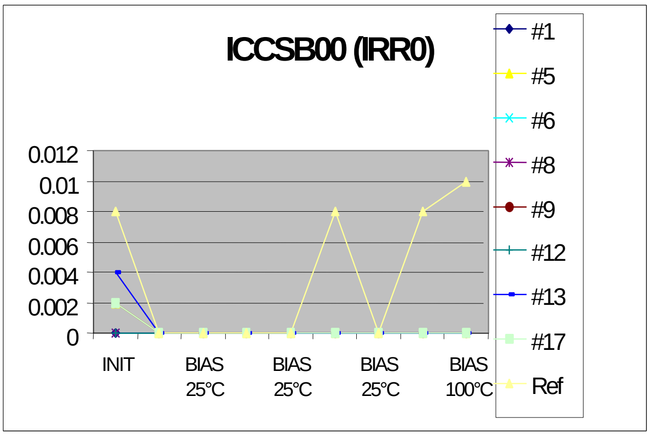
D. **Output voltages**
These parameters drift slightly due to irradiation but remains inside the specifications limits.
The recovery is achieved after ambient bias annealing .

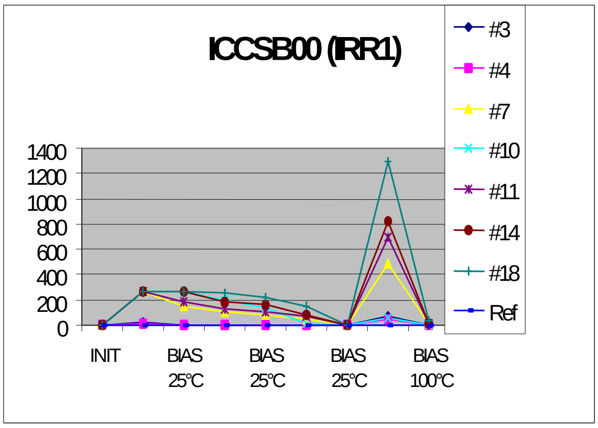
4.6.3 Irradiation summary

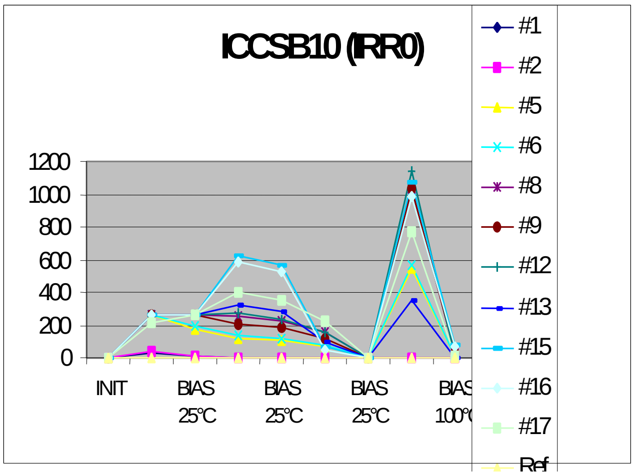
This test plan shows the high tolerance of the V29, MH1RT Test Vehicle to a total ionizing dose irradiation with Cobalt 60 gamma ray up to 500krads following the MIL STD 883 method 1019.5.

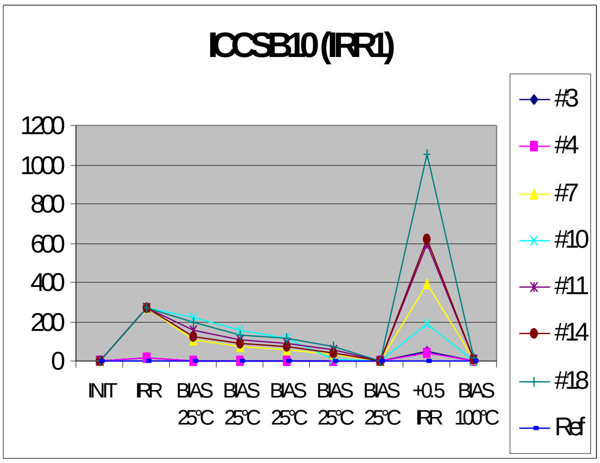
The behavior noticed on the test vehicle during the qualification experiments can reasonably be predicted on the whole MH1RT product family.

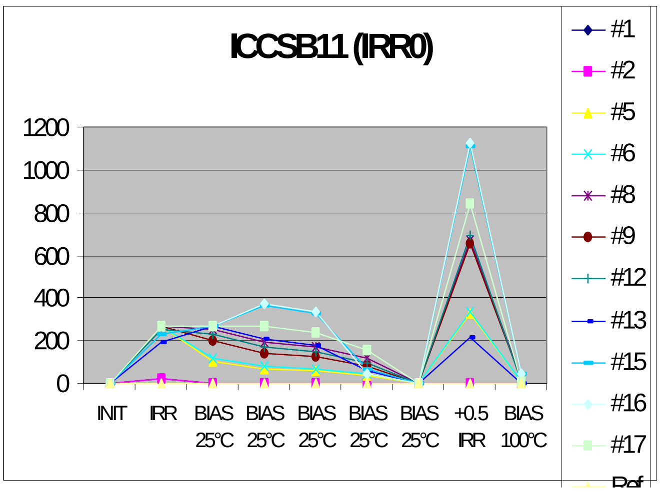
4.6.4 Irradiation test records

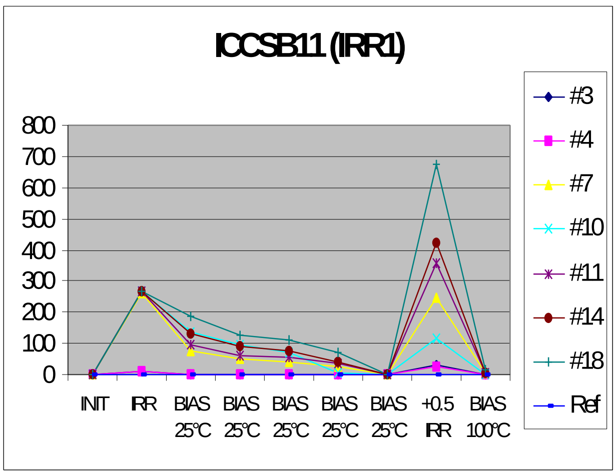


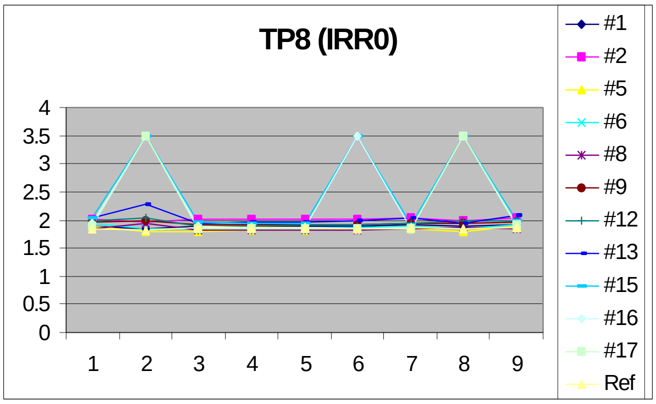











TP8 (IRR0)
4
3.5
3
2.5
2
1.5
1
0.5
0
1 2 3 4 5 6 7 8 9
#1
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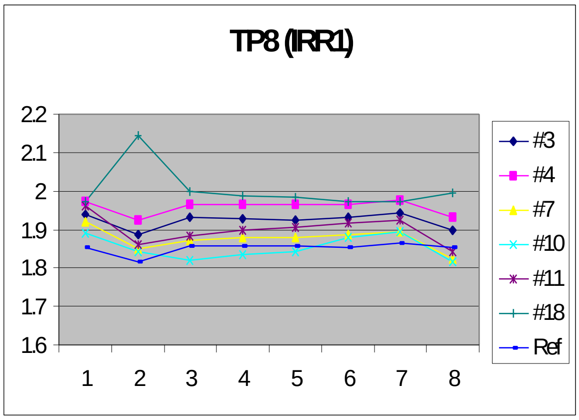
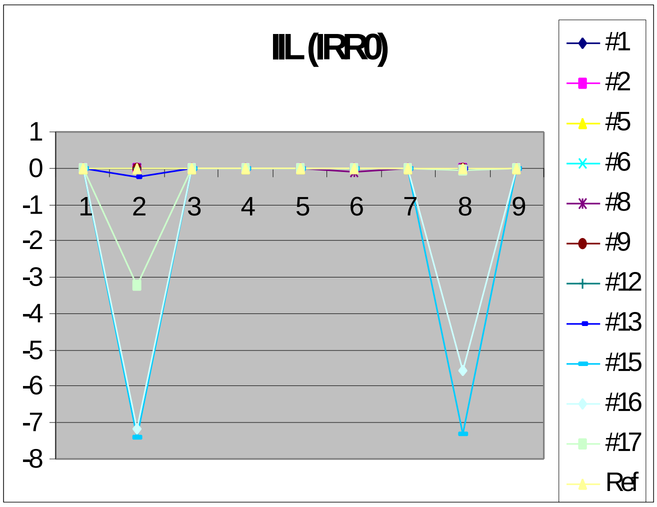
#8
#9
#12
#13
#15
#16
#17
Ref


TP8 (IRR1)
2.2
2.1
2
1.9
1.8
1.7
1.6
1 2 3 4 5 6 7 8
#3
#4
#7
#10
#11
#18
Ref


IIL (IRR0)
1
0
-1
-2
-3
-4
-5
-6
-7
-8
1 2 3 4 5 6 7 8 9
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#6
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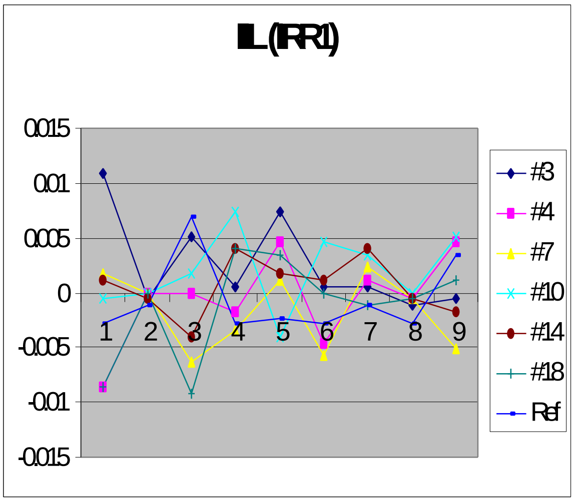
#15
#16
#17
Ref


IIL (IRR1)
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0.01
0.005
0
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-0.015
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#10
#14
#18
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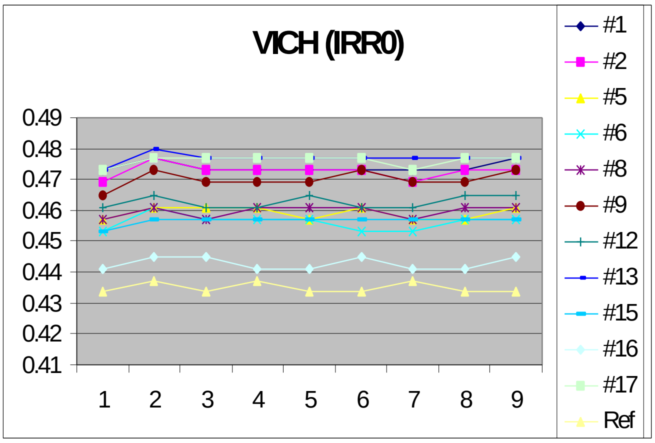
VICH (IRR0)
0.49
0.48
0.47
0.46
0.45
0.44
0.43
0.42
0.41
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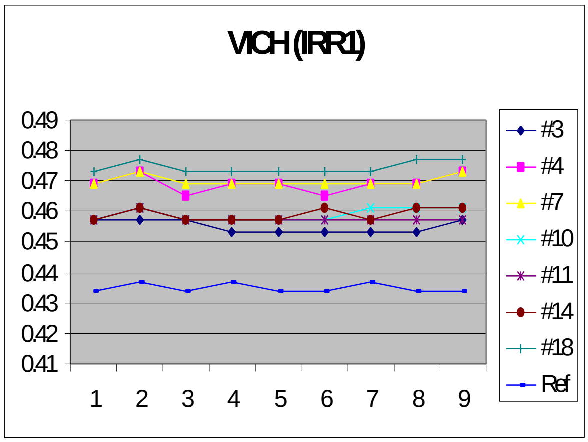
#15
#16
#17
Ref


VICH (IRR1)
0.49
0.48
0.47
0.46
0.45
0.44
0.43
0.42
0.41
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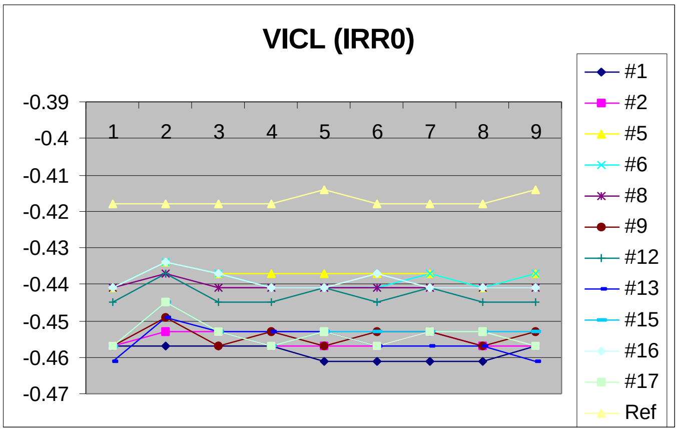
#11
#14
#18
Ref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-0.41
-0.42
-0.43
-0.44
-0.45
-0.46
-0.47
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#1
#2
#5
#6
#8
#9
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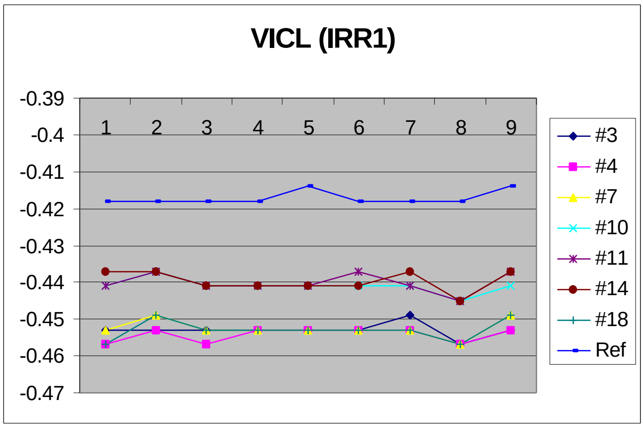
Ref


VICL (IRR1)
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-0.4
-0.41
-0.42
-0.43
-0.44
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-0.47
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#3
#4
#7
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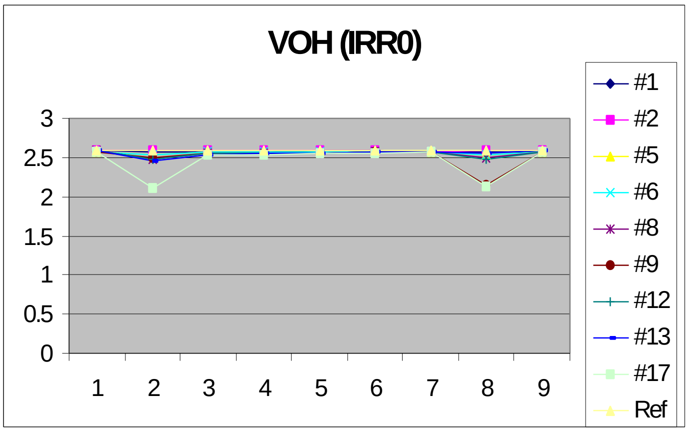
#11
#14
#18
Ref


VOH (IRR0)
3
2.5
2
1.5
1
0.5
0
1 2 3 4 5 6 7 8 9
#1
#2
#5
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#12
#13
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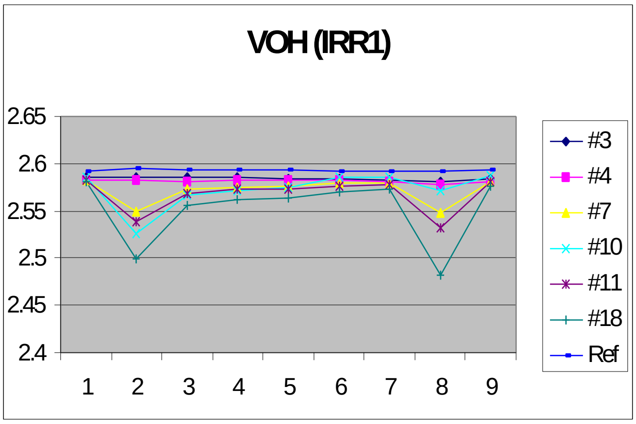
Ref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#11
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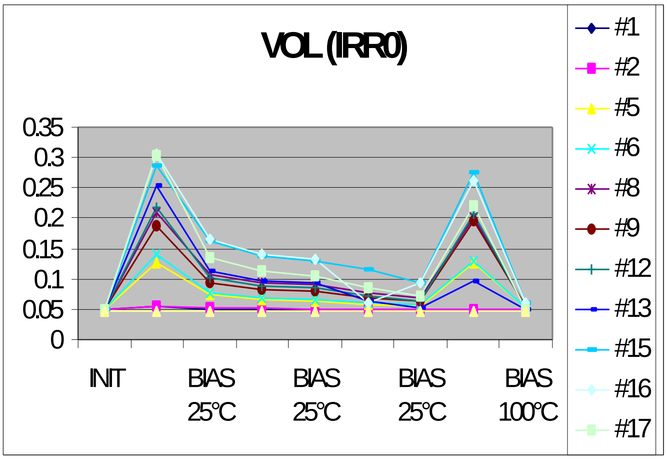
Ref


VOL (IRR0)
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0.3
0.25
0.2
0.15
0.1
0.05
0
INIT
BIAS 25°C
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#13
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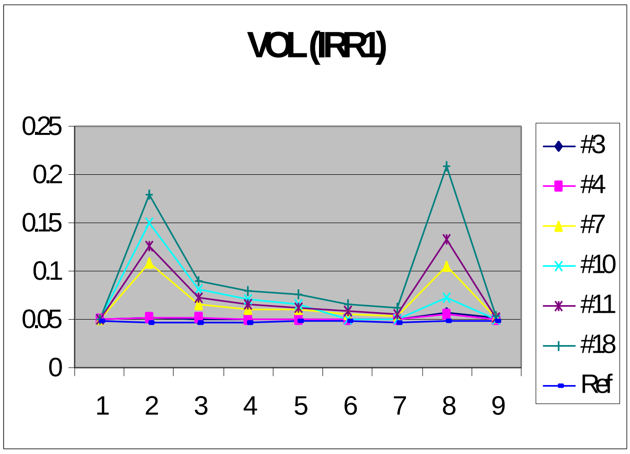
#16
#17


VOL (IRR1)
0.25
0.2
0.15
0.1
0.05
0
1 2 3 4 5 6 7 8 9
#3
#4
#7
#10
#11
#18
Ref

5. Environmental Information

Atmel Environmental Policy:

Atmel is committed to providing a safe and healthy workplace and complying with all environmental regulations.

Essential Elements
Our environmental, health and safety goals are to prevent incidents that:

Cause injury to our employees and visitors
Harm the environment
Cause property loss, and/or
Result in business interruption

Our goals also include a commitment to comply with environmental, health, and safety regulations, as well as a commitment to protect our human and natural resources.

We believe that all accidents and undesirable environmental incidents are preventable. Furthermore, there is no job which should become so routine, or so urgent that it cannot be done safely and/or in an environmentally sound manner.

Realization of these goals and objectives demand the support of every employee, at every level of the organization. Atmel employees must embrace this policy with the same spirit, commitment of resources, and intelligence, as we embrace customer satisfaction, product quality, and continuous improvement.

As part of this corporate policy, Ozone Depleting Chemicals are being replaced either by Atmel Nantes or its sub-contractors. In addition the factory is committed in:

- Reducing the use of harmful chemicals in its processes

- Reducing the content of harmful materials in its products

- Using recyclable materials wherever possible

- Reducing the energy content of its products

Atmel Nantes is ISO14001 certified since May 2000.

6. Other Data

6.1 ISO9001 and QS900 Certificates

CERTIFICAT AFAQ CERTIFICATE

N° QS/1999/12758a

AFAQ certifie que le système qualité adopté par,
AFAQ certifies that the quality system developed by :

ATMEL NANTES SA

pour les activités suivantes,
for the following activities :

CONCEPTION ET PRODUCTION DE CIRCUITS INTEGRES ET ASICS.

DESIGN AND PRODUCTION OF INTEGRATED CIRCUITS AND ASICS.

exercées sur le(s) site(s) suivant(s),
carried out in the following location(s) :

La Chantrerie BP 70602 F-44306 NANTES CEDEX 3

a été évalué conformément au code de déontologie de l'annexe B du QS-9000
et jugé conforme aux exigences des référentiels,
has been assessed in accordance with QS-9000 appendix B code of practice
and found to conform to the requirements of the standards :

ISO 9001 (1994) QS-9000 (03/98)

Le présent certificat, délivré dans les conditions fixées par AFAQ, est valable à dater du,
This certificate, delivered under AFAQ rules, is valid as from :

2001-01-30

(année-mois-jour) *jusqu'au / until** 2003-07-17 (year-month-day)

LE PRÉSIDENT DU COMITÉ DE CERTIFICATION *THE PRESIDENT OF THE CERTIFICATION COMMITTEE*	LE DIRECTEUR GÉNÉRAL D'AFAQ *THE MANAGING DIRECTOR OF AFAQ*	LE REPRÉSENTANT DE L'ENTREPRISE *ON BEHALF OF THE FIRM*
A. PIGEONNIER	O. PEYRAT	F. FAES

*Sauf suspension notifiée entre temps par AFAQ à l'entreprise désignée ci-dessus, qui s'est engagée à observer les règles définies par AFAQ. Le présent document ne peut se substituer en aucune manière au contrat signé entre l'entreprise et AFAQ, qui seul fait foi.
*Excepting notification by AFAQ of suspension of the above-mentioned company, which has agreed to respect the relevant AFAQ rules. The present document shall not replace, in any event the contract signed by the firm and AFAQ, which remains the sole binding document.

AFAQ - 116 AVENUE ARISTIDE BRIAND - BP 40 / F-92224 BAGNEUX CEDEX FRANCE

6.2 Data Book Reference

The data sheet is available upon request to sales representative or in Atmel site:

http://www.atmel.com/

Data sheet:

MH1RT 1.6M used gate Sea of Gates Rad Tolerant

Address References
All inquiries relating to this document should be addressed to the following:

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Product Assurance Manager
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Remarks: