

MH1V36CAM-6,-7

FAST PAGE MODE 37748736-BIT (1048576-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH1V36CAM is an 1M word by 36-bit dynamic RAM module and consists of 2 industry standard 1M X 16 dynamic RAMs in TSOP and 1 industry standard 1M X 4(4CAS) dynamic RAMs in TSOP.

The ICs are mounted on both sides of one small ceracom PC board with flash gold plating and form a convenient 68-pin package.

FEATURES

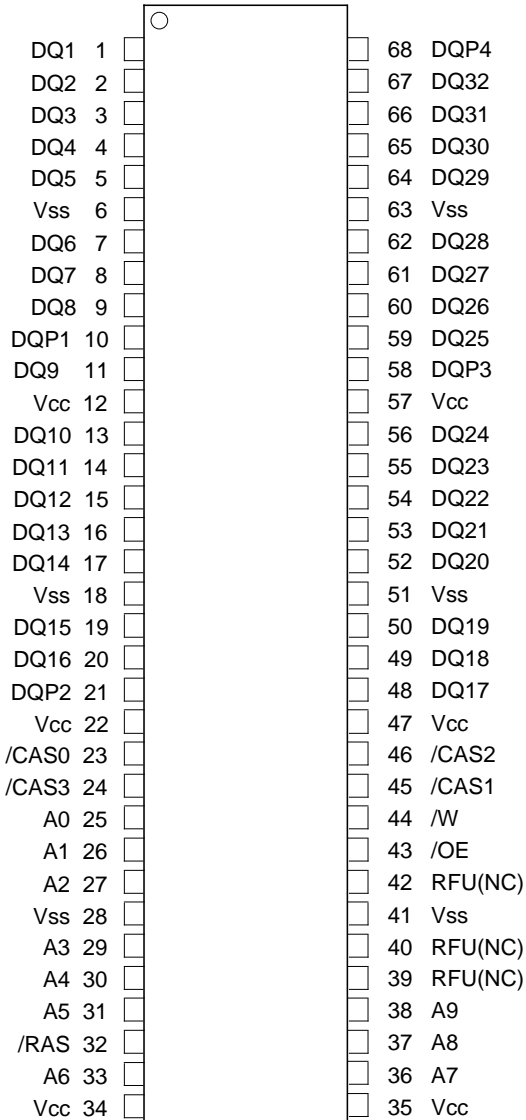
Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)
MH1V36CAM-6	60	15	30	15	110
MH1V36CAM-7	70	20	35	20	130

- Utilizes industry standard 1M X 16 DRAMs in TSOP package and industry standard 1M X 4(4CAS) DRAM in TSOP package
- Single 3.3V +/- 0.3V supply
- Low stand-by power dissipation
9mW (Max) CMOS Input level
- Low operating power dissipation
MH1V36CAM - 6 1.37W (Max)
MH1V36CAM - 7 1.20W (Max)
- All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A₀ ~ A₉)
- Includes 2pcs 0.22uF decoupling capacitors

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)



Preliminary Spec.

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FUNCTION

The MH1V36CAM provide, in addition to normal read, write, and read-modify-write operations, a number of

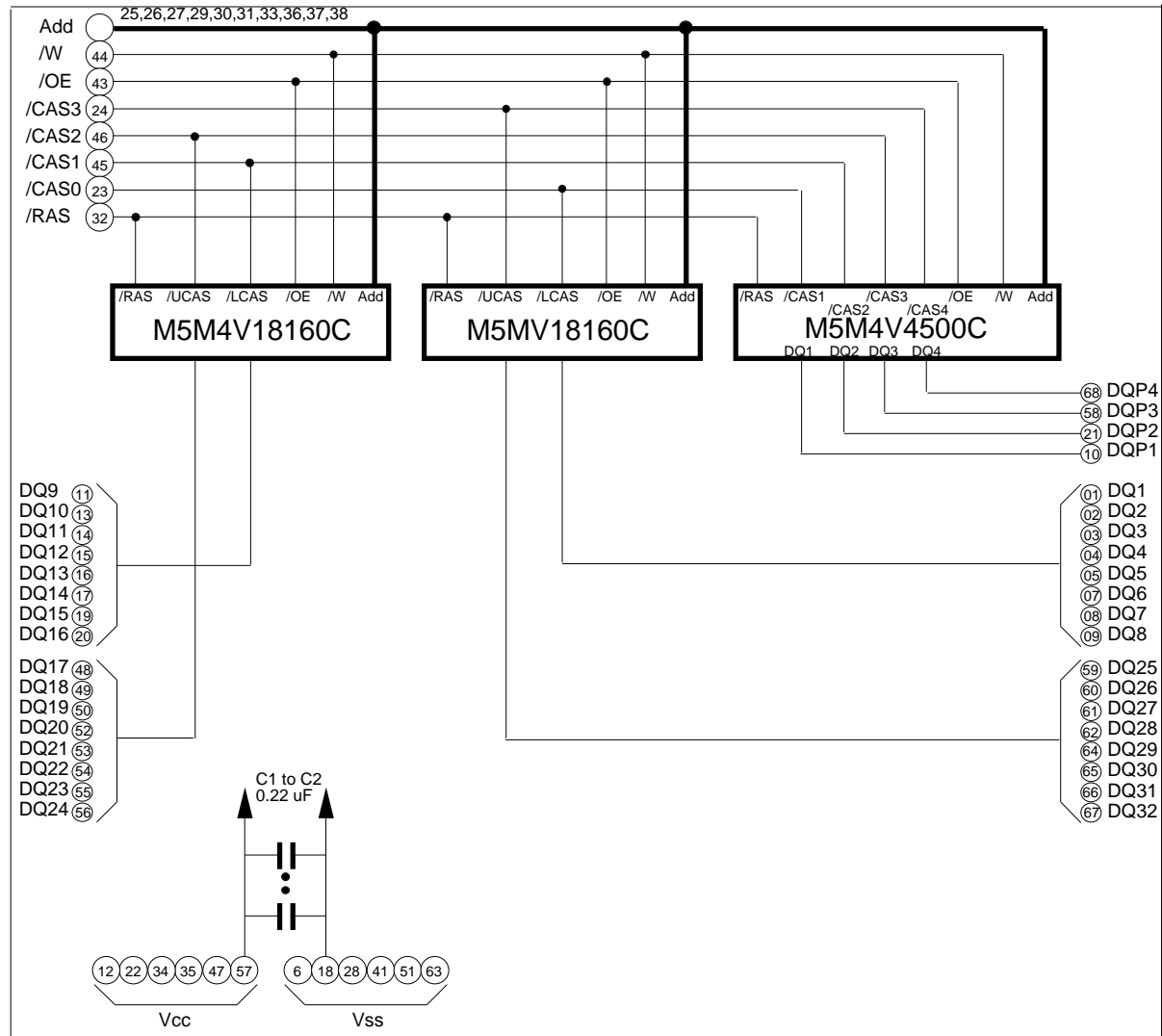
other functions, e.g., fast page mode, RAS-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	RAS	CAS	W	OE	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	Fast page mode identical
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
RAS-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
CAS before RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to V _{ss}	-0.5 ~ 4.6	V
V _I	Input voltage		-0.5 ~ 4.6	V
V _O	Output voltage		-0.5 ~ 4.6	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	3	W
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0 ~70 °C , unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{cc}	Supply voltage	3.0	3.3	3.6	V
V _{ss}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.0		V _{cc} +0.3	V
V _{IL}	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1 : All voltage values are with respect to V_{ss}

ELECTRICAL CHARACTERISTICS (T_a=0 ~70 °C, V_{cc}=3.3V±0.3V, V_{ss}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
VOH	High-level output voltage	I _{OH} =-2.0mA	2.4		V _{cc}	v
VOL	Low-level output voltage	I _{OL} =2.0mA	0		0.4	v
IOZ	Off-state output current	Q floating 0V V _{OUT} 3.3V	-10		10	
I _I	Input current	0V V _{IN} 3.6V, Other inputs pins=0V	-30		30	
I _{CC1} (AV)	Average supply current from V _{cc} operating (Note 3,4,*)	-6			380	mA
		-7			330	
I _{CC2}	Supply current from V _{cc} , stand-by	RAS= CAS =VIH, output open			6	mA
		RAS= CAS V _{cc} -0.2V, output open			1.5	
I _{CC3} (AV)	Average supply current from V _{cc} refreshing (Note 3,*)	-6			380	mA
		-7			330	
I _{CC4} (AV)	Average supply current from V _{cc} Fast-Page-Mode (Note 3,4,*)	-6			210	mA
		-7			190	
I _{CC6} (AV)	Average supply current from V _{cc} CAS before RAS refresh mode (Note 3,5,*)	-6			370	mA
		-7			320	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{cc1} (AV), I_{cc3} (AV) , I_{cc4} (AV) and I_{cc6} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{cc1} (AV) and I_{cc4} (AV) are dependent on output loading. Specified values are obtained with the output open.

*: Column Address can be changed once or less while RAS=V_{IL} and LCAS/UCAS=VIH

CAPACITANCE (T_a=0~70°C , V_{cc}=3.3V±0.3V, V_{ss}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I (A)	Input capacitance, address inputs	V _I =V _{ss} f=1MHZ V _i =25mVrms			50	pF
C _I (OE)	Input capacitance, OE input				55	pF
C _I (W)	Input capacitance, write control input				55	pF
C _I (RAS)	Input capacitance, RAS input				55	pF
C _I (CAS)	Input capacitance, CAS input				50	pF
C _I / O	Input/Output capacitance, data ports				40	pF

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SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.3V +/-0.3V, Vss=0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t _{CAS}	Access time from $\overline{\text{CAS}}$ (Note 6,7)		15		20	ns
t _{RAS}	Access time from $\overline{\text{RAS}}$ (Note 6,8)		60		70	ns
t _{AA}	Column address access time (Note 6,9)		30		35	ns
t _{CPA}	Access time from $\overline{\text{CAS}}$ precharge (Note 6,10)		35		40	ns
t _{OE}	Access time from $\overline{\text{OE}}$ (Note 6)		15		20	ns
t _{CLZ}	Output low impedance time from $\overline{\text{CAS}}$ low (Note 6)	5		5		ns
t _{OFF}	Output disable time after $\overline{\text{CAS}}$ high (Note 11)	0	15	0	20	ns
t _{OEZ}	Output disable time after $\overline{\text{OE}}$ high (Note 11)	0	15	0	20	ns

Note 5: An initial pause of 500us is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 $\overline{\text{RAS}}$ or $\overline{\text{RAS/CAS}}$ cycles are required after prolonged periods (greater than 16.4 ms) of RAS inactivity before proper device operation is achieved.

6: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-2mA)/V_{OL}=0.4V(I_{OL}=2mA) load 100pF.

The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

7: Assumes that t_{RCd} t_{RCd(max)} and t_{ASC} t_{ASC(max)}.

8: Assumes that t_{RCd} t_{RCd(max)} and t_{RAD} t_{RAD(max)}. If t_{RCd} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCd} exceeds the value shown.

9: Assumes that t_{RAD} t_{RAD(max)} and t_{ASC} t_{ASC(max)}.

10: Assumes that t_{CP} t_{CP(max)} and t_{ASC} t_{ASC(max)}.

11: t_{OFF(max)} and t_{OEZ(max)} defines the time at which the output achieves the high impedance state (I_{out} I +/- 10uA) and is not reference to V_{OH(min)} or V_{OL(max)}.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)

(Ta=0 ~ 70 °C, Vcc=3.3V +/- 0.3V, Vss=0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
t _{REF}	Refresh cycle time		16.4		16.4	ms
t _{RP}	RAS high pulse width	40		50		ns
t _{RCd}	Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ low (Note14)	20	45	20	50	ns
t _{CRP}	Delay time, $\overline{\text{CAS}}$ high to $\overline{\text{RAS}}$ low	10		10		ns
t _{RPC}	Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ low	0		0		ns
t _{CPN}	$\overline{\text{CAS}}$ high pulse width	10		10		ns
t _{RAD}	Column address delay time from $\overline{\text{RAS}}$ low (Note15)	15	30	15	35	ns
t _{ASR}	Row address setup time before $\overline{\text{RAS}}$ low	0		0		ns
t _{ASC}	Column address setup time before $\overline{\text{CAS}}$ low (Note16)	0	10	0	10	ns
t _{RAH}	Row address hold time after $\overline{\text{RAS}}$ low	10		10		ns
t _{CAH}	Column address hold time after $\overline{\text{CAS}}$ low	15		15		ns
t _{DZC}	Delay time, data to $\overline{\text{CAS}}$ low (Note17)	0		0		ns
t _{DZO}	Delay time, data to $\overline{\text{OE}}$ low (Note17)	0		0		ns
t _{CDD}	Delay time, $\overline{\text{CAS}}$ high to data (Note18)	15		20		ns
t _{ODD}	Delay time, $\overline{\text{OE}}$ high to data (Note18)	15		20		ns
t _t	Transition time (Note19)	1	50	1	50	ns

Note 12: The timing requirements are assumed t_t=5ns.

13: V_{IH(min)} and V_{IL(max)} are reference levels for measuring timing of input signals.

14: t_{RCd(max)} is specified as a reference point only. If t_{RCd} is less than t_{RCd(max)}, access time is t_{RAC}. If t_{RCd} is greater than t_{RCd(max)}, access time is controlled exclusively by t_{CAS} or t_{AA}. t_{RCd(min)} is specified as t_{RCd(min)} = t_{RAH(min)} + 2t_t + t_{ASC(min)}.

15: t_{RAD(max)} is specified as a reference point only. If t_{RAD} t_{RAD(max)} and t_{ASC} t_{ASC(max)}, access time is controlled exclusively by t_{AA}.

16: t_{ASC(max)} is specified as a reference point only. If t_{RCd} t_{RCd(max)} and t_{ASC} t_{ASC(max)}, access time is controlled exclusively by t_{CAS}.

17: Either t_{DZC} or t_{DZO} must be satisfied.

18: Either t_{CDD} or t_{ODD} must be satisfied.

19: t_t is measured between V_{IH(min)} and V_{IL(max)}.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
trc	Read cycle time	110		130		ns
trAS	RAS low pulse width	60	10000	70	10000	ns
tcAS	CAS low pulse width	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	60		70		ns
trSH	RAS hold time after CAS low	15		20		ns
trCS	Read Setup time after CAS high	0		0		ns
trCH	Read hold time after CAS low (Note 20)	0		0		ns
trRH	Read hold time after RAS low (Note 20)	10		10		ns
trAL	Column address to RAS hold time	30		35		ns
toCH	CAS hold time after OE low	15		20		ns
toRH	RAS hold time after OE low	15		20		ns

Note 20: Either trCH or trRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
twc	Write cycle time	110		130		ns
trAS	RAS low pulse width	60	10000	70	10000	ns
tcAS	CAS low pulse width	15	10000	20	10000	ns
tCSH	CAS hold time after RAS low	60		70		ns
trSH	RAS hold time after CAS low	15		20		ns
twCS	Write setup time before CAS low (Note 22)	0		0		ns
twCH	Write hold time after CAS low	10		15		ns
tcWL	CAS hold time after W low	15		20		ns
trWL	RAS hold time after W low	15		20		ns
tWP	Write pulse width	10		15		ns
tDS	Data setup time before CAS low or W low	0		0		ns
tdH	Data hold time after CAS low or W low	10		15		ns
toEH	OE hold time after W low	15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
trWC	Read write/read modify write cycle time (Note21)	155		180		ns
tRAS	RAS low pulse width	105	10000	120	10000	ns
tCAS	CAS low pulse width	60	10000	70	10000	ns
tCSH	CAS hold time after RAS low	105		120		ns
tRSH	RAS hold time after CAS low	60		70		ns
tRCS	Read setup time before CAS low	0		0		ns
tcWD	Delay time, CAS low to W low (Note22)	40		45		ns
trWD	Delay time, RAS low to W low (Note22)	85		95		ns
tAWD	Delay time, address to W low (Note22)	55		60		ns
tcWL	CAS hold time after W low	15		20		ns
trWL	RAS hold time after W low	15		20		ns
tWP	Write pulse width	10		15		ns
tDS	Data setup time before W low	0		0		ns
tDH	Data hold time after W low	10		15		ns
toEH	OE hold time after W low	15		20		ns

Note 21: trWC is specified as $trWC_{(min)} = trAC_{(max)} + tODD_{(min)} + trWL_{(min)} + trP_{(min)} + 5t$.

22: tcWS, tcWD, trWD and tAWD and, tcPWD are specified as reference points only. If tcWS (min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If tcWD (min), trWD (min), tAWD (min) and tcPWD (min) (for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to V_{ih}) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time	40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time	85		95		ns
tRAS	RAS low pulse width for read write cycle (Note24)	100	100000	115	100000	ns
tCP	CAS high pulse width (Note25)	10	15	10	15	ns
tcPRH	RAS hold time after CAS precharge	35		40		ns
tcPWD	Delay time, CAS precharge to W low (Note22)	60		65		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.

24: tRAS (min) is specified as two cycles of CAS input are performed.

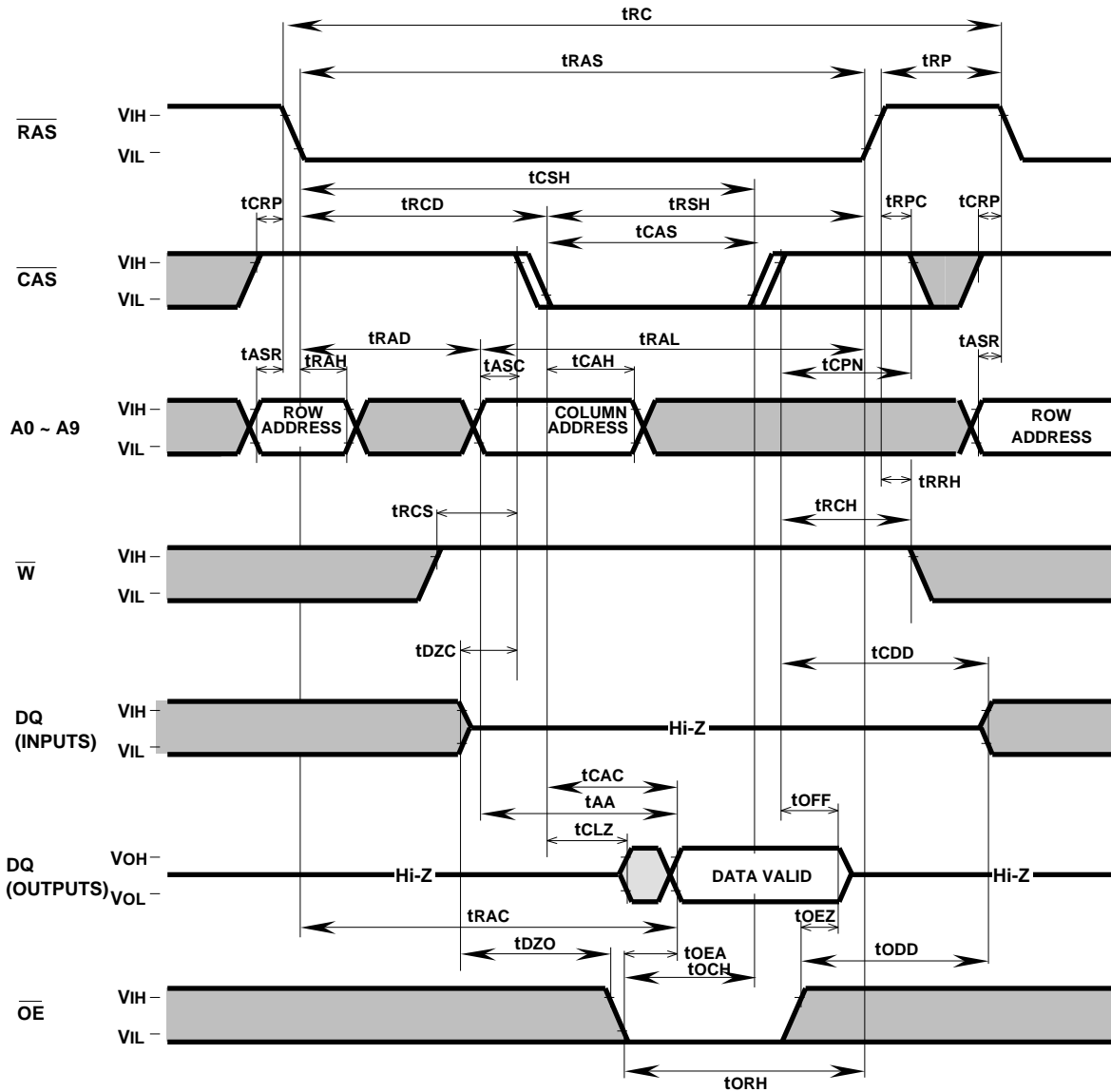
25: tCP (max) is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		-6		-7		
		Min	Max	Min	Max	
tcSR	CAS setup time before RAS low	10		10		ns
tCHR	CAS hold time after RAS low	10		15		ns
trSR	Read setup time before RAS low	10		10		ns
trHR	Read hold time after RAS low	10		15		ns
tcAS	CAS low pulse width	25		30		ns

Note 26: Eight or more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

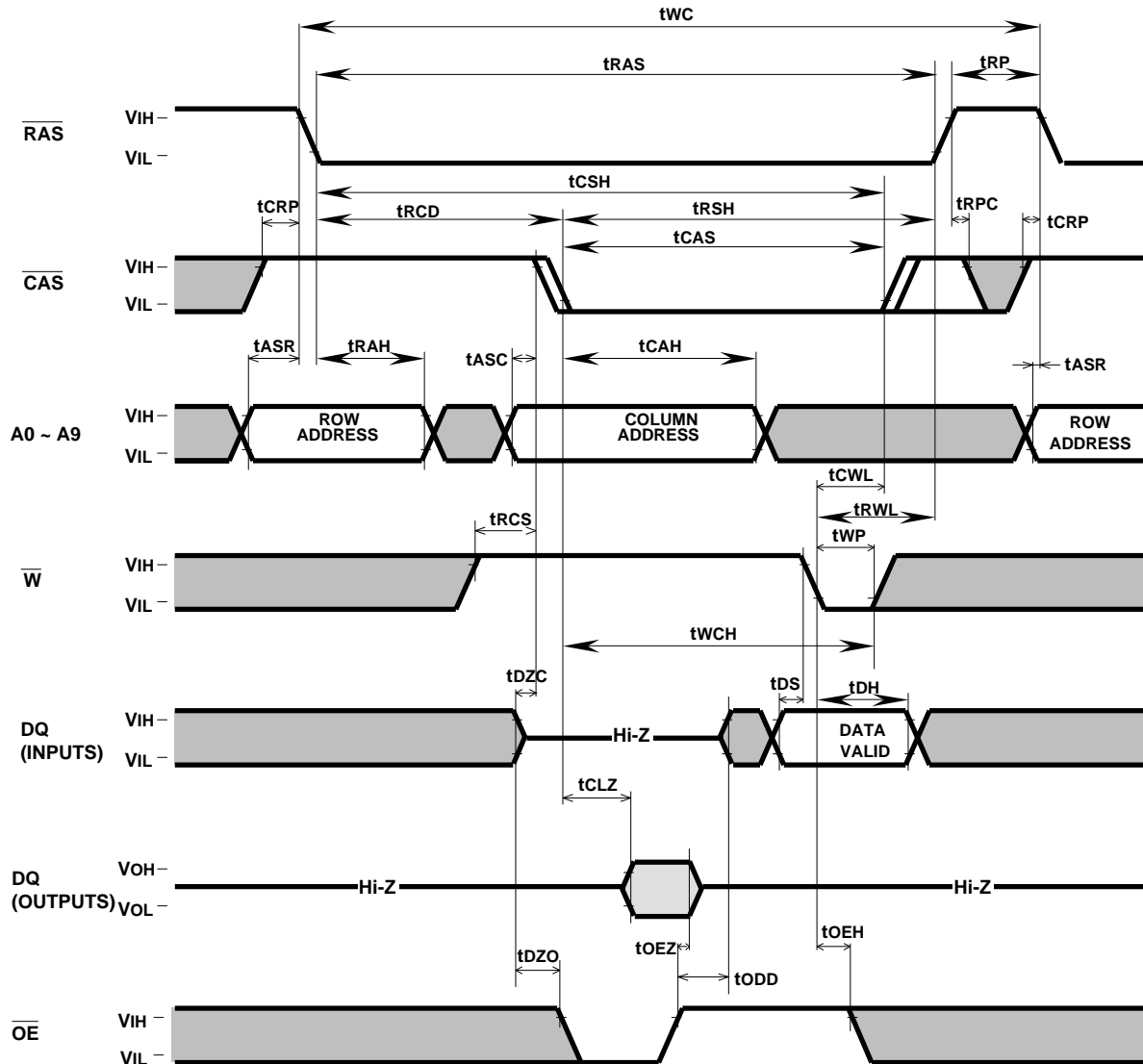
Timing Diagrams (Note 27)
Read Cycle



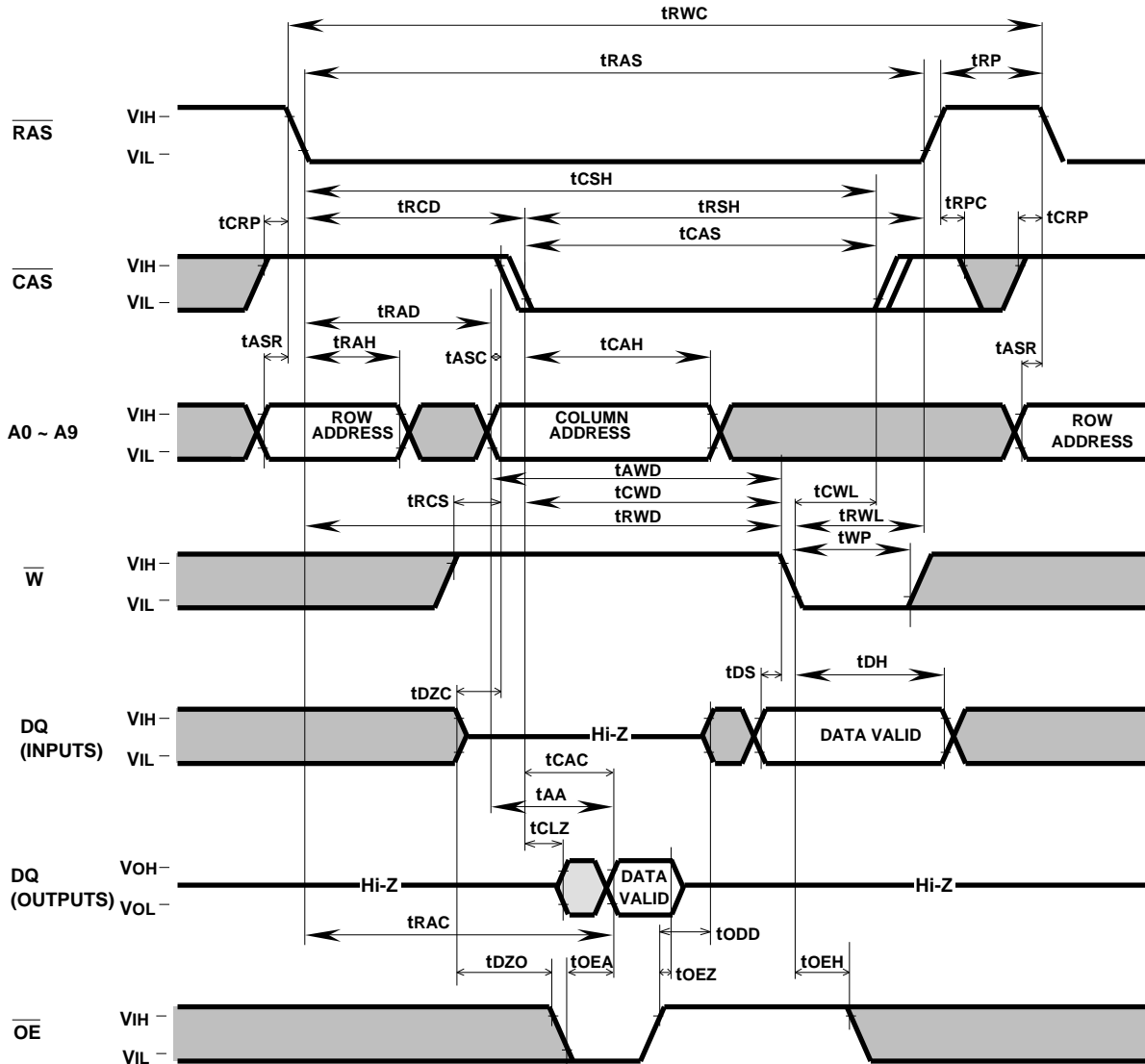
Note 27

- Indicates the don't care input.
VIH(min) VIN VIH(max) or VIL(min) VIN VIL(max)
- Indicates the invalid output.
- Indicates the skew of the four inputs.

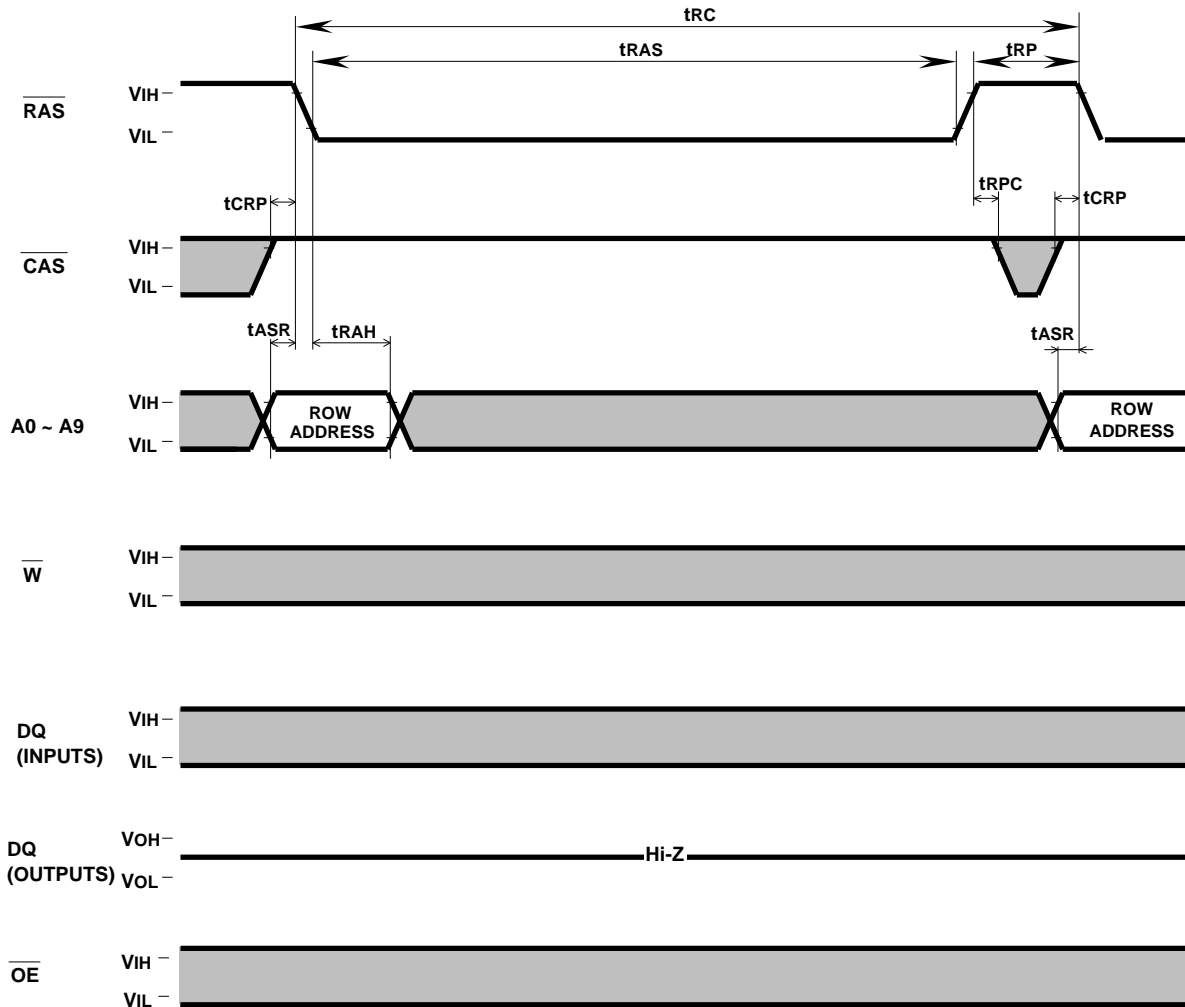
Write Cycle (Delayed write)



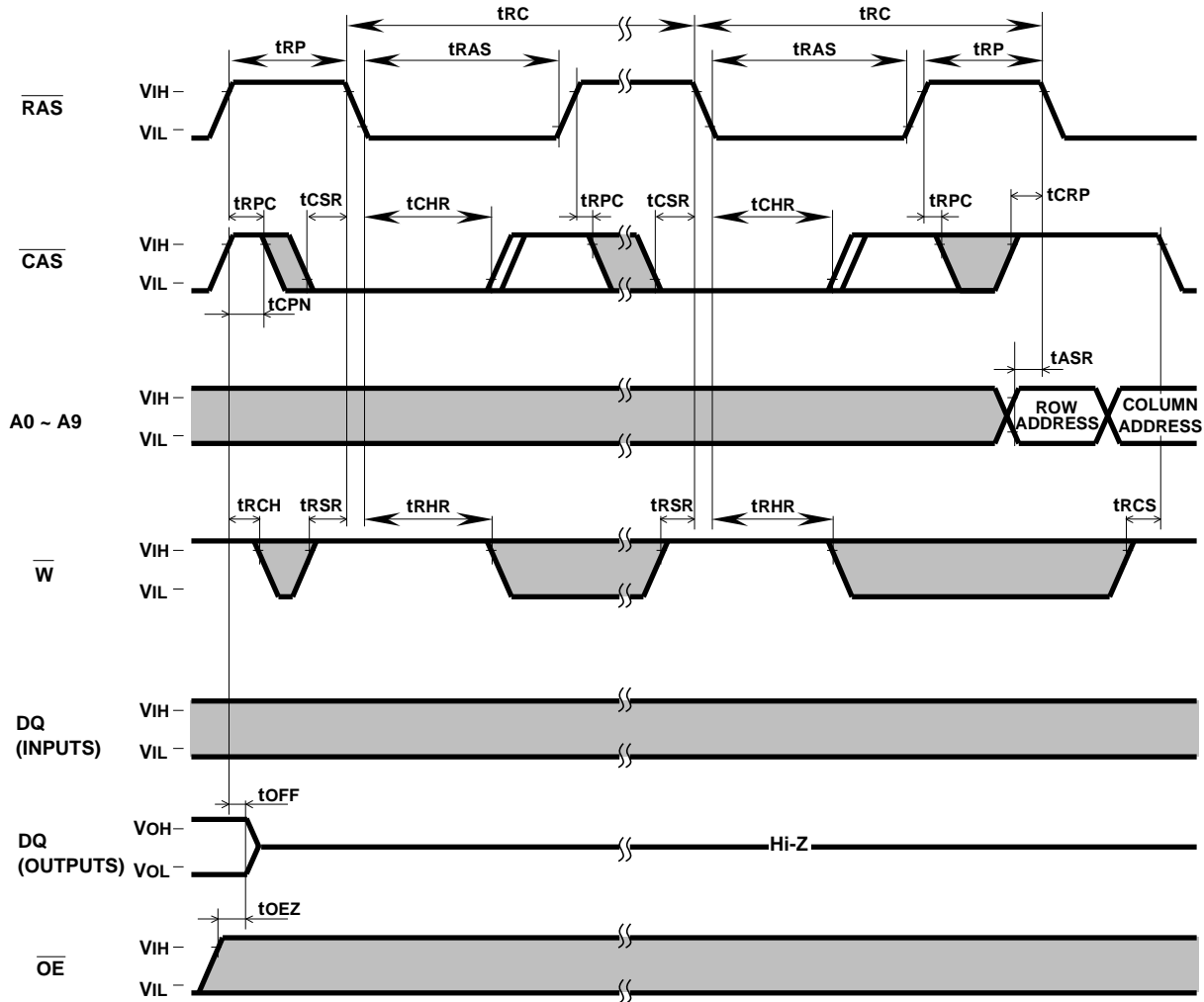
Read-Write, Read-Modify-Write Cycle



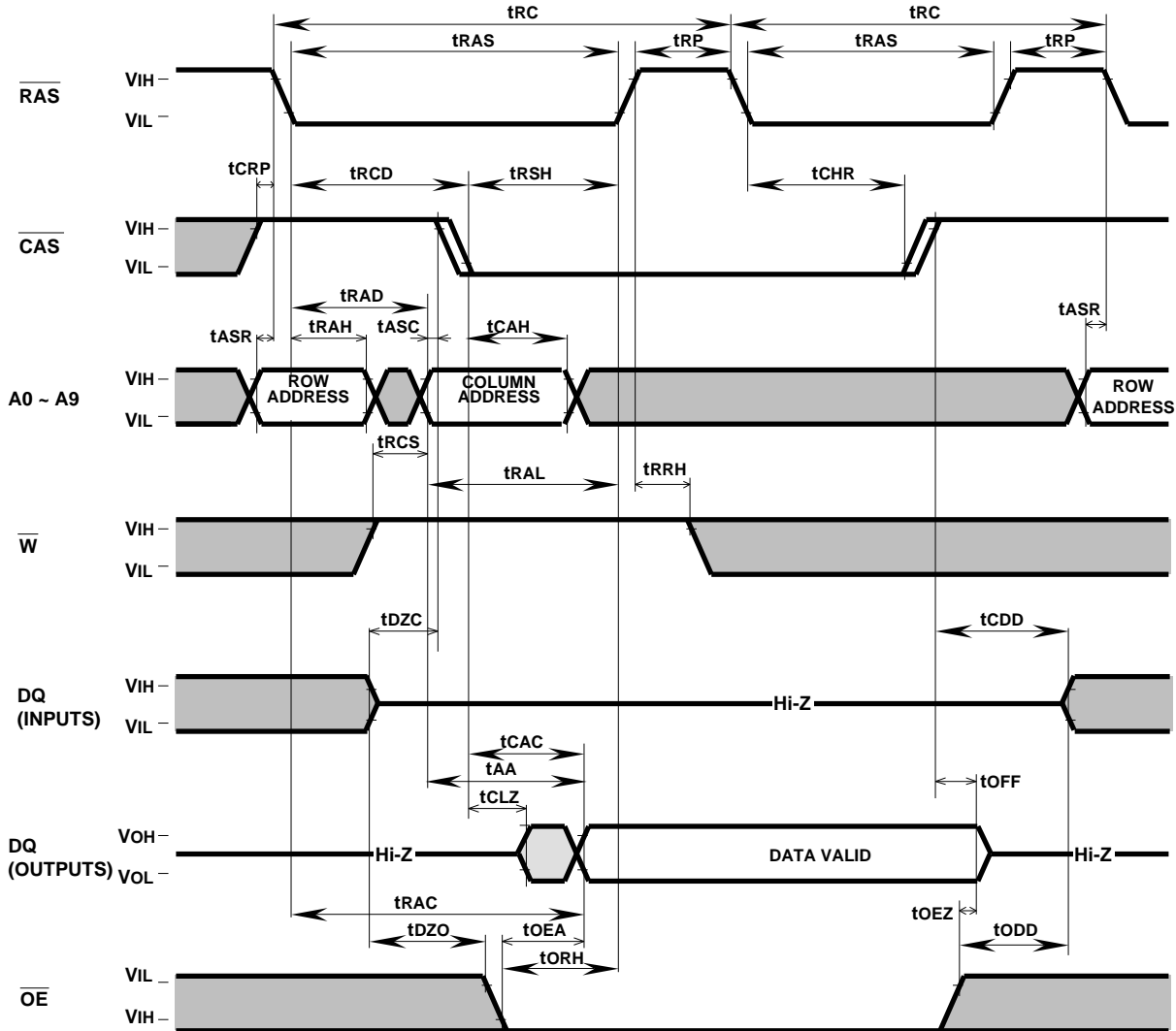
RAS-only Refresh Cycle



CAS before RAS Refresh Cycle

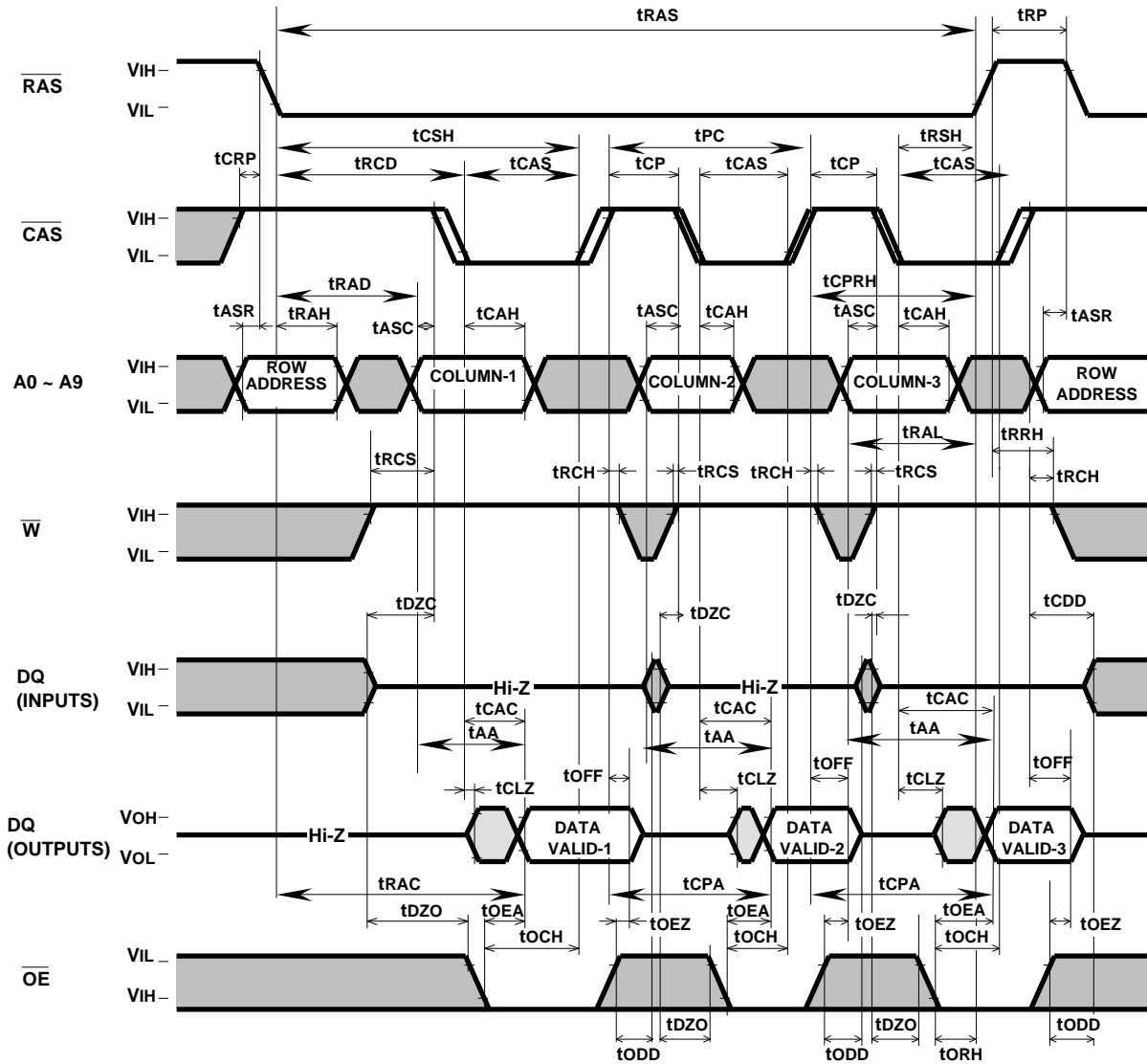


Hidden Refresh Cycle (Read) (Note 28)

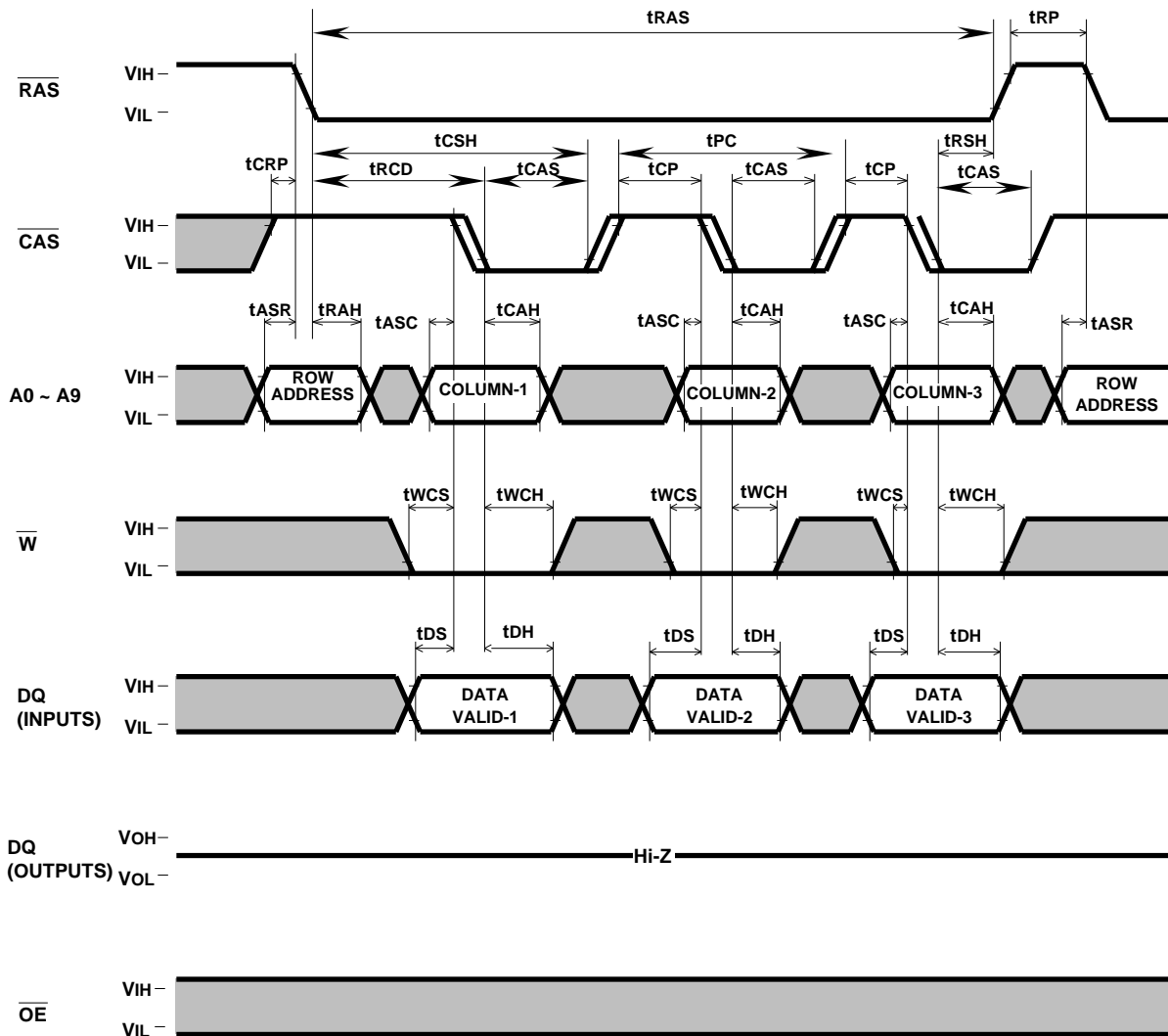


Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

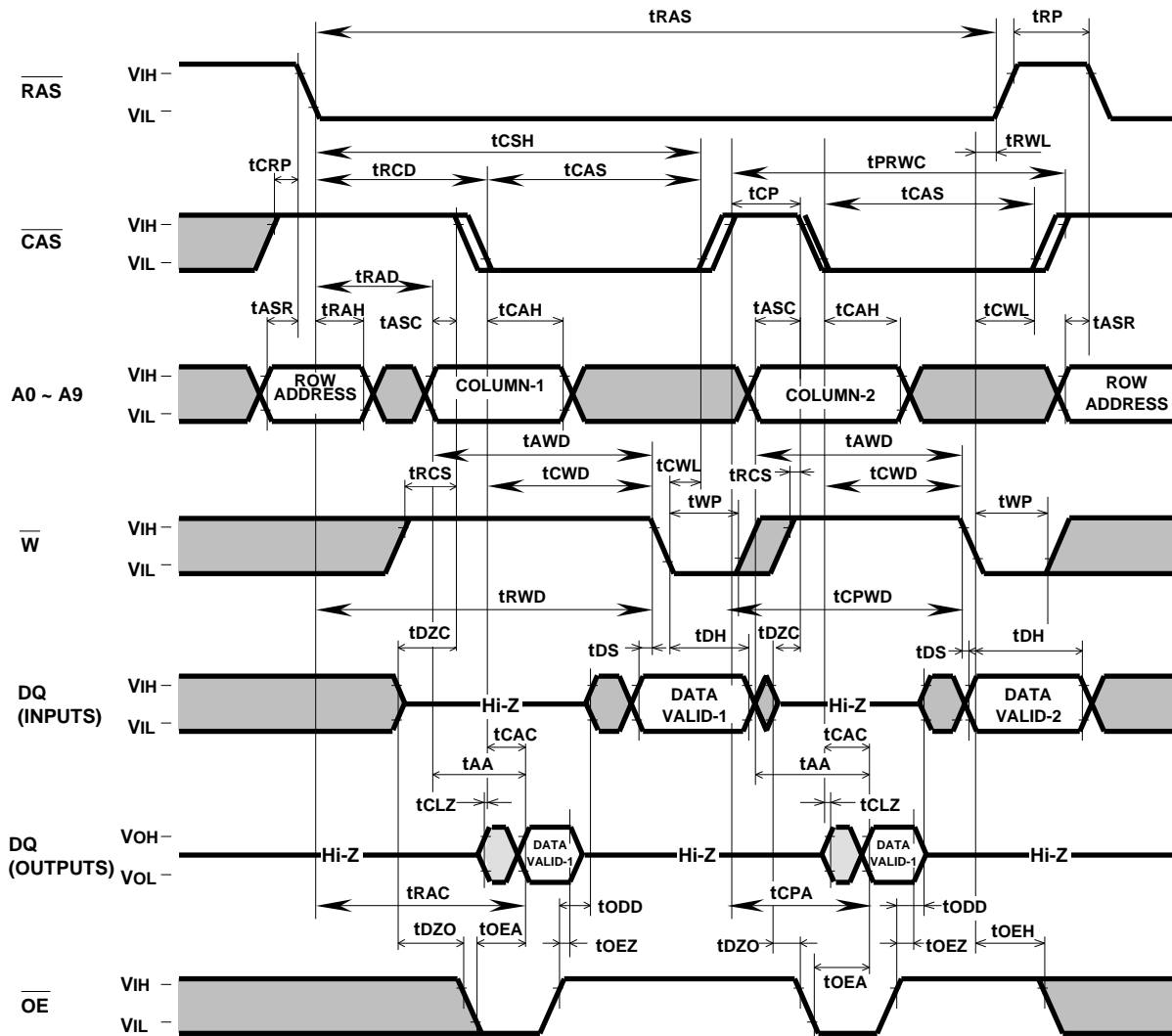
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Read-Write,Read-Modify-Write Cycle



Preliminary Spec.

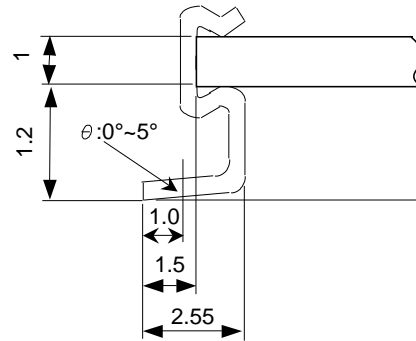
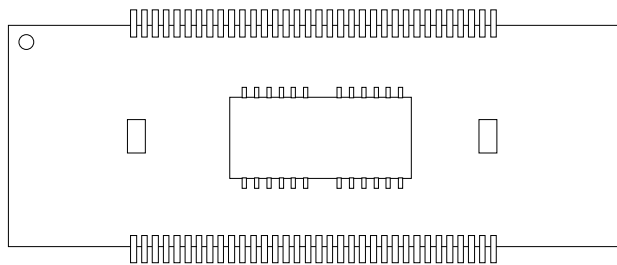
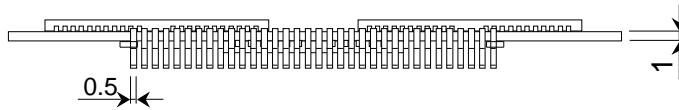
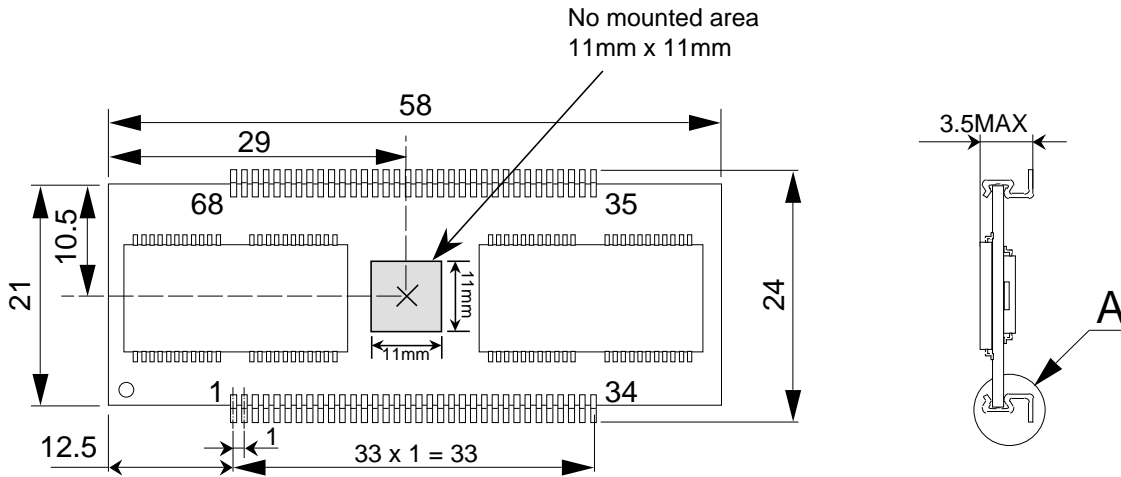
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MH1V36CAM OUTLINE



Detail A