

MH2M365CXJ/CNXJ-5,-6,-7

HYPER PAGE MODE 75497472-BIT (2097152-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH2M365CXJ/CNXJ is 2097152-word x 36-bits dynamic RAM. This consists of four industry standard 1M x 16 dynamic RAMs in SOJ and two industry 1M x 4 dyanmic RAMs in SOJ.

The mounting of SOJ on a single in-line package provides any application where high densities and large quantities of memory are required. This is a socket-type memory module,suitable for easy interchange or addition of modules.

FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH2M365CXJ/CNXJ-5	50	13	25	90	2137
MH2M365CXJ/CNXJ-6	60	15	30	110	1767
MH2M365CXJ/CNXJ-7	70	20	35	130	1537

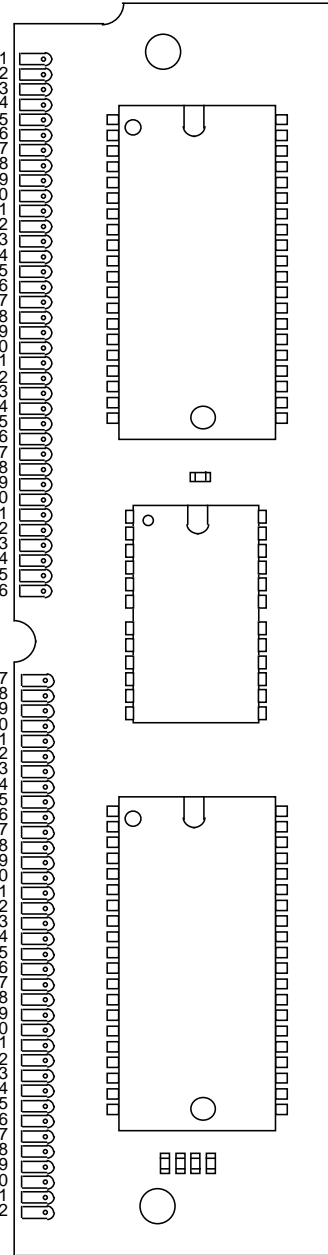
- 72pin single in-line package
- Single 5.0V ± 10% supply
- Low stand-by power dissipation
33mW (Max) ----- CMOS Input level
- Low operating power dissipation
MH2M365CXJ/CNXJ- 5 ----- 2.69W (Max)
MH2M365CXJ/CNXJ- 6 ----- 2.22W (Max)
MH2M365CXJ/CNXJ- 7 ----- 1.92W (Max)
- Hyper-page mode , $\overline{\text{RAS}}$ -only refresh , $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh capabilities
- All inputs and output directly TTL compatible
1024 refresh cycles every 16.4ms (A₀ ~ A₉)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW) [Double side]

1.Vss	37.MP1	1
2.DQ0	38.MP3	2
3.DQ16	39.Vss	3
4.DQ1	40.CAS0	4
5.DQ17	41. $\overline{\text{CAS}}$ 2	5
6.DQ2	42. $\overline{\text{CAS}}$ 3	6
7.DQ18	43. $\overline{\text{CAS}}$ 1	7
8.DQ3	44.RAS0	8
11.NC	45.RAS1	9
10.Vcc	46.NC	10
11.NC	47.W	11
12.A0	48.NC	12
13.A1	49.DQ8	13
14.A2	50.DQ24	14
15.A3	51.DQ9	15
16.A4	52.DQ25	16
17.A5	53.DQ10	17
18.A6	54.DQ26	18
19.NC	55.DQ11	19
20.DQ4	56.DQ27	20
21.DQ20	57.DQ12	21
22.DQ5	58.DQ28	22
23.DQ21	59.Vcc	23
24.DQ6	60.DQ29	24
25.DQ22	61.DQ13	25
26.DQ7	62.DQ30	26
27.DQ23	63.DQ14	27
28.A7	64.DQ31	28
29.NC	65.DQ15	29
30.Vcc	66.NC	30
31.A8	67.PD1	31
32.A9	68.PD2	32
33. $\overline{\text{RAS}}$ 3	69.PD3	33
34. $\overline{\text{RAS}}$ 2	70.PD4	34
35.MP2	71.NC	35
36.MP0	72.Vss	36



Outline 72N9J-C

	- 5	- 6	- 7
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	Vss	NC	Vss
PD4	Vss	NC	NC

NC: NO CONNECTION

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FUNCTION

in addition to normal read, write, a number of other functions, e.g., hyper page mode, RAS only refresh,

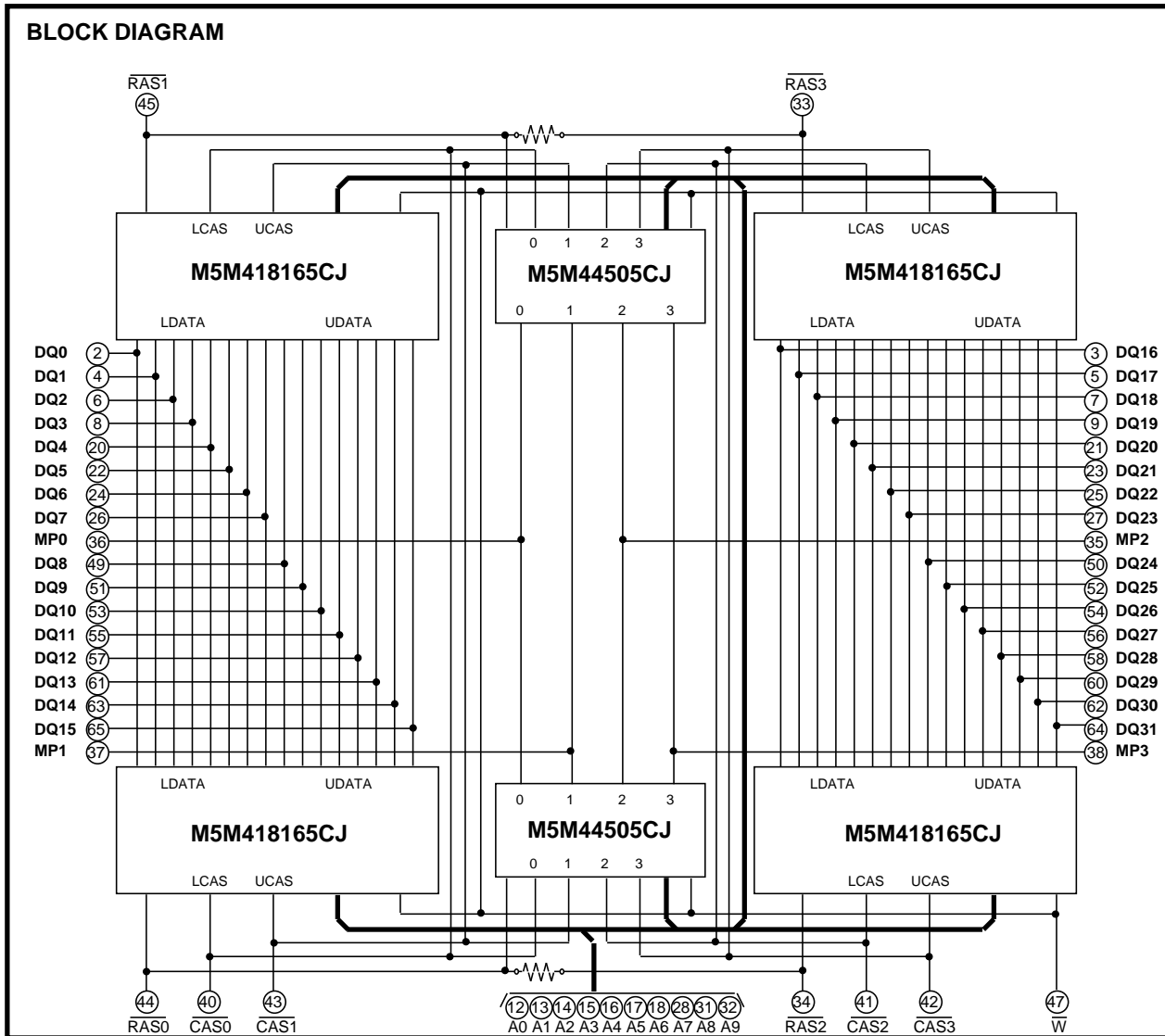
The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	RAS	CAS	W	Row address	Column address	Input	Output
Read	ACT	ACT	NAC	APD	APD	OPN	VLD
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN
RAS-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN
Hidden refresh	ACT	ACT	NAC	APD	DNC	OPN	VLD
CAS before RAS refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to V _{SS}	-1 ~ 7	V
V _I	Input voltage		-1 ~ 7	V
V _O	Output voltage		-1 ~ 7	V
I _O	Output current		50	mA
P _d	Power dissipation	T _a =25°C	6000	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{stg}	Storage temperature		-40 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0 ~ 70 °C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	High-level input voltage, all inputs	2.4		6.0	V
V _{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to V_{SS}

ELECTRICAL CHARACTERISTICS (T_a=0 ~ 70°C, V_{CC}=5.0V ± 10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{OH}	High-level output voltage	I _{OH} =-5.0mA	2.4		V _{CC}	V
V _{OL}	Low-level output voltage	I _{OL} =4.2mA	0		0.4	V
I _{OZ}	Off-state output current	Q floating 0V V _{OUT} 5.5V	-20		20	μA
I _I	Input current	0V V _{IN} 6 V, Other inputs pins=0V	-60		60	μA
I _{CC1} (AV)	Average supply current from V _{CC} operating (Note 3,4,5)	MH2M365C -5	R _{AS} , C _{AS} cycling t _{RC} =t _{WC} =min. output open		491	mA
		MH2M365C -6			406	
		MH2M365C -7			351	
I _{CC2}	Supply current from V _{CC} , stand-by (Note 6)	R _{AS} =C _{AS} =V _{IH} , output open			12	mA
		R _{AS} =C _{AS} V _{CC} -0.2 V			6	
I _{CC3} (AV)	Average supply current from V _{CC} refreshing (Note 3,5)	MH2M365C -5	R _{AS} cycling, C _{AS} =V _{IH} t _{RC} =min. output open		491	mA
		MH2M365C -6			406	
		MH2M365C -7			351	
I _{CC4} (AV)	Average supply current from V _{CC} Hyper-Page-Mode (Note 3,4,5)	MH2M365C -5	R _{AS} =V _{IL} , C _{AS} cycling t _{RC} =min. output open		461	mA
		MH2M365C -6			366	
		MH2M365C -7			311	
I _{CC6} (AV)	Average supply current from V _{CC} C _{AS} before R _{AS} refresh mode (Note 3)	MH2M365C -5	C _{AS} before R _{AS} refresh cycling t _{RC} =min. output open		471	mA
		MH2M365C -6			391	
		MH2M365C -7			341	

Note 2: Current flowing into an IC is positive, out is negative.

3: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while R_{AS}=V_{IL} and C_{AS}=V_{IH}.

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CAPACITANCE (Ta=0 ~ 70 °C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _{i(A)}	Input capacitance, address inputs	V _i =V _{ss} f=1MHz V _i =25mVrms			45	pF
C _{i(W)}	Input capacitance, write control input				57	pF
C _{i(RAS)}	Input capacitance, RAS input				36	pF
C _{i(CAS)}	Input capacitance, CAS input				43	pF
C _{i/O}	Input/Output capacitance, data ports				29	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70 °C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		MH2M365C -5		MH2M365C -6		MH2M365C -7		
		Min	Max	Min	Max	Min	Max	
t _{CAC}	Access time from CAS (Note 7,8)		13		15		20	ns
t _{RAC}	Access time from RAS (Note 7,9)		50		60		70	ns
t _{AA}	Column address access time (Note 7,10)		25		30		35	ns
t _{CPA}	Access time from CAS precharge (Note 7,11)		30		35		40	ns
t _{OH}	Output hold time from CAS	5		5		5		ns
t _{OHR}	Output hold time from RAS (Note 13)	5		5		5		ns
t _{CLZ}	Output low impedance time from CAS low (Note 7)	5		5		5		ns
t _{WEZ}	Output disable time after WE high (Note 12)		13		15		20	ns
t _{OFF}	Output disable time after CAS high (Note 12,13)		13		15		20	ns
t _{REZ}	Output disable time after RAS high (Note 12,13)		13		15		20	ns

Note 6: An initial pause of 500µs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause . And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 16.4 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V_{OH}=2.4V(I_{OH}=-5mA) / V_{OL}=0.4V(I_{OL}=-4.2mA) load 100pF.

The reference levels for measuring of output signal are 2.0V(V_{OH}) and 0.8V(V_{OL}).

8: Assumes that t_{RCD} t_{RCD(max)} and t_{ASC} t_{ASC(max)} and t_{CP} t_{CP(max)}.

9: Assumes that t_{RCD} t_{RCD(max)} and t_{RAD} t_{RAD(max)}. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that t_{RAD} t_{RAD(max)} and t_{ASC} t_{ASC(max)}.

11: Assumes that t_{CP} t_{CP(max)} and t_{ASC} t_{ASC(max)}.

12: t_{WEZ(max)}, t_{OFF(max)} and t_{REZ(max)} defines the time at which the output achieves the high impedance state (I_{out} I ± 10 µA) and is not reference to V_{OH(min)} or V_{OL(max)}.

13: Output is disabled after both RAS and CAS go to high.

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TIMING REQUIREMENTS (For Read, Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc = 5V ± 10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		MH2M365C -5		MH2M365C -6		MH2M365C -7		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tRP	RAS high pulse width	30		40		50		ns
tRCD	Delay time, RAS low to CAS low (Note16)	18	37	20	45	20	50	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	8		10		10		ns
tRAD	Column address delay time from RAS low (Note17)	13	25	15	30	15	35	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note18)	0	10	0	13	0	13	ns
tRAH	Row address hold time after RAS low	8		10		10		ns
tCAH	Column address hold time after CAS low	8		10		10		ns
tDZC	Delay time, data to CAS low (Note19)	0		0		0		ns
tRDD	Delay time, RAS high to data (Note20)	13		15		20		ns
tCDD	Delay time, CAS high to data (Note20)	13		15		20		ns
tT	Transition time (Note21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed $t_r = 3ns$.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC} . If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{TAA} .

17: $t_{RAD(max)}$ is specified as a reference point only. If t_{RAD} , $t_{RAD(max)}$ and t_{ASC} , $t_{ASC(max)}$, access time is controlled exclusively by t_{TAA} .

18: $t_{ASC(max)}$ is specified as a reference point only. If t_{RCD} , $t_{RCD(max)}$ and t_{ASC} , $t_{ASC(max)}$, access time is controlled exclusively by t_{CAC} .

19: t_{DZC} must be satisfied.

20: Either t_{RDD} or t_{CDD} must be satisfied.

21: t_r is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		MH2M365C -5		MH2M365C -6		MH2M365C -7		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	90		110		130		ns
tRAS	RAS low pulse width	50	10000	60	10000	70	10000	ns
tCAS	CAS low pulse width	8	10000	10	10000	13	10000	ns
tCSH	CAS hold time after RAS low	40		48		55		ns
tRSH	RAS hold time after CAS low	13		15		20		ns
tRCS	Read Setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 22)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 22)	10		10		10		ns
tRAL	Column address to RAS hold time	25		30		35		ns
tCAL	Column address to CAS hold time	13		18		23		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

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Write Cycle (Early Write)

Symbol	Parameter	Limits						Unit
		MH2M365C -5		MH2M365C -6		MH2M365C -7		
		Min	Max	Min	Max	Min	Max	
t _{WC}	Write cycle time	90		110		130		ns
t _{RAS}	RAS low pulse width	50	10000	60	10000	70	10000	ns
t _{CAS}	CAS low pulse width	8	10000	10	10000	13	10000	ns
t _{CSH}	CAS hold time after RAS low	40		48		55		ns
t _{RSH}	RAS hold time after CAS low	13		15		20		ns
t _{WCS}	Write setup time before CAS low	0		0		0		ns
t _{WCH}	Write hold time after CAS low	8		10		13		ns
t _{WP}	Write pulse width	8		10		13		ns
t _{DS}	Data setup time before CAS low or W low	0		0		0		ns
t _{DH}	Data hold time after CAS low or W low	8		10		13		ns

Hyper page Mode Cycle (Read, Early Write, Hi-Z control by \overline{W}) (Note 25)

Symbol	Parameter	Limits						Unit
		MH2M365C -5		MH2M365C -6		MH2M365C -7		
		Min	Max	Min	Max	Min	Max	
t _{HPC}	Hyper page mode read/write cycle time	20		25		30		ns
t _{DOH}	Output hold time from \overline{CAS} low	5		5		5		ns
t _{RAS}	RAS low pulse width for read write cycle (Note24)	65	100000	77	100000	92	100000	ns
t _{CP}	CAS high pulse width (Note25)	8	13	10	16	13	16	ns
t _{CPRH}	RAS hold time after CAS precharge	30		35		40		ns
t _{CHOL}	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
t _{WPE}	\overline{W} Pulse Width (Hi-Z control)	7		7		7		ns

Note 23: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

24: t_{RAS(min)} is specified as two cycles of CAS input are performed.

25: t_{CP(max)} is specified as a reference point only.

CAS before RAS Refresh Cycle (Note 26)

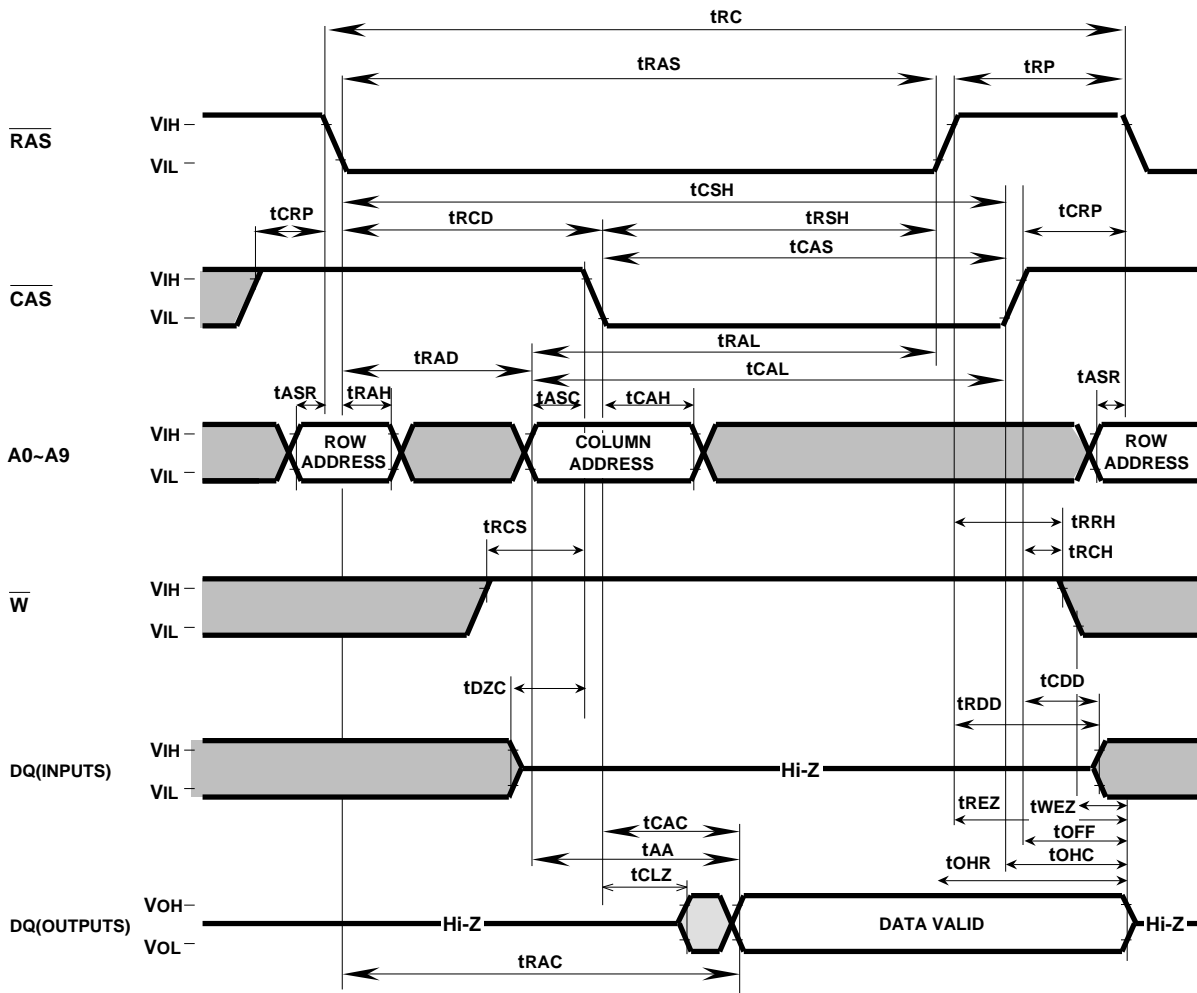
Symbol	Parameter	Limits						Unit
		MH2M365C -5		MH2M365C -6		MH2M365C -7		
		Min	Max	Min	Max	Min	Max	
t _{CSR}	CAS setup time before RAS low	5		5		5		ns
t _{CHR}	CAS hold time after RAS low	10		10		15		ns

Note 26: Eight or more \overline{CAS} before \overline{RAS} cycles instead of eight \overline{RAS} cycles are necessary for proper operation of \overline{CAS} before \overline{RAS} refresh mode.

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Timing Diagrams (Note 27) Read Cycle



Note 27

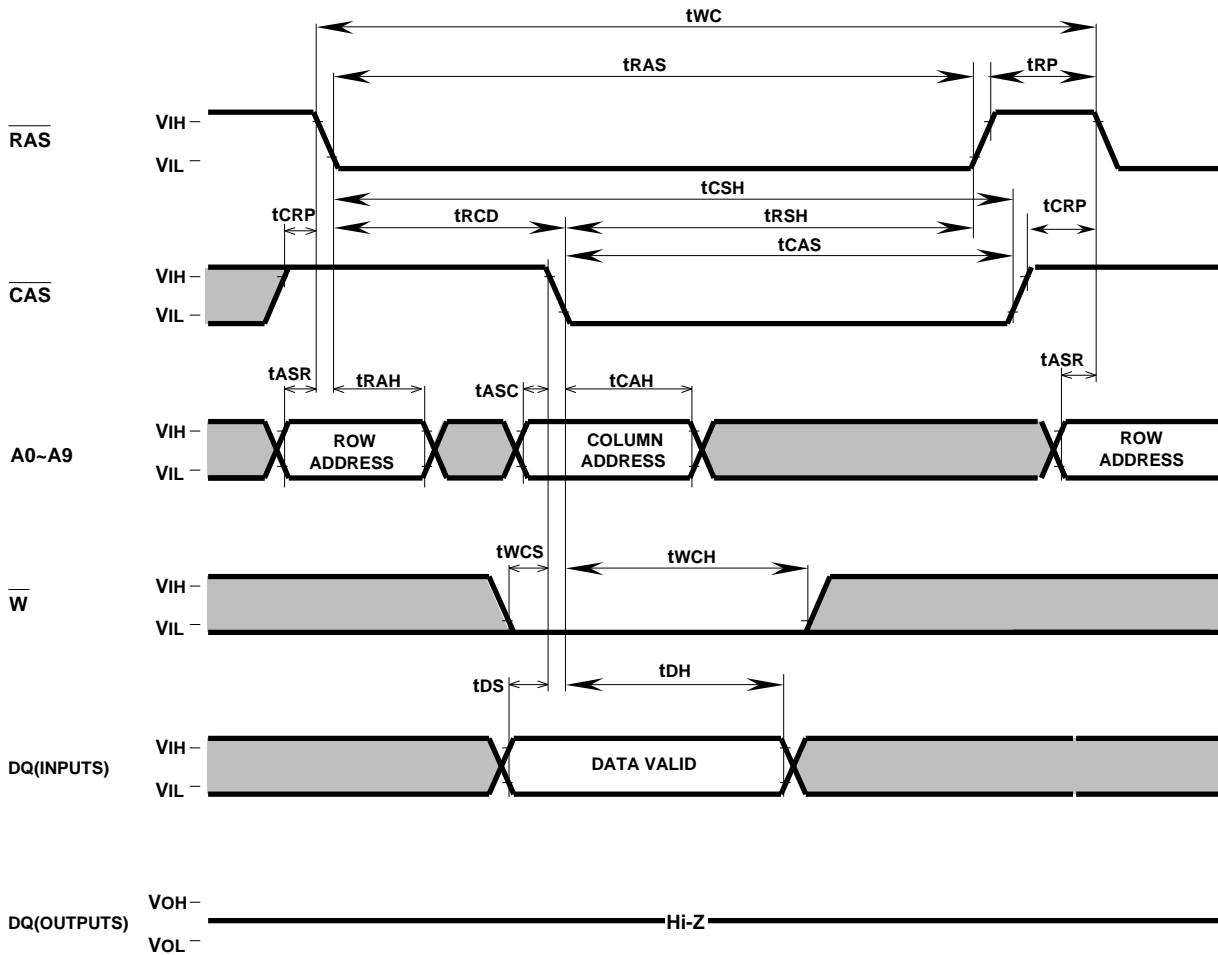


Indicates the don't care input.
 $V_{IH(min)}$ V_{IN} $V_{IH(max)}$ or
 $V_{IL(min)}$ V_{IN} $V_{IL(max)}$
 Indicates the invalid output.

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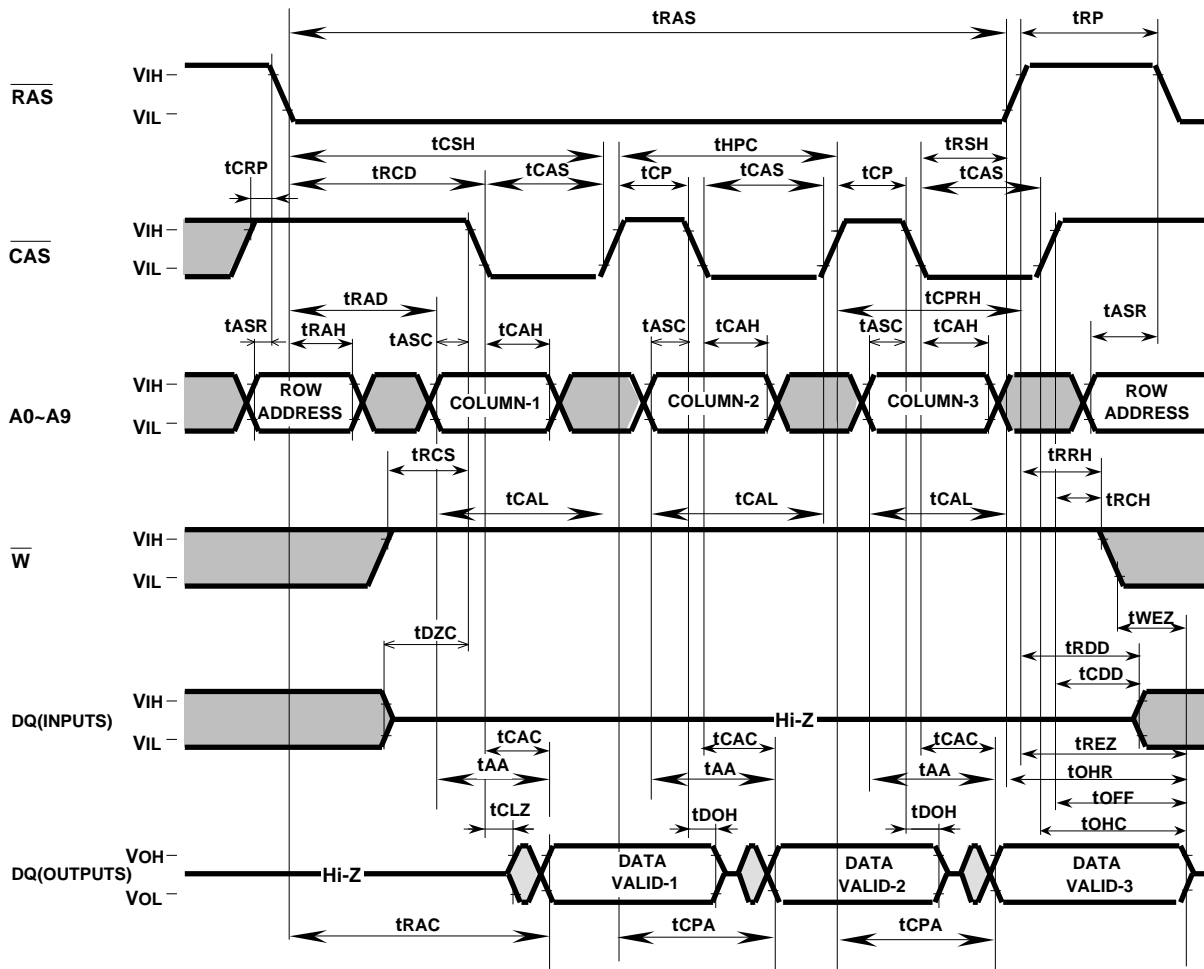
Early Write Cycle



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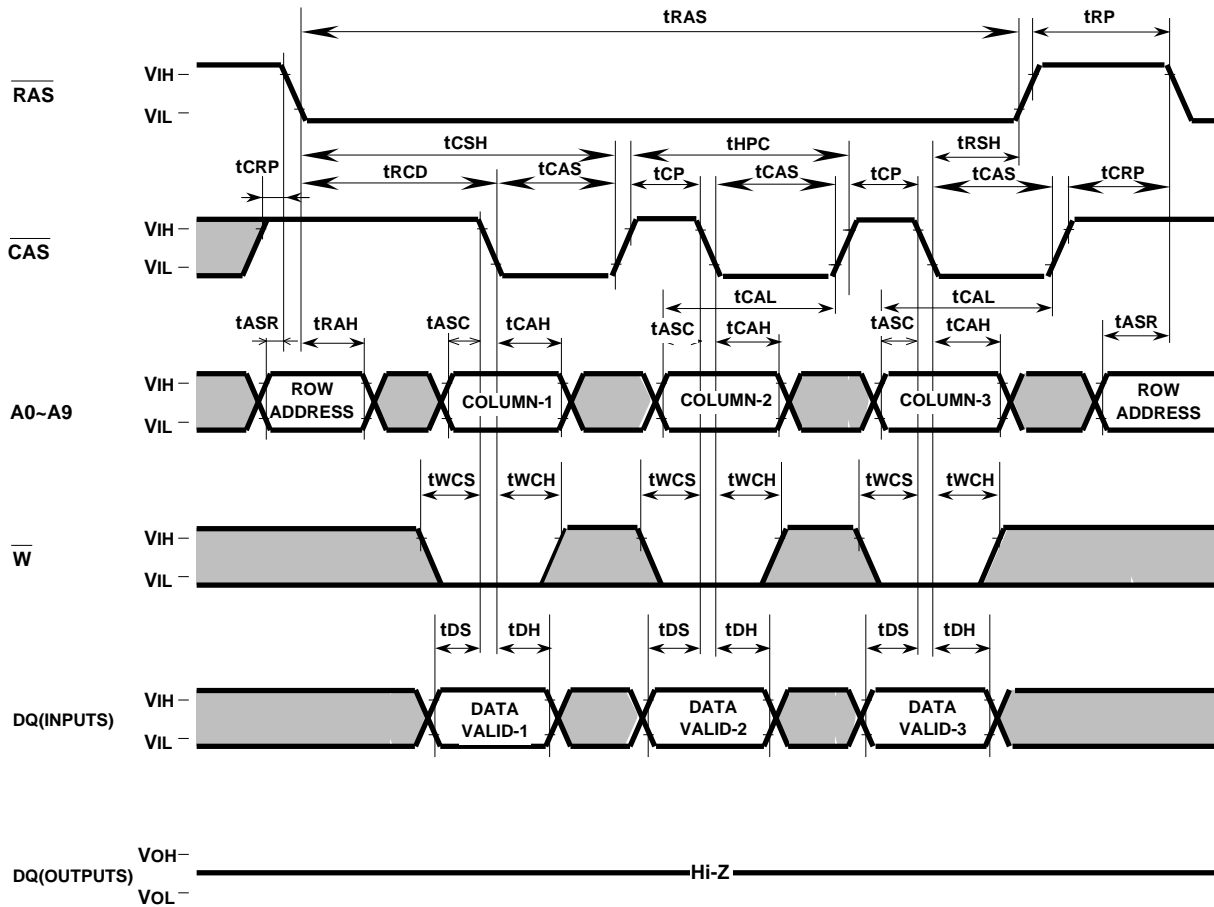
Hyper Page Mode Read Cycle



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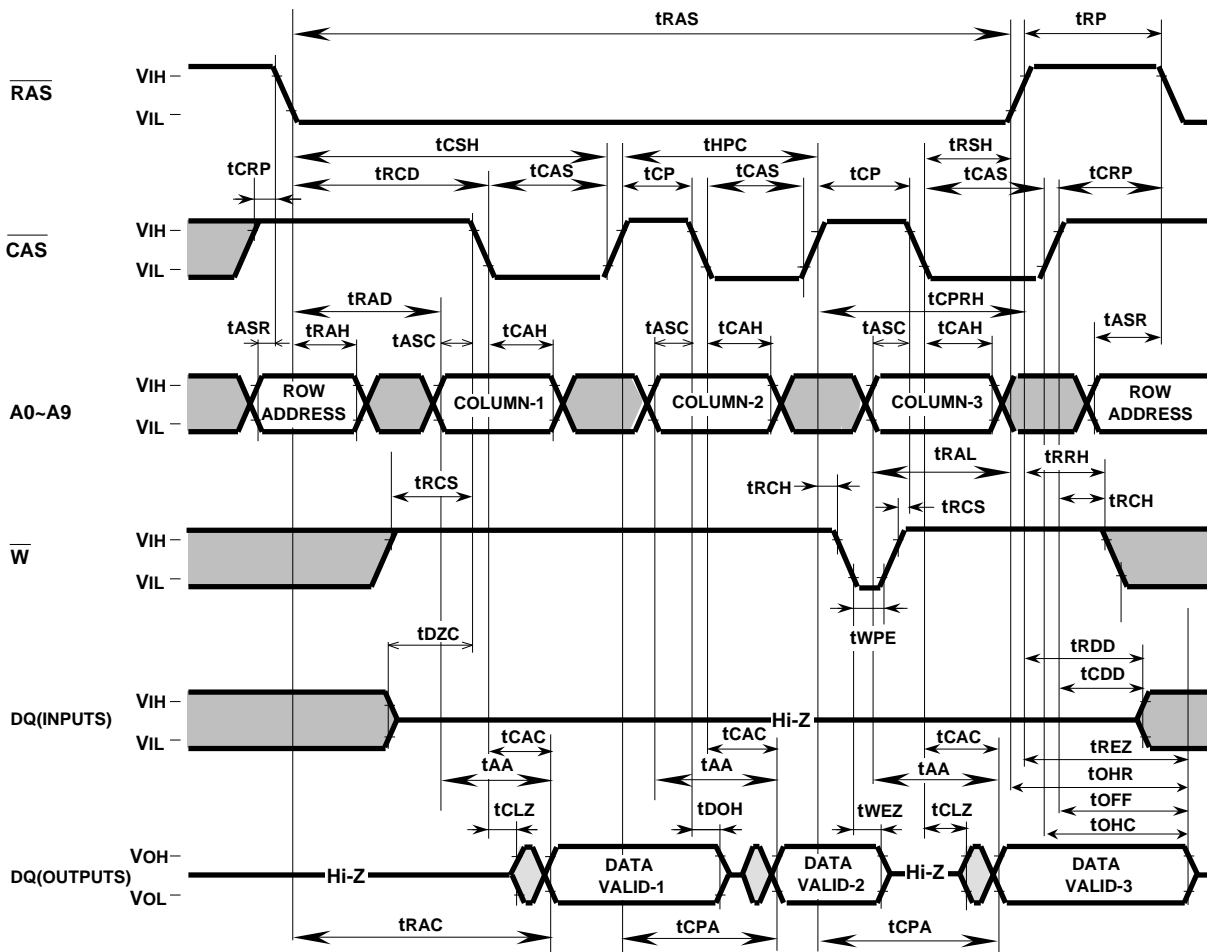
Hyper Page Mode Early Write Cycle



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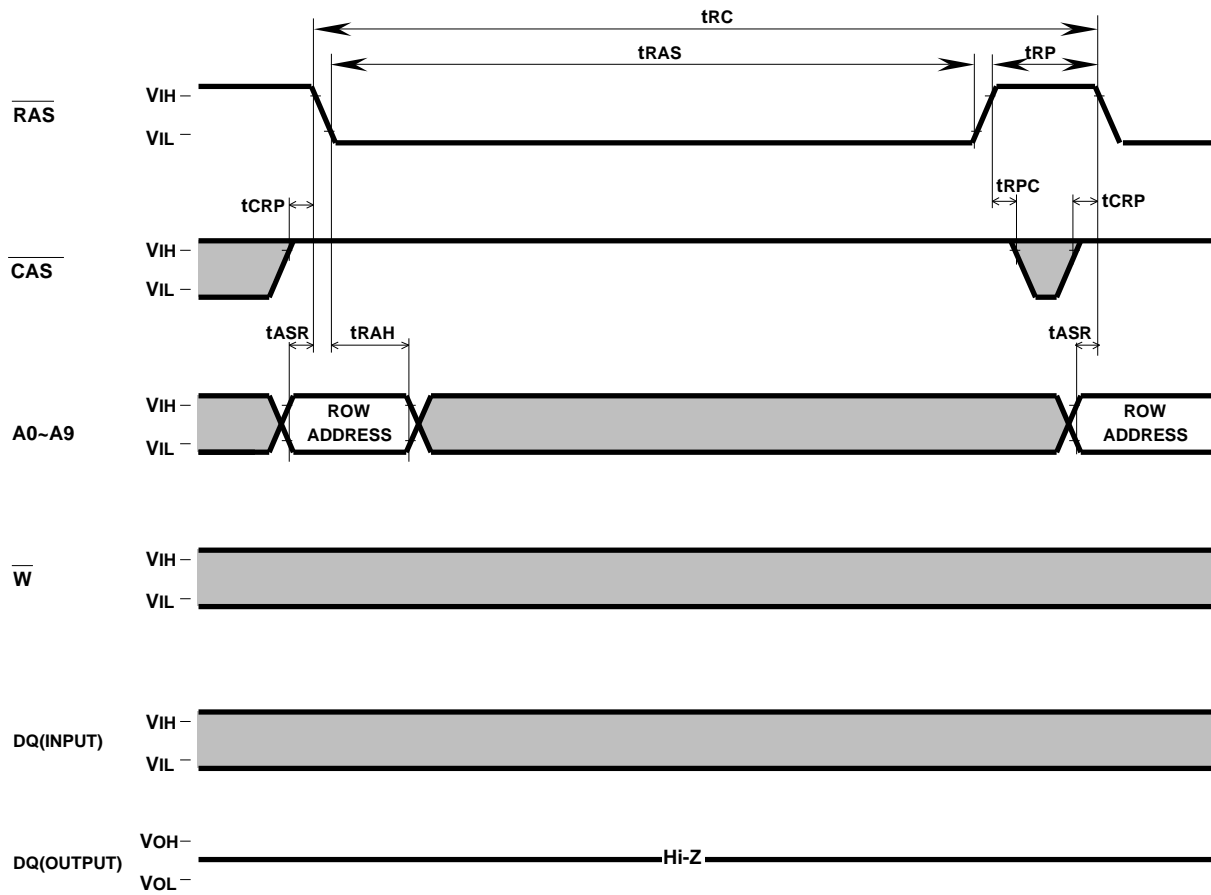
Hyper Page Mode Read Cycle (Hi-Z control by \overline{W})



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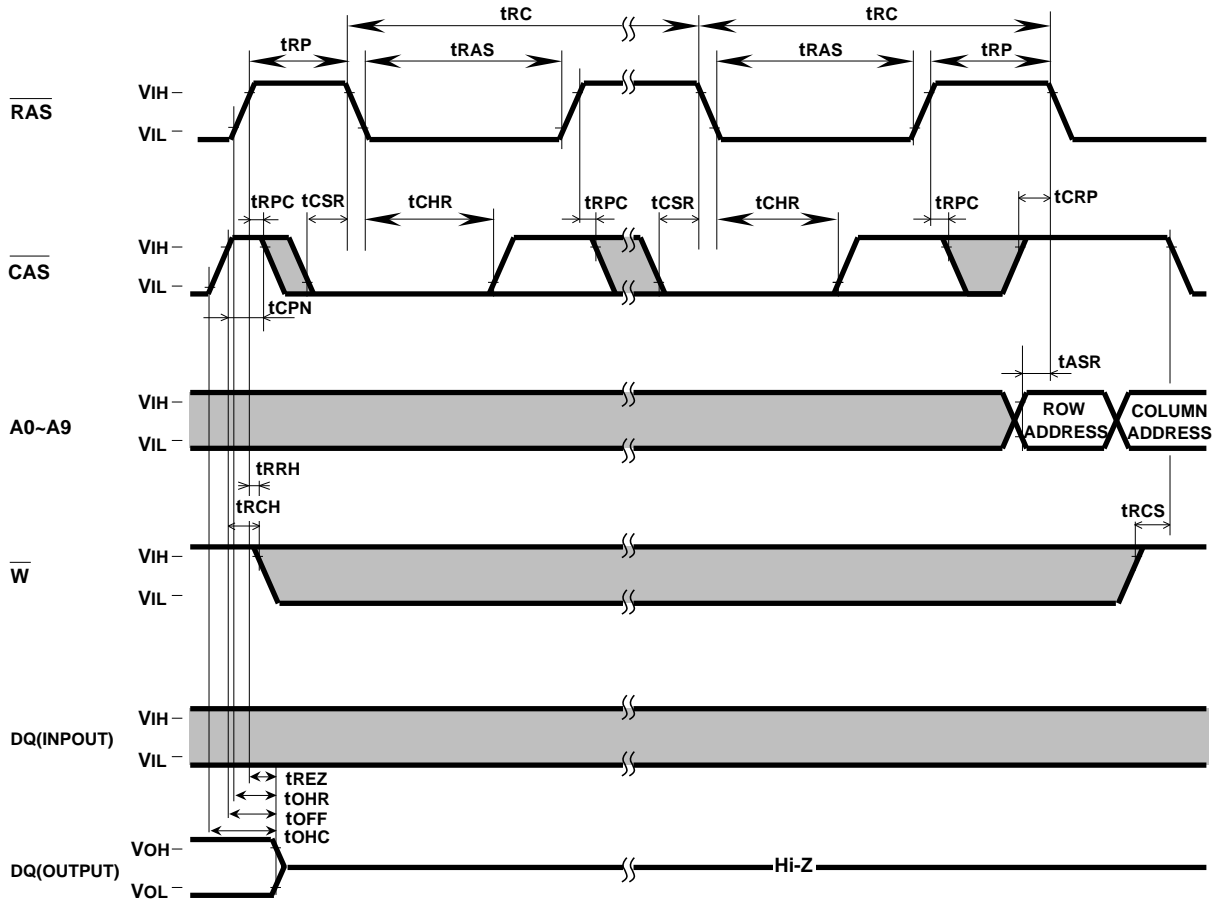
RAS-only Refresh Cycle



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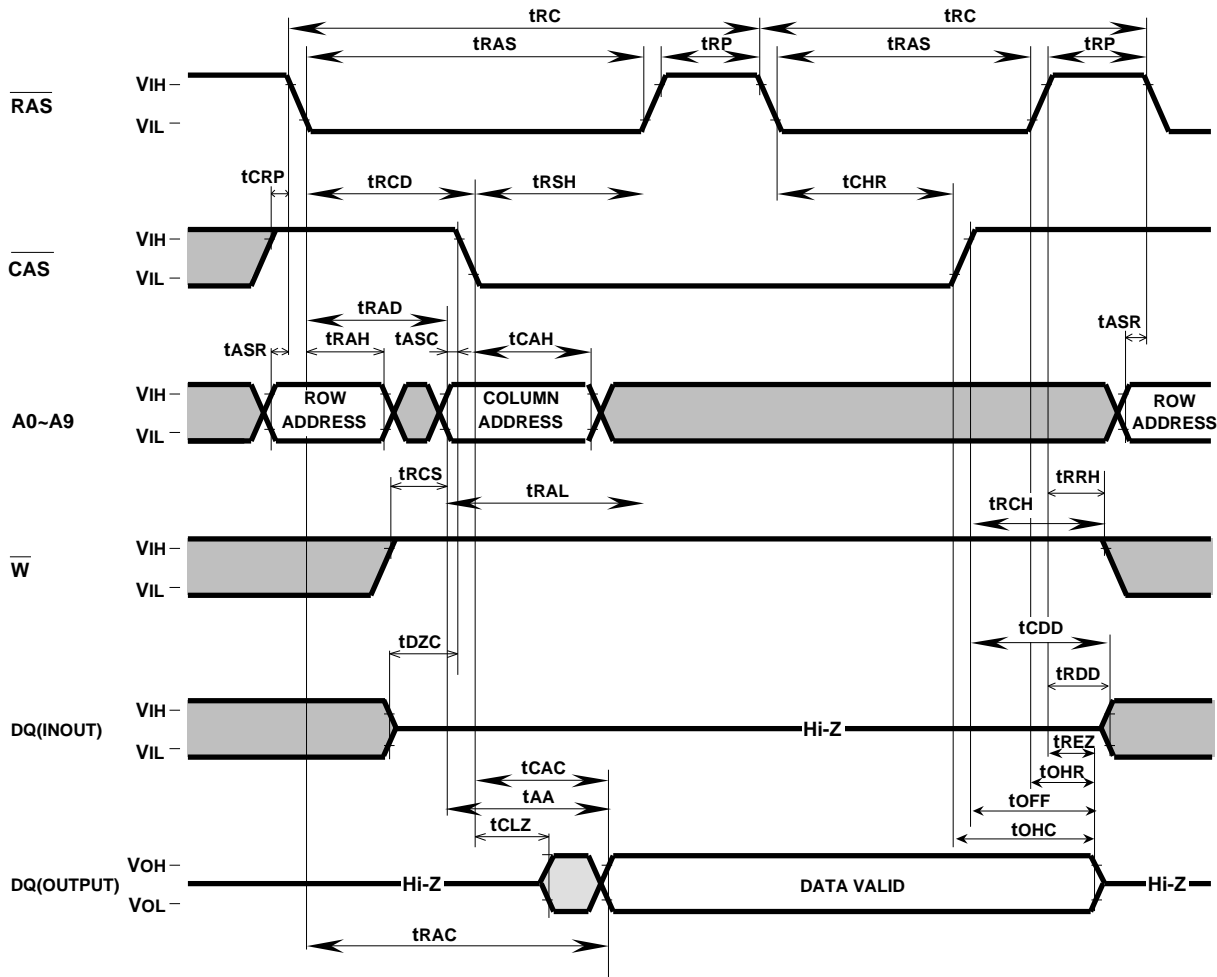
CAS before RAS Refresh Cycle



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Hidden Refresh Cycle (Read) (Note 28)



Note 28: Early write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

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72pin DRAM Module Outline

