FEDL9042-01
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OKI Semiconductor

ML9042-xx

DOT MATRIX LCD CONTROLLER DRIVER

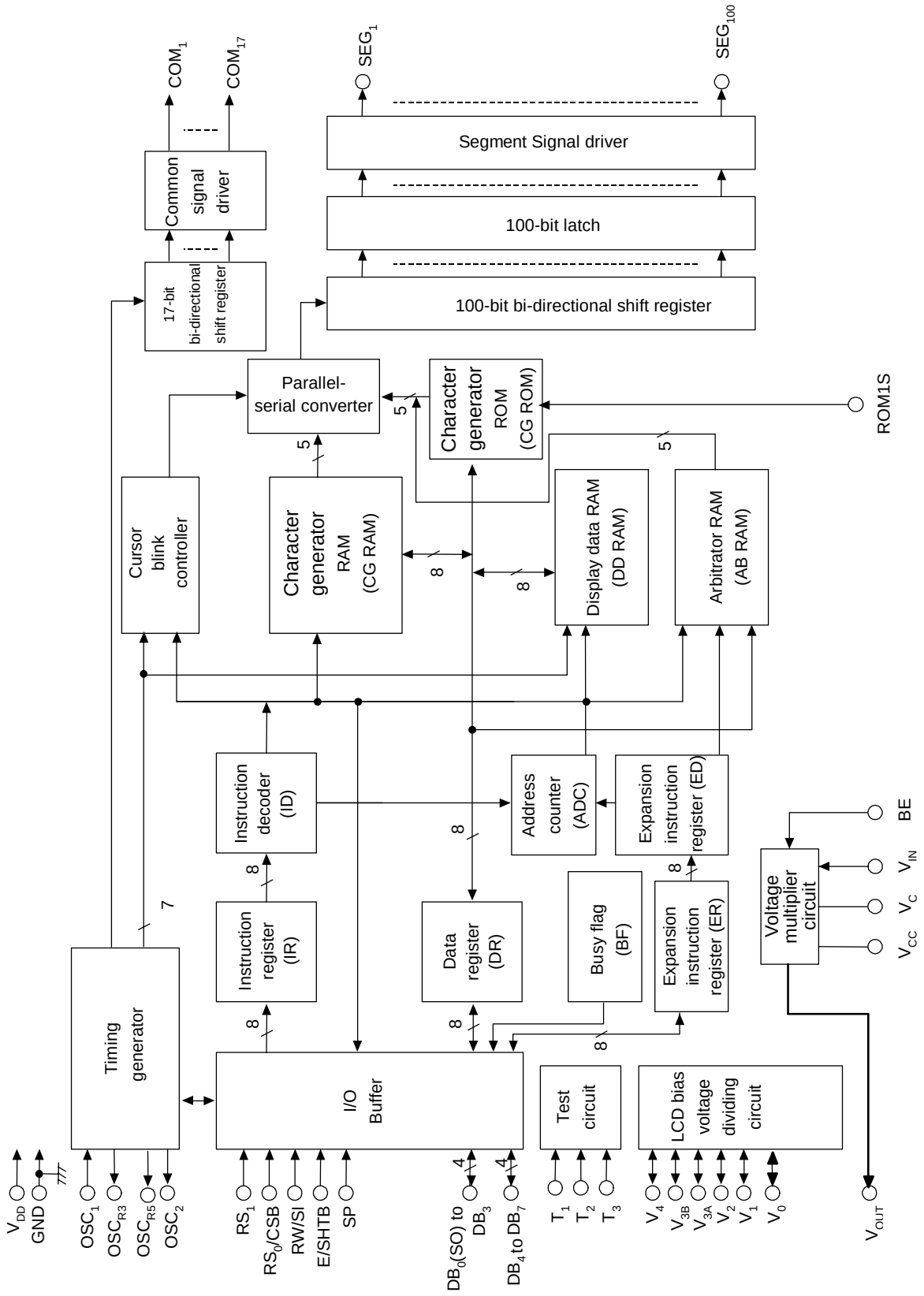
GENERAL DESCRIPTION

The ML9042 used in combination with an 8-bit or 4-bit microcontroller controls the operation of a character type dot matrix LCD.

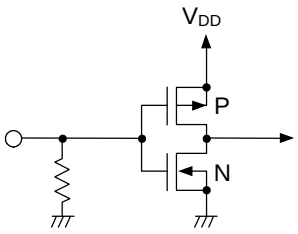
FEATURES

- Easy interfacing with an 8-bit or 4-bit microcontroller
- Switchable between serial and parallel interfaces
- Dot-matrix LCD controller driver for a 5 × 8 dot font
- Built-in circuit allowing automatic resetting at power-on
- Built-in 17 common signal drivers and 100 segment signal drivers
- Two built-in character generator ROMs each capable of generating 240 characters (5 × 8 dots)
  The character generator ROM can be selected by bank switching (ROM1S) pin.
- Creation of character patterns by programming: up to 8 character patterns (5 × 8 dots)
- Built-in RC oscillation circuit using external or internal resistors
- Program-selectable duties
  When ABE bit is “L”: 1/8 duty (1 line: 5 × 8 dots), or 1/16 duty (2 lines: 5 × 8 dots)
  When ABE bit is “H”: 1/9 duty (1 line: 5 × 8 dots + arbitrator), or 1/17 duty (2 lines: 5 × 8 dots + arbitrator)
- Cursor display
- Built-in bias dividing resistors to drive the LCD
- Bi-directional transfer of segment outputs
- Bi-directional transfer of common outputs
- 100-dot arbitrator display
- Line display shifting
- Built-in voltage multiplier circuit
- Gold Bump Chip
  ML9042-xx CVWA/DVWA
  *xx indicates a character generator ROM code number.
  *01, 11 and 21 indicate general character generator ROM code numbers.
  CVWA indicates a bump chip with high hardness, and DVWA indicates a bump chip with low hardness.

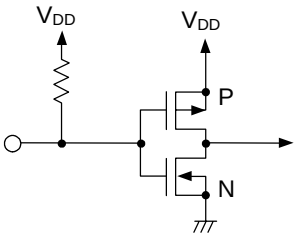
BLOCK DIAGRAM



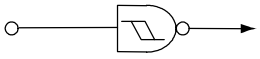
I/O CIRCUITS



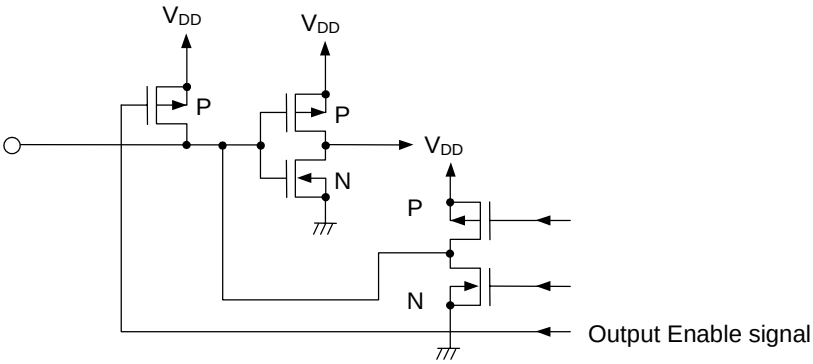
Applied to pins T_1, T_2, and T_3



Applied to pins RW/SI, RS_1, and RS_0/CSB



Applied to pins E/SHTB, SP, ROM1S, and BE



Applied to pins DB_0(SO) to DB_7

PIN DESCRIPTIONS

<table>
<tr><th>Symbol</th><th>Description</th></tr>
<tr><td>RW/SI</td><td>The input pin with a pull-up resistor to select Read (“H”) or Write (“L”) in the Parallel I/F Mode.
The pin to input data in the Serial l/F Mode. Each instruction code and each data are read in by the rising edge of the E/SHTB signal.</td></tr>
<tr><td>RS_0/CSB, RS_1</td><td>The input pins with a pull-up resistor to select a register in the Parallel l/F Mode.
<table>
<tr><th>RS_1</th><th>RS_0/CSB</th><th>Name of register</th></tr>
<tr><td>H</td><td>H</td><td>Data register</td></tr>
<tr><td>H</td><td>L</td><td>Instruction register</td></tr>
<tr><td>L</td><td>L</td><td>Expansion Instruction register</td></tr>
</table>
The RSo/CSB pin is configured as a chip enable input in the Serial I/F Mode. Setting the RSo/CSB pin to “L” allows the I/F to be provided.</td></tr>
<tr><td>E/SHTB</td><td>The input pin for data input/output between the CPU and the ML9042 and for activating instructions in the Parallel l/F Mode.
This pin is configured as a shift clock input in the Serial I/F Mode. The data input to the PW/SI pin is synchronized to the rising edge of the clock, and the data output from the DB0(SO) pin is synchronized to the falling edge of the shift clock.</td></tr>
<tr><td>DB_0(SO) to DB_3</td><td>The input/output pins to transfer data of lower-order 4 bits between the CPU and the ML9042 in the Parallel l/F Mode. The pins are not used for the 4-bit interface.
Only the DB0(SO) pin is configured as a data output in the Serial I/F Mode. Busy flag & address and data are output synchronized to the falling edge of the E/SHTB signal. These pins remain pulled up when data is not output.
Each pin is equipped with a pull-up resistor, so this pin should be open when not used.</td></tr>
<tr><td>DB_4 to DB_7</td><td>The input/output pins to transfer data of upper 4 bits between the CPU and the ML9042 in the Parallel l/F Mode. The pins are not used for the serial interface.
Each pin is equipped with a pull-up resistor, so this pin should be open in the Serial I/F Mode when not used.</td></tr>
<tr><td>OSC_1
OSC_2
OSC_{R3}
OSC_{R5}</td><td>The clock oscillation pins required for LCD drive signals and the operation of the ML9042 by instructions sent from the CPU.
To input external clock, the OSC_1 pin should be used. The OSC_{R3}, $OSC_{R5,}$ and OSC_2 pins should be open.
To start oscillation with an external resistor, the resistor should be connected between the OSC_1 and OSC_2 pins. The OSC_{R3} and OSC_{R5} pins should be open.
To start oscillation at 5 V using an internal resistor, the OSC_2 and OSC_{R5} pins should be short-circuited outside the ML9042. The OSC_1 and OSC_{R3} pins should be open.
To start oscillation at 3 V using an internal resistor, the OSC_2 and OSC_{R3} pins should be short-circuited outside the ML9042. The OSC_1 and OSC_{R5} pins should be open.
(The OSC_2, $OSC_{R3,}$ and OSC_{R5} pins can also be short-circuited outside the ML9042, and the OSC_1 pin can be open.)</td></tr>
<tr><td>COM_1 to COM_{17}</td><td>The LCD common signal output pins.
For 1/8 duty, non-selectable voltage waveforms are output via COM_9 to COM_{17}. For 1/9 duty, non-selectable voltage waveforms are output via COM_{10} to COM_{17}. For 1/16 duty, a non-selectable voltage waveform is output via $COM_{17.}$</td></tr>
<tr><td>SEG_1 to SEG_{100}</td><td>The LCD segment signal output pins.</td></tr>
</table>

Symbol	Description
ROM1S	The input pin to switch the ROM bank. “H” selects ROM1 and “L” selects ROM0. Switching after power-on is prohibited.
V_1 , V_2, V_{3A}, V_{3B}, V_4	The pins to output bias voltages to the LCD. For 1/4 bias : The V_2 and V_{3B} pins are shorted. For 1/5 bias : The V_{3A} and V_{3B} pins are shorted.
BE	The input pin to enable or disable the voltage multiplier circuit. "L" disables the voltage multiplier circuit. "H" enables the voltage multiplier circuit. The voltage multiplier circuit doubles the input voltage between the V_{IN} pin and the GND pin, and the multiplied voltage referenced to the GND is output to the V_{OUT} pin. The voltage multiplier circuit can be used only when generating a level higher than the V_{DD}.
$TEST_{IN}$	The input pin for test circuits. Normally connect this pin to V_{DD}.
$TEST_{OUT}$	The output pin for the test circuits. Normally leave this pin open.
V_{IN}	The pin to input voltage to the voltage multiplier.
V_0, V_{OUT}	The pins to supply the LCD drive voltage. The same potential as the V_{DD} potential is supplied to the V_{OUT} and V_0 pins when the voltage multiplier is not used (BE = “0” or BE = “1”, and the capacitor is not connected to the V_C and V_{CC} pins) When the voltage multiplier is used (BE = “1”), the multiplied voltage is output to the V_{OUT} pin, so that the V_{OUT} pin and V_0 pin should be connected. Capacitors for the voltage multiplier should be connected between the GND and the V_{OUT} pin.
V_C	The pin to connect the negative pin of the capacitor for the voltage multiplier. Leave the pin open when the voltage multiplier circuit is not used.
V_{CC}	The pin to connect the positive pin of the capacitor used for the voltage multiplier. Leave the pin open when the voltage multiplier circuit is not used.
T_1, T_2, T_3	The input pins for test circuits (normally open). Each of these pins is equipped with a pull-down resistor, so this pin should be left open.
V_{DD}	The power supply pin.
GND	The ground level input pin.
SP	The input pin to select the serial or parallel interface. “L” selects the parallel interface. “H” selects the serial interface.
$DUMMYV_{DD}$	The output pin to fix the adjacent input pin to the V_{DD} level. Use this pin only for this purpose.
DUMMYGND	The output pin to fix the adjacent input pin to the GND level. Use this pin only for this purpose.
DUMMY	NC (No Connection) pin.

ABSOLUTE MAXIMUM RATINGS

(GND = 0 V)

Parameter	Symbol	Condition	Rating	Unit	Applicable pins
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to +6.5	V	V_{DD}
LCD Driving Voltage	V_0, V_1, V_2, V_3, V_4,	Ta = 25°C	–0.3 to +6.5	V	V_{OUT}, V_0, V_1, V_2, V_{3A}, V_{3B}, V_4, GND
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD}+0.3	V	RW/SI, E/SHTB, SP, RS_0/CSB, RS_1, BE, ROM1S, T_1 to T_3, DB_0(SO) to DB_7, V_{IN}
Storage Temperature	T_{STG}	—	–55 to +150	°C	—

RECOMMENDED OPERATING CONDITIONS

(GND = 0 V)

Parameter	Symbol	Condition	Range	Unit	Applicable pins
Supply Voltage	V_{DD}	—	2.7 to 5.5	V	V_{DD}
LCD Driving Voltage	V_0 (See Note)	—	2.7 to 5.5	V	V_{OUT}, V_0
Voltage Multipler Input Voltage	V_{MUL}	BE = “1”	1.8 to 2.75	V	V_{IN}
Operating Temperature	T_{op}	—	–40 to +85	°C	—

Note: This voltage should be applied across V_0 and GND. The following voltages are output to the V_1, V_2, V_{3A} (V_{3B}) and V_4 pins:

• 1/4 bias (V_2 and V_{3B} are short-circuited)
$V_1 = 3\ V_0/4 \pm 0.15$ V
$V_2 = V_{3B} = V_0/2 \pm 0.15$ V
$V_4 = V_0/4 \pm 0.15$ V

• 1/5 bias (V_{3A} and V_{3B} are short-circuited)
$V_1 = 4\ V_0/5 \pm 0.15$ V
$V_2 = 3\ V_0/5 \pm 0.15$ V
$V_{3A} = V_{3B} = 2\ V_0/5 \pm 0.15$ V
$V_4 = V_0/5 \pm 0.15$ V

The voltages at the V_0, V_1, V_2, V_{3A} (V_{3B}), V_4 and GND pins should satisfy

$V_0 > V_1 > V_2 > V_{3A}$ (V_{3B}) $> V_4 >$ GND
(Higher ← → Lower)

* If the chip is attached on a substrate using COG technology, the chip tends to be susceptible to electrical characteristics of the chip due to trace resistance on the glass substrate. It is recommended to use the chip by confirming that it operates on the glass substrate properly. Trace resistance, especially, V_{DD} and V_{SS} trace resistance, between the chip on the LCD panel and the flexible cable should be designed as low as possible. Trace resistance that cannot be very well decreased, larger size of the LCD panel, or greater trace capacitance between the microcontroller and the ML9042 device can cause device malfunction. In order to avoid the device malfunction, power noise should be reduced by serial interfacing of the microcontroller and the ML9042 device.

* Do not apply short-circuiting across output pins and across an output pin and an input/output pin or the power supply pin in the output mode.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(GND = 0 V, V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V	RW/SI, RS_0/CSB, RS_1, E/SHTB, DB_0(SO) to DB_7, SP, OSC_1, BE, ROM1S
"L" Input Voltage	V_{IL}	—	0	—	0.2V_{DD}	V	
"H" Output Voltage 1	V_{OH1}	I_{OH} = –0.1 mA	0.9V_{DD}	—	—	V	DB_0(SO) to DB_7
"L" Output Voltage 1	V_{OL1}	I_{OL} = +0.1 mA	—	—	0.1V_{DD}	V	
"H" Output Voltage 2	V_{OH2}	I_{OH} = –13 µA	0.9V_{DD}	—	—	V	OSC_2
"L" Output Voltage 2	V_{OL2}	I_{OL} = +13 µA	—	—	0.1V_{DD}	V	
COM Voltage Drop	V_{CH}	I_{OCH} = –4 µA, V_0 –GND = 5 V Note 1	V_0–0.3	V_0–0.012	V_0	V	COM_1 to COM_{17}
	V_{CMH}	I_{OCMH} = ±4 µA, V_0 –GND = 5 V Note 1	V_1–0.3	V_1±0.012	V_1+0.3	V	
	V_{CML}	I_{OCML} = ±4 µA, V_0 –GND = 5 V Note 1	V_4–0.3	V_4±0.012	V_4+0.3	V	
	V_{CL}	I_{OCL} = +4 µA, V_0 –GND = 5 V Note 1	GND	GND+0.012	GND+0.3	V	
SEG Voltage Drop	V_{SH}	I_{OSH} = –4 µA, V_0 –GND = 5 V Note 1	V_0–0.3	V_0–0.012	V_0	V	SEG_1 to SEG_{100}
	V_{SMH}	I_{OSMH} = ±4 µA, V_0 –GND = 5 V Note 1	V_2–0.3	V_2±0.012	V_2+0.3	V	
	V_{SML}	I_{OSML} = ±4 µA, V_0 –GND = 5 V Note 1	V_3–0.3	V_3±0.012	V_3+0.3	V	
	V_{SL}	I_{OSL} = +4 µA, V_0 –GND = 5 V Note 1	GND	GND+0.012	GND+0.3	V	
Input Leakage Current	| IIL |	V_{DD} = 5 V, V_I = 5 V or 0 V	—	—	1.0	µA	E/SHTB, BE, SP, V_{IN}
Input Current 1	| II1 |	V_{DD} = 5 V, V_I = GND	10	25	61	µA	RW/SI, RS_0/CSB, RS_1, DB_0(SO) to DB_7
		V_{DD} = 5 V, V_I = V_{DD}, Excluding current flowing through the pull-up resistor and the output driving MOS	—	—	2.0	µA	
Input Current 2	| II2 |	V_{DD} = 5 V, V_I = V_{DD}	15	45	105	µA	T_1, T_2, T_3
		V_{DD} = 5 V, V_I = GND Excluding current flowing through the pull-down resistor	—	—	2.0	µA	
Supply Current	I_{DD}	V_{DD} = 5 V Note 2	—	—	1.2	mA	V_{DD}–GND
Oscillation Frequency of External Resistor Rf	f_{osc1}	Rf = 85 kΩ±2% Note 3	175	270	400	kHz	OSC_1, OSC_2

Oscillation Frequency of Internal Resistor Rf		f_{osc2}	V_{DD} = 4.0 to 5.5 V Ta = -20 to 75°C OSC_1 and OSC_{R3}: Open OSC_2 and OSC_{R5}: Short-circuited Note 4	200	270	351	kHz	OSC_1, OSC_2, OSC_{R5}
			V_{DD} = 2.7 to 3.6 V Ta = -20 to 75°C OSC_1 and OSC_{R5}: Open OSC_2 and OSC_{R3}: Short-circuited Note 4	200	280	364	kHz	OSC_1, OSC_2, OSC_{R3}
External Clock	Clock Input Frequency	f_{in}	OSC_2, OSC_R: Open Input from OSC_1	175	—	400	kHz	OSC_1
	Input Clock Duty	f_{duty}	Note 5	45	50	55	%	
	Input Clock Rise Time	f_{rf}	Note 6	—	—	0.2	µs	
	Input Clock Fall Time	f_{ff}	Note 6	—	—	0.2	µs	
LCD Bias Resistor		R_{LB}	-0x code	1.4	2.0	2.6	kΩ	V_0, V_1, V_2, V_{3A}, V_{3B}, V_4, GND
			-1x code	2.8	4.0	5.2	kΩ	V_0, V_1, V_2, V_{3A}, V_{3B}, V_4, GND
			-2x code	7.0	10.0	13.0	kΩ	V_0, V_1, V_2, V_{3A}, V_{3B}, V_4, GND

(GND = 0 V, V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pins
Voltage Multiplier Input Voltage	V_{MUL}	Note 7		1.8	—	2.75	V	V_{IN}
Voltage Multiplier Output Voltage	V_{OUT}	V_{DD} = 2.7 V, V_{IN} = 2.25 V f = 175 kHz A capacitor for the voltage multiplier = 1 to 4.7 μF V_{OUT} load current = 54 μA BE = "H" Applied to LCD bias resistance of 10 kΩ (TYP) only	1/5 bias	4.3	—	(V_{DD}–V_{IN}) × 2	V	V_{OUT}
			1/4 bias	4.3	—	(V_{DD}–V_{IN}) × 2		
Bias Voltage for Driving LCD	V_{LCD1}	V_0–GND Note 8	1/5 bias	2.7	—	5.5	V	V_0
	V_{LCD2}		1/4 bias	2.7	—	5.5		

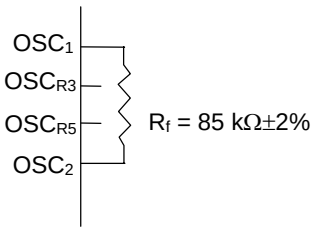
Note 1: Applied to the voltage drop occurring between any of the V_0, V_1, V_4 and GND pins and any of the common pins (COM_1 to COM_{17}) when the current of 4 μA flows in or flows out at one common pin.
Also applied to the voltage drop occurring between any of the V_0, V_2, V_{3A} (V_{3B}) and GND pins and any of the segment pins (SEG_1 to SEG_{100}) when the current of 4 μA flows in or flows out at one segment pin.

The current of 4 μA flows out when the output level is V_{DD} or flows in when the output level is V_5.

Note 2: Applied to the current flowing into the V_{DD} pin when the external clock (f_{OSC2} = f_{in} = 270 kHz) is fed to the internal R_f oscillation or OSC_1 under the following conditions:

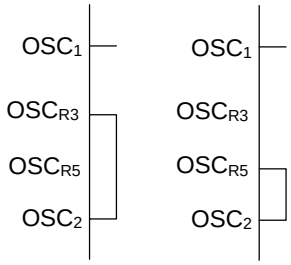
V_{DD} = V_0 = 5 V
GND = 0 V,
V_1, V_2, V_{3A} (V_{3B}) and V_4: Open
E/SHTB and BE: "L" (fixed)
Other input pins: "L" or "H" (fixed)
Other output pins: No load

Note 3:



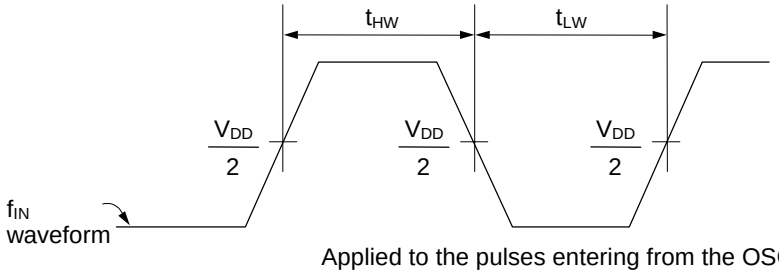
The wire between OSC_1 and R_f and the wire between OSC_2 and R_f should be as short as possible. Keep OSC_{R3} and OSC_{R5} open.

Note 4:



The wire between OSC_{R3} and OSC_2, or between OSC_{R5} and OSC_2 should be as short as possible. Keep open between OSC_1 and OSC_{R3}, or between OSC_1 and OSC_{R5}.

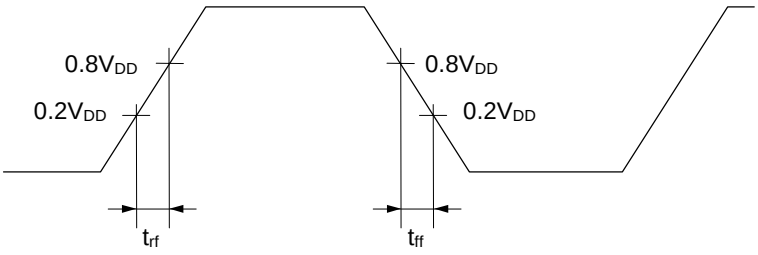
Note 5:



Applied to the pulses entering from the OSC_1 pin

$f_{duty} = t_{HW}/(t_{HW} + t_{LW}) \times 100$ (%)

Note 6:



Applied to the pulses entering from the OSC_1 pin

Note 7: The maximum value of the voltage multiplier input voltage should be set at 2.75 V, and the minimum value of the voltage multiplier input voltage should be set by monitoring the voltage of V_0 in actual use so that the voltage multiplier output voltage meets the specification for the bias voltage for driving LCD after contrast adjustment.

Note 8: For 1/4 bias, V_2 and V_{3B} pins are short-circuited. V_{3A} pin is open.
For 1/5 bias, V_{3A} and V_{3B} pins are short-circuited. V_2 pin is open.

I/O Characteristics

- Parallel Interface Mode

The timing for the input from the CPU and the timing for the output to the CPU are as shown below:

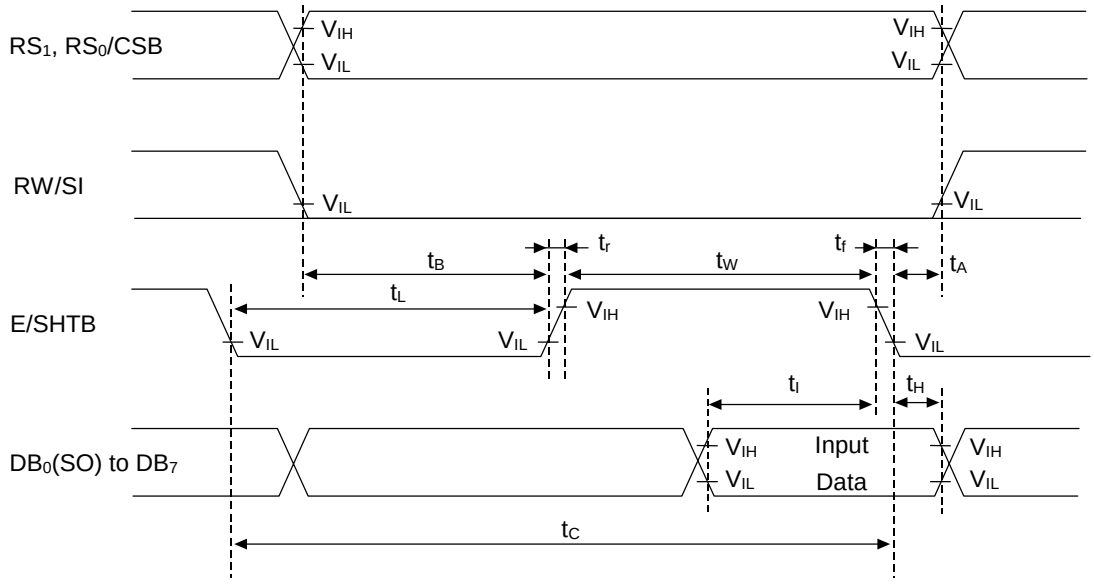
1) WRITE MODE (Timing for input from the CPU)

(V_{DD} = 2.7 to 4.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
RW/SI, RS_0/CSB, RS_1 Setup Time	t_B	40	—	—	ns
E/SHTB Pulse Width	t_W	450	—	—	ns
RW/SI, RS_0/CSB, RS_1 Hold Time	t_A	10	—	—	ns
E/SHTB Rise Time	t_r	—	—	125	ns
E/SHTB Fall Time	t_f	—	—	125	ns
E/SHTB Pulse Width	t_L	430	—	—	ns
E/SHTB Cycle Time	t_C	1000	—	—	ns
DB_0(SO) to DB_7 Input Data Setup Time	t_I	195	—	—	ns
DB_0(SO) to DB_7 Input Data Hold Time	t_H	10	—	—	ns

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
RW/SI, RS_0/CSB, RS_1 Setup Time	t_B	40	—	—	ns
E/SHTB Pulse Width	t_W	220	—	—	ns
RW/SI, RS_0/CSB, RS_1 Hold Time	t_A	10	—	—	ns
E/SHTB Rise Time	t_r	—	—	125	ns
E/SHTB Fall Time	t_f	—	—	125	ns
E/SHTB Pulse Width	t_L	220	—	—	ns
E/SHTB Cycle Time	t_C	500	—	—	ns
DB_0(SO) to DB_7 Input Data Setup Time	t_I	60	—	—	ns
DB_0(SO) to DB_7 Input Data Hold Time	t_H	10	—	—	ns



2) READ MODE (Timing for output to the CPU)

(V_{DD} = 2.7 to 4.5 V, Ta = –40 to +85°C)

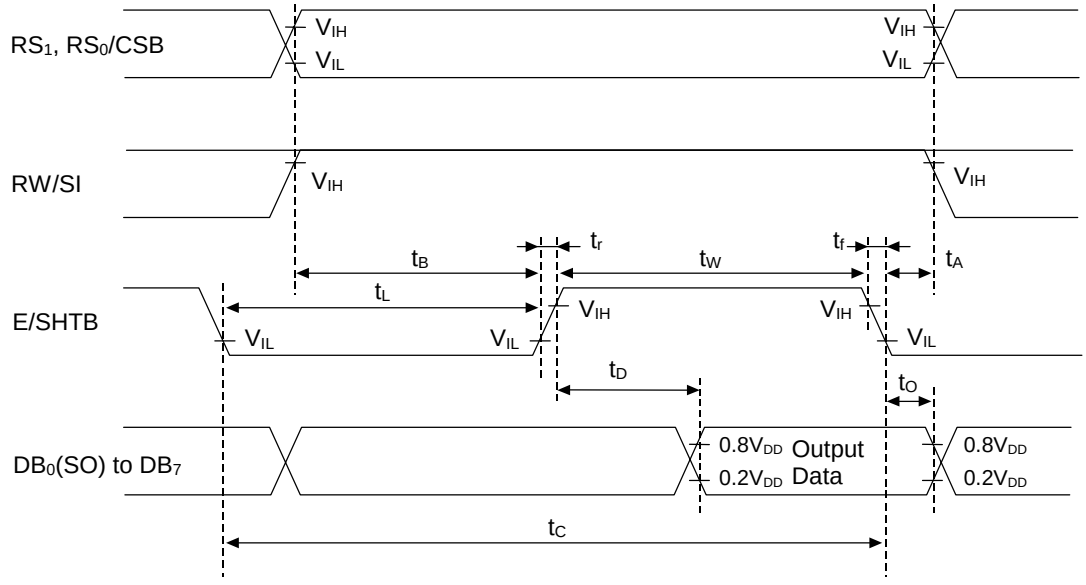
Parameter	Symbol	Min.	Typ.	Max.	Unit
RW/SI, RS_1, RS_0/CSB Setup Time	t_B	40	—	—	ns
E/SHTB Pulse Width	t_W	450	—	—	ns
RW/SI, RS_1, RS_0/CSB Hold Time	t_A	10	—	—	ns
E/SHTB Rise Time	t_r	—	—	125	ns
E/SHTB Fall Time	t_f	—	—	125	ns
E/SHTB Pulse Width	t_L	430	—	—	ns
E/SHTB Cycle Time	t_C	1000	—	—	ns
DB_0(SO) to DB_7 Output Data Delay Time	t_D	—	—	350	ns
DB_0(SO) to DB_7 Output Data Hold Time	t_O	20	—	—	ns

Note: A load capacitance of each of DB_0(SO) to DB_7 must be 50 pF or less.

(V_{DD} = 4.5 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
RW/SI, RS_1, RS_0/CSB Setup Time	t_B	40	—	—	ns
E/SHTB Pulse Width	t_W	220	—	—	ns
RW/SI, RS_1, RS_0/CSB Hold Time	t_A	10	—	—	ns
E/SHTB Rise Time	t_r	—	—	125	ns
E/SHTB Fall Time	t_f	—	—	125	ns
E/SHTB Pulse Width	t_L	220	—	—	ns
E/SHTB Cycle Time	t_C	500	—	—	ns
DB_0(SO) to DB_7 Output Data Delay Time	t_D	—	—	250	ns
DB_0(SO) to DB_7 Output Data Hold Time	t_O	20	—	—	ns

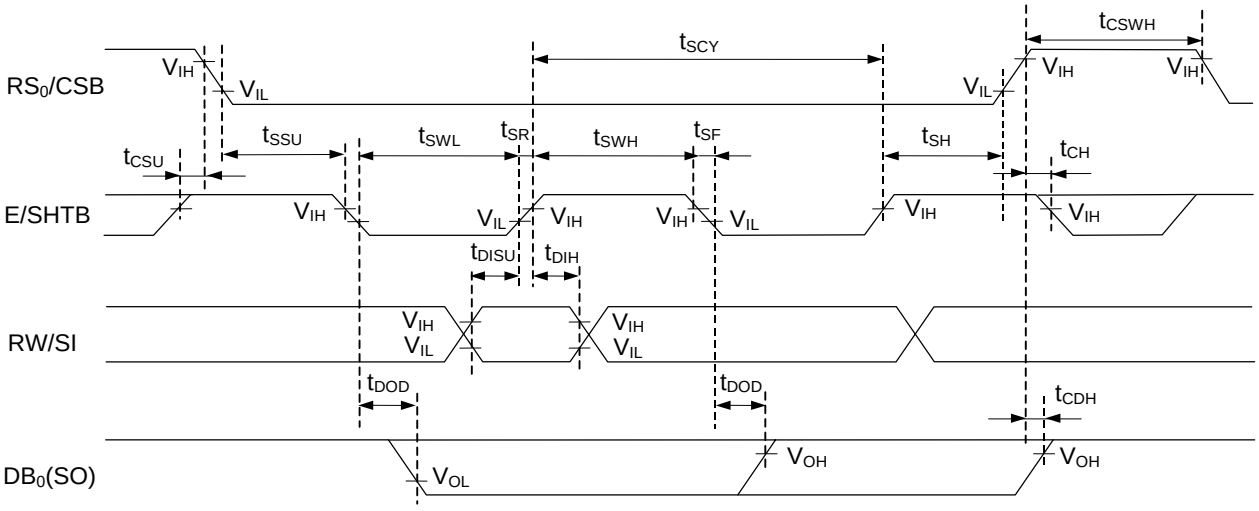
Note: A load capacitance of each of DB_0(SO) to DB_7 must be 50 pF or less.



- Serial Interface Mode

(V_{DD} = 2.7 to 5.5 V, Ta = –40 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
E/SHTB Cycle Time	t_{SCY}	500	—	—	ns
RS_0/CSB Setup Time	t_{CSU}	100	—	—	ns
RS_0/CSB Hold Time	t_{CH}	100	—	—	ns
RS_0/CSB “H” Pulse Width	t_{CSWH}	200	—	—	ns
E/SHTB Setup Time	t_{SSU}	60	—	—	ns
E/SHTB Hold Time	t_{SH}	200	—	—	ns
E/SHTB “H” Pulse Width	t_{SWH}	200	—	—	ns
E/SHTB “L” Pulse Width	t_{SWL}	200	—	—	ns
E/SHTB Rise Time	t_{SR}	—	—	125	ns
E/SHTB Fall Time	t_{SF}	—	—	125	ns
RW/SI Setup Time	t_{DISU}	100	—	—	ns
RW/SI Hold Time	t_{DIH}	100	—	—	ns
DB_0(SO) Output Data Delay Time	t_{DOD}	—	—	160	ns
DB_0(SO) Output Data Hold Time	t_{CDH}	0	—	—	ns



FUNCTIONAL DESCRIPTION

Instruction Register (IR), Data Register (DR), and Expansion Instruction Register (ER)

These registers are selected by setting the level of the Register Selection input pins RS_0/CSB and RS_1. The DR is selected when both RS_0/CSB and RS_1 are "H". The IR is selected when RS_0/CSB is "L" and RS_1 is "H". The ER is selected when both RS_0/CSB and RS_1 are "L". (When RS_0/CSB is "H" and RS_1 is "L", the ML9042 is not selected.)
The IR stores an instruction code and sets the address code of the display data RAM (DDRAM) or the character generator RAM (CGRAM).
The microcontroller (CPU) can write but cannot read the instruction code.
The ER sets the display positions of the arbitrator and the address code of the arbitrator RAM (ABRAM).
The CPU can write but cannot read the display positions of the arbitrator.
The DR stores data to be written in the DDRAM, ABRAM and CGRAM and also stores data read from the DDRAM, ABRAM and CGRAM.
The data written in the DR by the CPU is automatically written in the DDRAM, ABRAM or CGRAM.
When an address code is written in the IR or ER, the data of the specified address is automatically transferred from the DDRAM, ABRAM or CGRAM to the DR. The data of the DDRAM, ABRAM and CGRAM can be checked by allowing the CPU to read the data stored in the DR.
After the CPU writes data in the DR, the data of the next address in the DDRAM, ABRAM or CGRAM is selected to be ready for the next writing by the CPU. Similarly, after the CPU reads the data in the DR, the data of the next address in the DDRAM, ABRAM or CGRAM is set in the DR to be ready for the next reading by the CPU.
Writing in or reading from these 3 registers is controlled by changing the status of the RW/SI pin.

Table 1 RW/SI pin status and register operation

RW/SI	RS_0/CSB	RS_1	Operation
L	L	H	Writing in the IR
H	L	H	Reading the Busy flag (BF) and the address counter (ADC)
L	H	H	Writing in the DR
H	H	H	Reading from the DR
L	L	L	Writing in the ER
H	L	L	Disabled (Not in a busy state, not performing the reads. Note that the data bus goes into a high impedance state.)
L	H	L	Disabled (Not in a busy state, not performing the writes)
H	H	L	Disabled (Not in a busy state, not performing the reads. Note that the data bus goes into a high impedance state.)

Busy Flag (BF)

The status "1" of the Busy Flag (BF) indicates that the ML9042 is carrying out internal operation.
When the BF is "1", any new instruction is ignored.
When RW/SI = "H", RS_0/CSB = "L" and RS_1 = "H", the data in the BF is output to the DB_7.
New instructions should be input when the BF is "0".
When the BF is "1", the output code of the address counter (ADC) is undefined.

Address Counter (ADC)

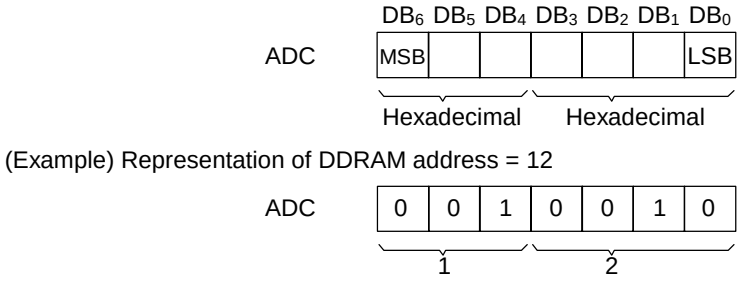
The address counter provides a read/write address for the DDRAM, ABRAM or CGRAM and also provides a cursor display address.
When an instruction code specifying DDRAM, ABRAM or CGRAM address setting is input to the pre-defined register, the register selects the specified DDRAM, ABRAM or CGRAM and transfers the address code to the ADC. The address data in the ADC is automatically incremented (or decremented) by 1 after the display data is written in or read from the DDRAM, ABRAM or CGRAM.
The data in the ADC is output to DB_0(SO) to DB_6 when RW/SI = "H", RS_0/CSB = "L", RS_1 = "H" and BF = "0".

Timing Generator

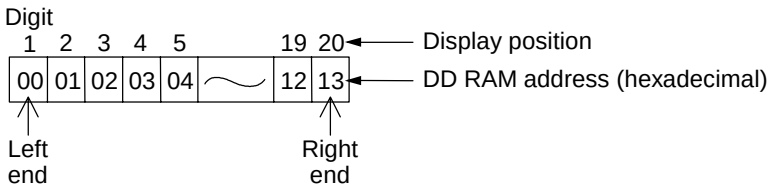
The timing generator generates timing signals for the internal operation of the ML9042 activated by the instruction sent from the CPU or for the operation of the internal circuits of the ML9042 such as DDRAM, ABRAM, CGRAM and CGROM. Timing signals are generated so that the internal operation carried out for LCD displaying will not be interfered by the internal operation initiated by accessing from the CPU. For example, when the CPU writes data in the DDRAM, the display of the LCD not corresponding to the written data is not affected.

Display Data RAM (DDRAM)

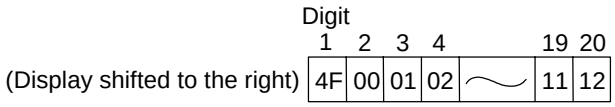
This RAM stores the 8-bit character codes (see Table 2).
The DDRAM addresses correspond to the display positions (digits) of the LCD as shown below. The DDRAM addresses (to be set in the ADC) are represented in hexadecimal.

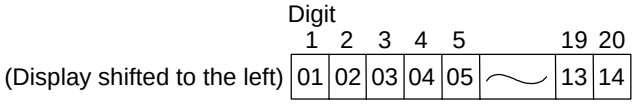


1) Relationship between DDRAM addresses and display positions (1-line display mode)

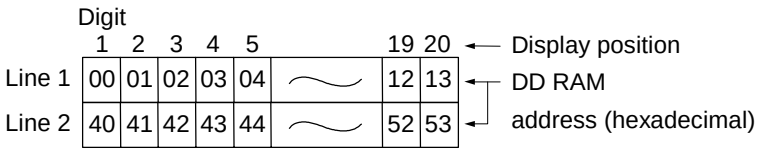


In the 1-line display mode, the ML9042 can display up to 20 characters from digit 1 to digit 20. While the DDRAM has addresses “00” to “4F” for up to 80 character codes, the area not used for display can be used as a RAM area for general data. When the display is shifted by instruction, the relationship between the LCD display position and the DDRAM address changes as shown below:





2) Relationship between DDRAM addresses and display positions (2-line display mode)
In the 2-line mode, the ML9042 can display up to 40 characters (20 characters per line) from digit 1 to digit 20.



Note: The DDRAM address at digit 20 in the first line is not consecutive to the DDRAM address at digit 1 in the second line.

When the display is shifted by instruction, the relationship between the LCD display position and the DDRAM address changes as shown below:

(Display shifted to the right)

Digit	1	2	3	4	5		19	20
Line 1	27	00	01	02	03		11	12
Line 2	67	40	41	42	43		51	52

(Display shifted to the left)

Digit	1	2	3	4	5		19	20
Line 1	01	02	03	04	05		13	14
Line 2	41	42	43	44	45		53	54

Character Generator ROM (CGROM)

The CGROM generates character patterns (5 × 8 dots, 240 patterns) from the 8-bit character code signals in the DDRAM. The bank switching pin (ROM1S) can switch to the other ROM that generates character patterns (5 × 8 dots, 240 patterns), allowing a total of 480 characters to be controlled.
When the 8-bit character code corresponding to a character pattern in the CGROM is written in the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address.
Character codes 10 to FF are contained in the ROM area in the CG ROM.
The general character generator ROM codes are 01/11/21.
The relationship between character codes and general purpose character patterns in Bank0 (ROM0) and Bank1 (ROM1) are indicated in Table 2-1 and Table 2-2, respectively.

Character Generator RAM (CGRAM)

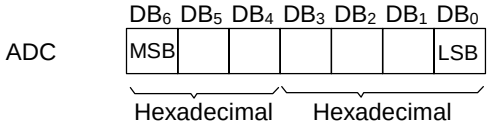
The CGRAM is used to generate user-specific character patterns that are not in the CGROM. CGRAM (64 bytes = 512 bits) can store up to 8 character patterns (5 × 8 dots) .
When displaying a character pattern stored in the CGRAM, write an 8-bit character code (00 to 07 or 08 to 0F; hex.) to the DDRAM. This enables outputting the character pattern to the LCD display position corresponding to the DDRAM address.
The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.
The following describes how character patterns are written in and read from the CGRAM. (See Tables 2-1 and 2-2.)

(1) A method of writing character patterns to the CGRAM from the CPU
The three CGRAM address bit weights 0 to 2 select one of the lines constituting a character pattern.
First, set the mode to increment or decrement from the CPU, and then input the CGRAM address.
Write each line of the character pattern in the CGRAM through DB_0(SO) to DB_7.
The data lines DB_0(SO) to DB_7 correspond to the CGRAM data bit weights 0 to 7, respectively (see Table 3-1). Input data "1" represents the ON status of an LCD dot and "0" represents the OFF status. Since the ADC is automatically incremented or decremented by 1 after the data is written to the CGRAM, it is not necessary to set the CGRAM address again.
The bottom line of a character pattern (the CGRAM address bit weights 0 to 2 are all "1", which means 7 in hexadecimal) is the cursor line. The ON/OFF pattern of this line is ORed with the cursor pattern for displaying on the LCD. Therefore, the pattern data for the cursor position should be all zeros to display the cursor.
Whereas the data given by the CGRAM data bit weights 0 to 4 is output to the LCD as display data, the data given by the CGRAM data bit weights 5 to 7 is not. Therefore, the CGRAM data bit weights 5 to 7 can be used as a RAM area.

(2) A method of displaying CGRAM character patterns on the LCD
The CGRAM is selected when the higher-order 4 bits of a character code are all zeros. Since bit weight 3 of a character code is not used, the character pattern "0" in Table 3-1 can be selected using the character code "00" or "08" in hexadecimal.
When the 8-bit character code corresponding to a character pattern in the CGRAM is written to the DDRAM, the character pattern is displayed in the display position specified by the DDRAM address. (The DDRAM data bit weights 0 to 2 correspond to the CGRAM address bit weights 3 to 5, respectively.)

Arbitrator RAM (ABRAM)

The arbitrator RAM (ABRAM) stores arbitrator display data.
100 dots can be displayed in both 1-line and 2-line display modes. The arbitrator RAM has the addresses (hexadecimal) from “00” to “1F” and the valid display address area is from 00 to 19 (0H to 13H). The area of 20 to 31 (14H to 1FH) not used for display can be used as a data RAM area for general data. Even if the display is shifted by instruction, the arbitrator display is not shifted.
A capacity of 8 bits by 32 addresses (= 256 bits) is available for data write.
First set the mode to increment or decrement from the CPU, and then input the ABRAM address.
Write Display-ON data in the ABRAM through DB_0(SO) to DB_7.
DB_0(SO) to DB_7 correspond to the ABRAM data bit weights 0 to 7 respectively. Input data “1” represents the ON status of an LCD dot and “0” represents the OFF status.
Since ADC is automatically incremented or decremented by 1 after the data is written to the ABRAM, it is not necessary to set the ABRAM address again.
Whereas ABRAM data bit weights 0 to 4 are output as display data to the LCD, the ABRAM data bit weights 5 to 7 are not. These bits can be used as a RAM area.
The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.



The arbitrator RAM can store a maximum of 100 dots of the arbitrator Display-ON data in units of 5 dots.
The relationship with the LCD display positions is shown below.

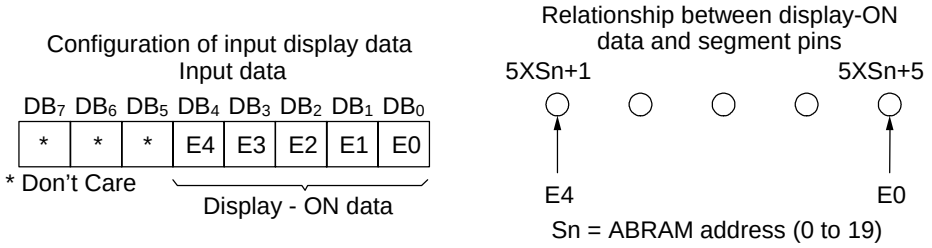


Table 2-1 Character Codes in Bank0 (ROM1S = "0")

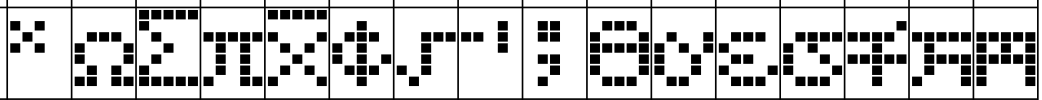
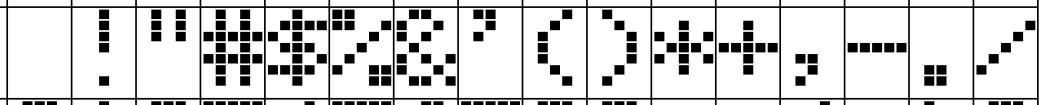
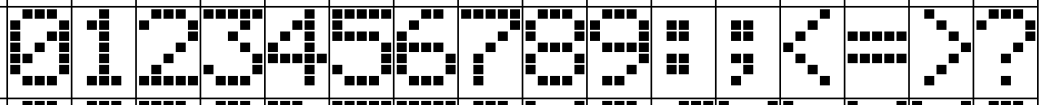
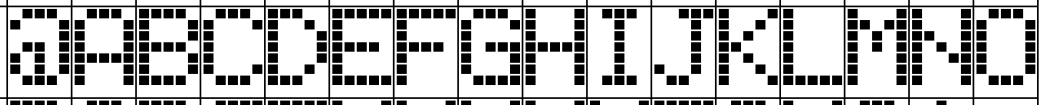
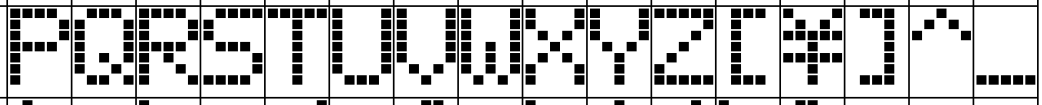
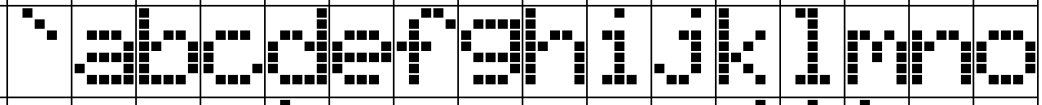
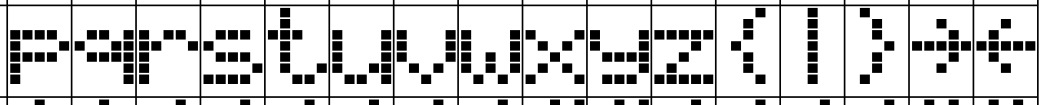
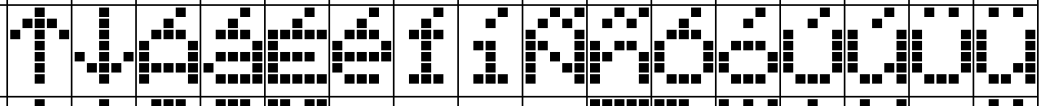
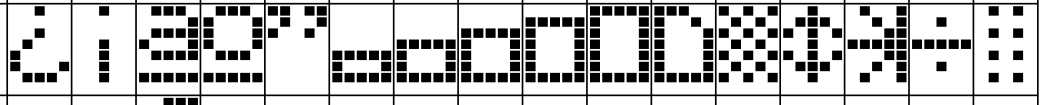
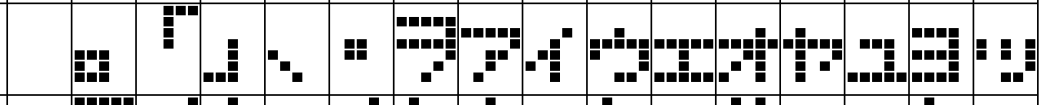
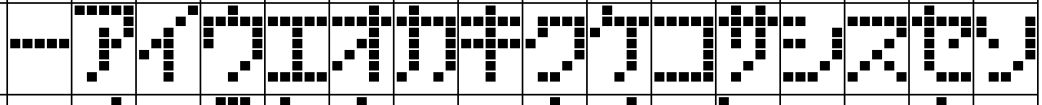
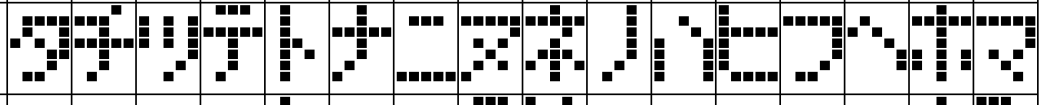
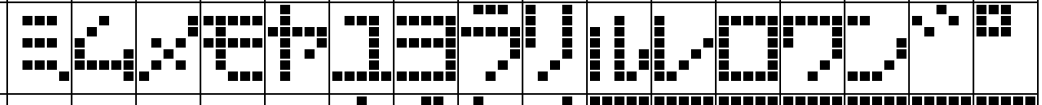
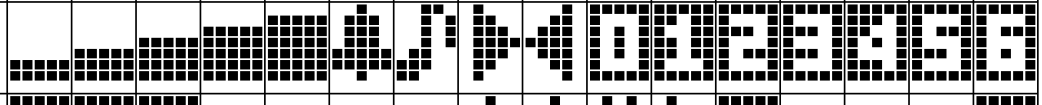
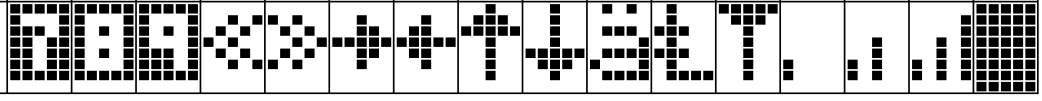
Higher 4 bits \ Lower 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

Table 2-2 Character Codes in Bank1 (ROM1S = "1")

Higher 4 bits \ Lower 4 bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)
0001																
0010																
0011																
0100																
0101																
0110																
0111																
1000																
1001																
1010																
1011																
1100																
1101																
1110																
1111																

Note: The same CGRAM character patterns are displayed in Bank0 and Bank1.

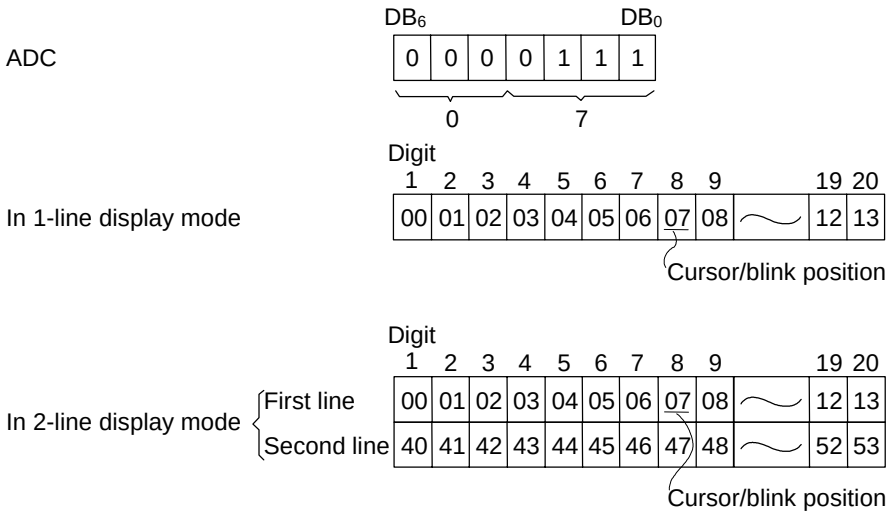
Table 3-1 Relationship between CGRAM address bits, CGRAM data bits (character pattern) and DDRAM data bits (character code) in 5 × 7 dot character mode. (Examples)

CG RAM address	CG RAM data (Character pattern)	DD RAM data (Character code)
5 4 3 2 1 0 (MSB LSB)	7 6 5 4 3 2 1 0 (MSB LSB)	7 6 5 4 3 2 1 0 (MSB LSB)
0 0 0 0 0 0	× × × 0 1 1 1 0	0 0 0 0 × 0 0 0
0 0 1	1 0 0 0 1	
0 1 0	1 0 0 0 1	
0 1 1	1 0 0 0 1	
1 0 0	1 0 0 0 1	
1 0 1	1 0 0 0 1	
1 1 0	0 1 1 1 0	
1 1 1	0 0 0 0 0	
0 0 1 0 0 0	× × × 1 0 0 0 1	0 0 0 0 × 0 0 1
0 0 1	1 0 0 1 0	
0 1 0	1 0 1 0 0	
0 1 1	1 1 0 0 0	
1 0 0	1 0 1 0 0	
1 0 1	1 0 0 1 0	
1 1 0	1 0 0 0 1	
1 1 1	0 0 0 0 0	
1 1 1 0 0 0	× × × 0 1 1 1 0	0 0 0 0 × 1 1 1
0 0 1	0 0 1 0 0	
0 1 0	0 0 1 0 0	
0 1 1	0 0 1 0 0	
1 0 0	0 0 1 0 0	
1 0 1	0 0 1 0 0	
1 1 0	0 1 1 1 0	
1 1 1	0 0 0 0 0	

×: Don't Care

Cursor/Blink Control Circuit

This circuit generates the cursor and blink of the LCD.
The operation of this circuit is controlled by the program of the CPU.
The cursor/blink display is carried out in the position corresponding to the DDRAM address set in the ADC (Address Counter).
For example, when the ADC stores a value of "07" (hexadecimal), the cursor or blink is displayed as follows:



Note: The cursor or blink is also displayed even when a CGRAM or ABRAM address is set in the ADC. Therefore, the cursor or blink display should be inhibited while the ADC is holding a CGRAM or ABRAM address.

LCD Display Circuit (COM1 to COM17, SEG1 to SEG100, SSR and CSR)

The ML9042 has 17 common signal outputs and 100 segment signal outputs to display 20 characters (in the 1-line display mode) or 40 characters (in the 2-line display mode).
The character pattern is converted into serial data and transferred in series through the shift register.
The transfer direction of serial data is determined by the SSR bit. The shift direction of common signals is determined by the CSR bit. The following tables show the transfer and shift directions:

SSR bit	Transfer direction
L	$SEG_1 \rightarrow SEG_{100}$
H	$SEG_{100} \rightarrow SEG_1$

ABE bit	CSR bit	duty	AS bit	Shift Direction	Arbitrator's common pin
L	L	1/8	L	COM1→COM8	None
L	L	1/8	H	COM1→COM8	None
L	L	1/16	L	COM1→COM16	None
L	L	1/16	H	COM1→COM16	None
L	H	1/8	L	COM8→COM1	None
L	H	1/8	H	COM8→COM1	None
L	H	1/16	L	COM16→COM1	None
L	H	1/16	H	COM16→COM1	None
H	L	1/9	L	COM1→COM9	COM9
H	L	1/9	H	COM1→COM9	COM1
H	L	1/17	L	COM1→COM17	COM17
H	L	1/17	H	COM1→COM17	COM1
H	H	1/9	L	COM9→COM1	COM1
H	H	1/9	H	COM9→COM1	COM9
H	H	1/17	L	COM17→COM1	COM1
H	H	1/17	H	COM17→COM1	COM17

* Refer to the Expansion Instruction Codes section about the ABE bit, SSR bit, CSR bit, and AS bit.

Signals to be input to the SSR bit, CSR bit, ABE bit, and AS bit should be initially determined at power-on and be kept unchanged.

Built-in Reset Circuit

The ML9042 is automatically initialized when the power is turned on.
During initialization, the Busy Flag (BF) is "1" and the ML9042 does not accept any instruction from the CPU (other than the Read BF instruction).
The Busy Flag is "1" for about 15 ms after the V_{DD} becomes 2.7 V or higher.
During this initialization, the ML9042 performs the following instructions:

1) Display clearing
2) CPU interface data length = 8 bits (DL = "1")
3) 1-line LCD display (N = "0")
4) ADC counting = Increment (I/D = "1")
5) Display shifting = None (S = "0")
6) Display = Off (D = "0")
7) Cursor = Off (C = "0")
8) Blinking = Off (B = "0")
9) Arbitrator = Displayed in the lower line (AS = "0")
10) Arbitrator = Not displayed (ABE = "0")
11) Segment shift direction = $SEG_1 \rightarrow SEG_{100}$ (SSR = "0")
12) Common shift direction = $COM_1 \rightarrow COM_{17}$ (CSR = "0")

To use the built-in reset circuit, the power supply conditions shown below should be satisfied. Otherwise, the built-in reset circuit may not work properly. In such a case, initialize the ML9042 with the instructions from the CPU. The use of a battery always requires such initialization from the CPU. (See "Initial Setting of Instructions")

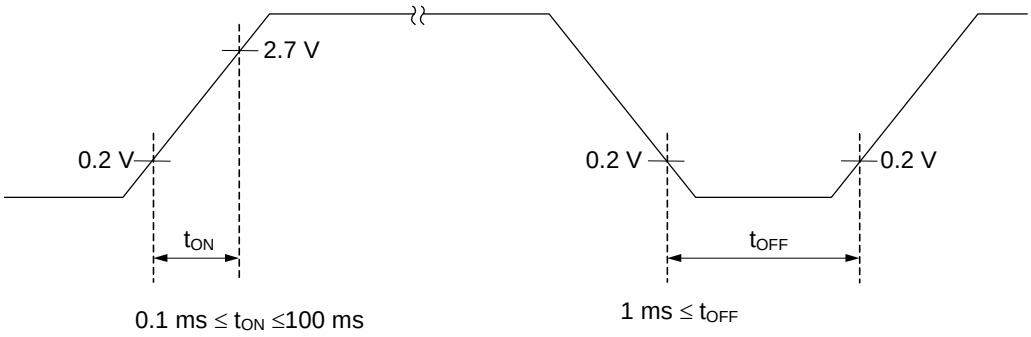


Figure 1 Power-on and Power-off Waveform

I/F with CPU

Parallel interface mode
The ML9042 can transfer either 8 bits once or 4 bits twice on the data bus for interfacing with any 8-bit or 4-bit microcontroller (CPU).

1) 8-bit interface data length
   The ML9042 uses all of the 8 data bus lines DB_0(SO) to DB_7 at a time to transfer data to and from the CPU.

2) 4-bit interface data length
   The ML9042 uses only the higher-order 4 data bus lines DB_4 to DB_7 twice to transfer 8-bit data to and from the CPU.
   The ML9042 first transfers the higher-order 4 bits of 8-bit data (DB_4 to DB_7 in the case of 8-bit interface data length) and then the lower-order 4 bits of the data (DB_0(SO) to DB_3 in the case of 8-bit interface data length). The lower-order 4 bits of data should always be transferred even when only the transfer of the higher-order 4 bits of data is required. (Example: Reading the Busy Flag)
   Two transfers of 4 bits of data complete the transfer of a set of 8-bit data. Therefore, when only one access is made, the following data transfer cannot be completed properly.

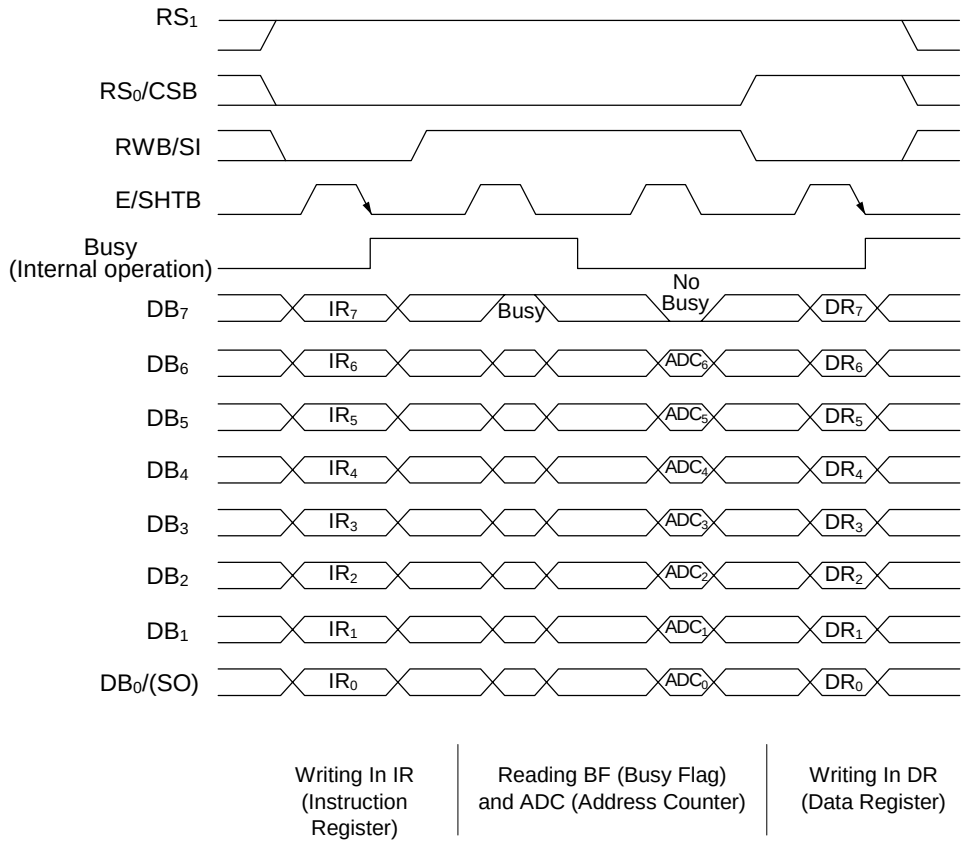


Figure 2 8-Bit Data Transfer

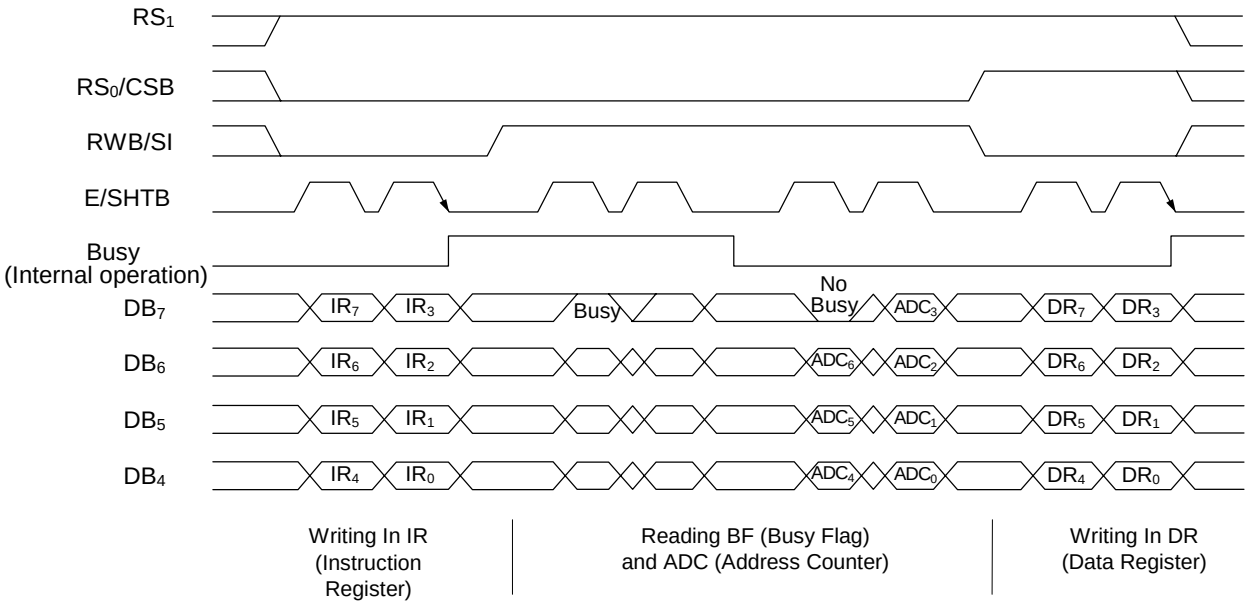


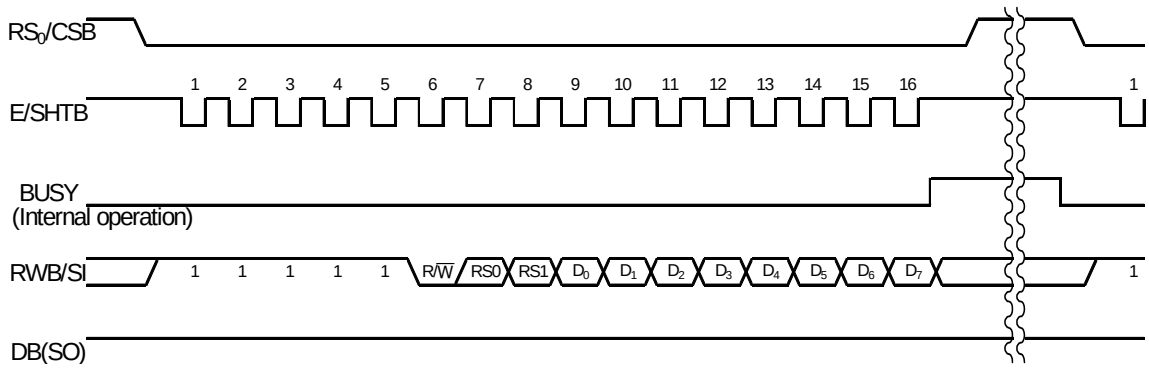
Figure 3 4-Bit Data Transfer

Serial Interface Mode

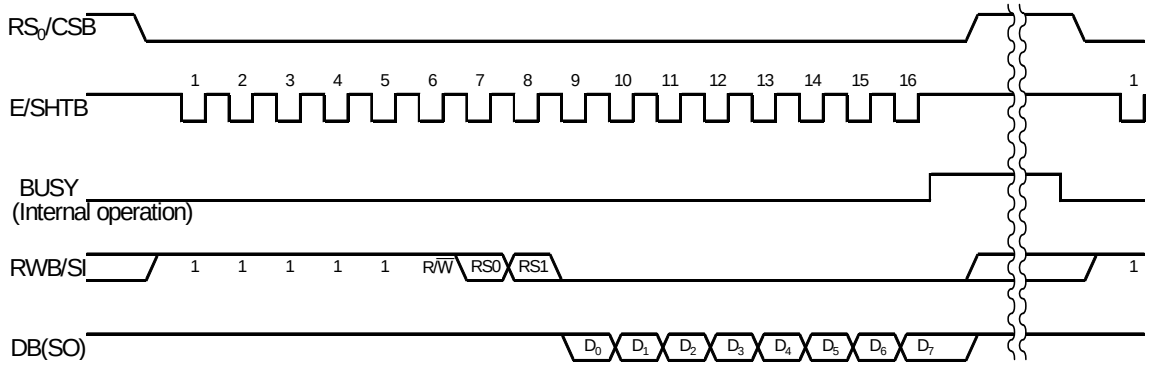
In the Serial I/F Mode, the ML9042 interfaces with the CPU via the RS_0/CSB, E/SHTB, RW/SI, and DB_0(SO) pins.
Writing and reading operations are executed in units of 16 bits after the RS_0/CSB signal falls down. If the RS_0/CSB signal rises up before the completion of 16-bit unit access, this access is ignored.
When the BF bit is "1", the ML9042 cannot accept any other instructions. Before inputting a new instruction, check that the BF bit is "0". Any access when the BF bit is "1" is ignored.
Data format is LSB-first.

Examples of Access in the Serial I/F Mode

1) WRITE MODE



2) READ MODE



Note 1: Higher 5 bits of each instruction must be input at a "H" level.
Note 2: Lower 8 bits are "don't care" when the instructions in the READ MODE are set.
Note 3: After one instruction is input, the next instruction must be input after the RS_0/CSB pin is pulled at a "H" level.

Instruction Codes

Table of Instruction Codes

Instruction	Code											Function	Execution Time f = 270 kHz
	RS_1	RS_0/ CSB	RW/ SI	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0 (SO)		
Display Clear	1	0	0	0	0	0	0	0	0	0	1	Clears all the displayed digits of the LCD and sets the DDRAM address 00 in the address counter. The arbitrator data is cleared.	1.52 ms
Cursor Home	1	0	0	0	0	0	0	0	0	1	X	Sets the DDRAM address 00 in the address counter and shifts the display back to the original. The content of the DDRAM remains unchanged.	1.52 ms
Entry Mode Setting	1	0	0	0	0	0	0	0	1	I/D	S	Determines the direction of movement of the cursor and whether or not to shift the display. This instruction is executed when data is written or read.	37 μs
Display ON/OFF Control	1	0	0	0	0	0	0	1	D	C	B	Sets LCD display ON/OFF (D), cursor ON/OFF (C) or cursor-position character blinking ON/OFF (B).	37 μs
Cursor/Display Shift	1	0	0	0	0	0	1	S/C	R/L	X	X	Moves the cursor or shifts the display without changing the content of the DDRAM.	37 μs
Function Setting	1	0	0	0	0	1	DL	N	ABE	SSR	CSR	Sets the interface data length (DL), the number of display lines (N), the arbitrator display (ABE), the segment data shift direction (SSR), or the common data shift direction (CSR).	37 μs
CGRAM Address Setting	1	0	0	0	1	ACG						Sets on CGRAM address. After that, CGRAM data is transferred to and from the CPU.	37 μs
DDRAM Address Setting	1	0	0	1	ADD							Sets a DDRAM address. After that, DDRAM data is transferred to and from the CPU.	37 μs
Busy Flag/ Address Read	1	0	1	BF	ADC							Reads the Busy Flag (indicating that the ML9042 is operating) and the content of the address counter.	0 μs
RAM Data Write	1	1	0	WRITE DATA								Writes data in DDRAM, ABRAM or CGRAM.	37 μs
RAM Data Read	1	1	1	READ DATA								Reads data from DDRAM, ABRAM or CGRAM.	37 μs
Arbitrator Display Line Set	0	0	0	0	0	0	0	0	0	1	AS	Sets the arbitrator display line.	37 μs
ABRAM Address Setting	0	0	0	0	1	1	AAB					Sets an ABRAM address. After that, ABRAM data is transferred to and from the CPU.	37 μs

—	I/D = “1” (Increment) I/D = “0” (Decrement) S = “1” (Shifts the display.) S/C = “1” (Shifts display.) S/C = “0” (Moves the cursor.) R/L = “1” (Right shift) R/L = “0” (Left shift) D/L = “1” (8-bit data) DL = “0” (4-bit data) N = “1” (2 lines) N = “0” (1 line) ABE = “1” (Arbitrator displayed) ABE = “0” (Arbitrator not displayed) SSR = “1” (Transfer direction: $SEG_{100} \rightarrow SEG_1$) SSR = “0” (Transfer direction: $SEG_1 \rightarrow SEG_{100}$) CSR = “1” (Transfer direction: COMn → COM1) CSR = “0” (Transfer direction: COM1 → COMn) BF = “1” (Busy) BF = “0” (Ready to accept an instruction) B = “1” (Enables blinking) C = “1” (Displays the cursor.) D = “1” (Displays a character pattern.) AS = “1” (Arbitrator Displays arbitrator on the upper line) AS = “0” (Arbitrator Displays arbitrator on the lower line)	DD RAM: Display data RAM CG RAM: Character generator RAM ABRAM: Arbitrator data RAM ACG: CGRAM address ADD: DDRAM address (Corresponds to the cursor address) AAB: ABRAM address ADC: Address counter (Used by DDRAM, ABRAM and CGRAM)	The execution time is dependent upon frequencies.

×: Don't Care

Instruction Codes

An instruction code is a signal sent from the CPU to access the ML9042. The ML9042 starts operation as instructed by the code received. The busy status of the ML9042 is rather longer than the cycle time of the CPU, since the internal processing of the ML9042 starts at a timing which does not affect the display on the LCD. In the busy status (Busy Flag is "1"), the ML9042 cannot input the Busy Flag Read instruction only. Therefore, the CPU should ensure that the Busy Flag is "0" before sending an instruction code to the ML9042.

1) Display Clear

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction Code:	1	0	0	0	0	0	0	0	0	0	1

When this instruction is executed, the LCD display including arbitrator display is cleared and the I/D entry mode is set to "Increment". The value of "S" (Display shifting) remains unchanged. The position of the cursor or blink being displayed moves to the left end of the LCD (or the left end of the line 1 in the 2-line display mode).

Note: All DDRAM and ABRAM data turn to "20" and "00" in hexadecimal, respectively. The value of the address counter (ADC) turns to the one corresponding to the address "00" (hexadecimal) of the DDRAM.
The execution time of this instruction is 1.52 ms (maximum) at an oscillation frequency of 270 kHz.

2) Cursor Home

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	0	0	0	1	×

×: Don't Care

When this instruction is executed, the cursor or blink position moves to the left end of the LCD (or the left end of line 1 in the 2-line display mode). If the display has been shifted, the display returns to the original display position before shifting.

Note: The value of the address counter (ADC) goes to the one corresponding to the address "00" (hexadecimal) of the DDRAM).
The execution time of this instruction is 1.52 ms (maximum) at an oscillation frequency of 270 kHz.

3) Entry Mode Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	0	0	1	I/D	S

(1) When the I/D is set, the cursor or blink shifts to the right by 1 character position (ID= "1"; increment) or to the left by 1 character position (I/D= "0"; decrement) after an 8-bit character code is written to or read from the DDRAM. At the same time, the address counter (ADC) is also incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement). After a character pattern is written to or read from the CGRAM, the address counter (ADC) is incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement).
Also after data is written to or read from the ABRAM, the address counter (ADC) is incremented by 1 (when I/D = "1"; increment) or decremented by 1 (when I/D = "0"; decrement).

(2) When S = "1", the cursor or blink stops and the entire display shifts to the left (I/D = "1") or to the right (I/D = "0") by 1 character position after a character code is written to the DDRAM.
In the case of S = "1", when a character code is read from the DDRAM, when a character pattern is written to or read from the CGRAM or when data is written to or read from the ABRAM, normal read/write is carried out without shifting of the entire display. (The entire display does not shift, but the cursor or blink shifts to the right (I/D = "1") or to the left (I/D = "0") by 1 character position.)
When S = "0", the display does not shift, but normal write/read is performed.

Note: The execution time of this instruction is 37 μs (maximum) at an oscillation frequency of 270 kHz.

4) Display ON/OFF Control

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	0	1	D	C	B

(1) The "D" bit (DB2) of this instruction determines whether or not to display character patterns on the LCD. When the "D" bit is "1", character patterns are displayed on the LCD.
When the "D" bit is "0", character patterns are not displayed on the LCD and the cursor/blinking also disappear.

Note: Unlike the Display Clear instruction, this instruction does not change the character code in the DDRAM .

(2) When the "C" bit (DB1) is "0", the cursor turns off. When both the "C" and "D" bits are "1", the cursor turns on.

(3) When the "B" bit (DB0) is "0", blinking is canceled. When both the "B" and "D" bits are "1", blinking is performed.
In the Blinking mode, all dots including those of the cursor, the character pattern and the cursor are alternately displayed.

Note: The execution time of this instruction is 37 μs (maximum) at an oscillation frequency of 270 kHz.

5) Cursor/Display Shift

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	0	1	S/C	R/L	×	×

×: Don't Care

S/C = "0", R/L = "0" This instruction shifts left the cursor and blink positions by 1 (decrements the content of the ADC by 1).

S/C = "0", R/L = "1" This instruction shifts right the cursor and blink positions by 1 (increments the content of the ADC by 1).

S/C = "1", R/L = "0" This instruction shifts left the entire display by 1 character position. The cursor and blink positions move to the left together with the entire display. The Arbitrator display is not shifted. (The content of the ADC remains unchanged.)

S/C = "1", R/L = "1" This instruction shifts right the entire display by 1 character position. The cursor and blink positions move to the right together with the entire display. The Arbitrator display is not shifted. (The content of the ADC remains unchanged.)

In the 2-line mode, the cursor or blink moves from the first line to the second line when the cursor at digit 40 (27; hex) of the first line is shifted right.
When the entire display is shifted, the character pattern, cursor or blink will not move between the lines (from line 1 to line 2 or vice versa).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

6) Function Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	0	1	DL	N	ABE	SSR	CSR

×: Don't Care

(1) When the "DL" bit (DB_4) of this instruction is "1", the data transfer to and from the CPU is performed once by the use of 8 bits DB_7 to DB_0.
When the "DL" bit (DB_4) of this instruction is "0", the data transfer to and from the CPU is performed twice by the use of 4 bits DB_7 to DB_4.

(2) The 2-line display mode is selected when the "N" bit (DB_3) of this instruction is "1". The 1-line display mode is selected when the "N" bit is "0".
The arbitrator is displayed when the "ABE" bit (DB_2) of this instruction is "1".
The arbitrator is not displayed when the "ABE" bit (DB_2) of this instruction is "0".

(3) The transfer direction of the segment signal output data is controlled.
When the "SSR" bit (DB_1) of this instruction is "1", the data is transferred from SEG_{100} to SEG_1.
When the "SSR" bit (DB_1) of this instruction is "0", the data is transferred from SEG_1 to SEG_{100}.
The transfer direction of the common signal output data is controlled.
At 1/n duty,
When the "CSR" bit (DB_0) of this instruction is "1", the data is transferred from COMn to COM1.
When the "CSR" bit (DB_0) of this instruction is "0", the data is transferred from COM1 to COMn.

After the ML9042 is powered on, this function setting should be carried out before execution of any instruction except the Busy Flag Read. After this function setting, no instructions other than the DL Set instruction can be executed. In the Serial I/F Mode, DL setting is ignored.

N	ABE	Number of display lines	Font size	Duty	Number of biases	Number of common signals
0	0	1	5 × 8	1/8	4	8
0	1	1	5 × 8	1/9	4	9
1	0	2	5 × 8	1/16	5	16
1	1	2	5 × 8	1/17	5	17

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

7) CGRAM Address Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	0	1	C_5	C_4	C_3	C_2	C_1	C_0

This instruction sets the CGRAM address to the data represented by the bits C_5 to C_0 (binary).
The CGRAM addresses are valid until DDRAM or ABRAM addresses are set.
The CPU writes or reads character patterns starting from the one represented by the CGRAM address bits C_5 to C_0 set in the instruction code at that time.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

8) DDRAM Address Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	0	1	D_6	D_5	D_4	D_3	D_2	D_1	D_0

This instruction sets the DDRAM address to the data represented by the bits D_6 to D_0 (binary).
The DDRAM addresses are valid until CGRAM or ABRAM addresses are set.
The CPU writes or reads character codes starting from the one represented by the DDRAM address bits D_6 to D_0 set in the instruction code at that time.
In the 1-line mode (the "N" bit is "0"), the DDRAM address represented by bits D_6 to D_0 (binary) should be in the range "00" to "4F" in hexadecimal.
In the 2-line mode (the "N" bit is "1"), the DDRAM address represented by bits D_6 to D_0 (binary) should be in the range "00" to "27" or "40" to "67" in hexadecimal.
If an address other than above is input, the ML9042 cannot properly write a character code in or read it from the DDRAM.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

9) DDRAM/ABRAM/CGRAM Data Write

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	1	0	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0

A character code (E_7 to E_0) is written to the DDRAM, Display-ON data (E_7 to E_0) to the ABRAM or a character pattern (E_7 to E_0) to the CGRAM.
The DDRAM, ABRAM or CGRAM is selected at the preceding address setting.
After data is written, the address counter (ADC) is incremented or decremented as set by the Entry Mode Setting instruction (see 3).

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

10) Busy Flag/Address Counter Read (Execution time: 0 μs)

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	0	1	BF	O_6	O_5	O_4	O_3	O_2	O_1	O_0

The "BF" bit (DB7) of this instruction tells whether the ML9042 is busy in internal operation (BF = "1") or not (BF = "0").
When the "BF" bit is "1", the ML9042 cannot accept any other instructions. Before inputting a new instruction, check that the "BF" bit is "0".
When the "BF" bit is "0", the ML9042 outputs the correct value of the address counter. The value of the address counter is equal to the DDRAM, ABRAM or CGRAM address. Which of the DDRAM, ABRAM and CGRAM addresses is set in the counter is determined by the preceding address setting.
When the "BF" bit is "1", the value of the address counter is not always correct because it may have been incremented or decremented by 1 during internal operation.

11) DDRAM/ABRAM/CGRAM Data Read

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code:	1	1	1	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

A character code (P_7 to P_0) is read from the DDRAM, Display-ON data (P_7 to P_0) from the ABRAM or a character pattern (P_7 to P_0) from the CGRAM.
The DDRAM, ABRAM or CGRAM is selected at the preceding address setting.
After data is read, the address counter (ADC) is incremented or decremented as set by the Entry Mode Setting instruction (see 3).

Note: Conditions for reading correct data

(1) The DDRAM, ABRAM or CGRAM Setting instruction is input before this data read instruction is input.

(2) When reading a character code from the DDRAM, the Cursor/Display Shift instruction (see 5) is input before this Data Read instruction is input.

(3) When two or more consecutive RAM Data Read instructions are executed, the following read data is correct.
Correct data is not output under conditions other than the cases (1), (2) and (3) above.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

Expansion Instruction Codes

The busy status of the ML9042 is rather longer than the cycle time of the CPU, since the internal processing of the ML9042 starts at a timing which does not affect the display on the LCD. In the busy status (Busy Flag is "1"), the ML9042 executes the Busy Flag Read instruction only. Therefore, the CPU should ensure that the Busy Flag is "0" before sending an expansion instruction code to the ML9042.

1) Arbitrator Display Line Set

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Expansion instruction code:	0	0	0	0	0	0	0	0	0	1	AS

This expansion instruction code sets the Arbitrator display line. The relationship between the status of this bit and the common outputs is as follows:
For display examples, refer to LCD Drive Waveforms section.

ABE bit	CSR bit	duty	AS bit	Shift direction	Arbitrator's common pin
L	L	1/8	L	COM1→COM8	None
L	L	1/8	H	COM1→COM8	None
L	L	1/16	L	COM1→COM16	None
L	L	1/16	H	COM1→COM16	None
L	H	1/8	L	COM8→COM1	None
L	H	1/8	H	COM8→COM1	None
L	H	1/16	L	COM16→COM1	None
L	H	1/16	H	COM16→COM1	None
H	L	1/9	L	COM1→COM9	COM9
H	L	1/9	H	COM1→COM9	COM1
H	L	1/17	L	COM1→COM17	COM17
H	L	1/17	H	COM1→COM17	COM1
H	H	1/9	L	COM9→COM1	COM1
H	H	1/9	H	COM9→COM1	COM9
H	H	1/17	L	COM17→COM1	COM1
H	H	1/17	H	COM17→COM1	COM17

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

2) ABRAM Address Setting

	RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Expansion instruction code:	0	0	1	0	1	1	H_4	H_3	H_2	H_1	H_0

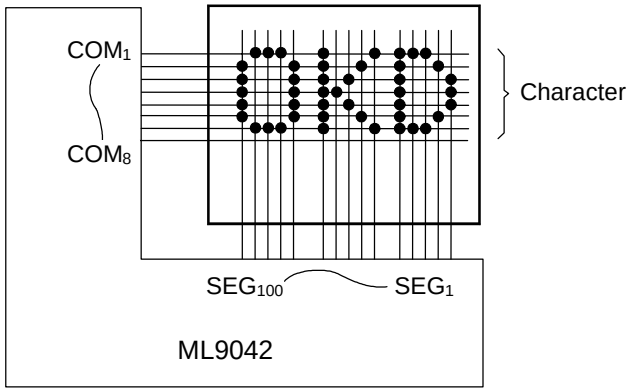
This instruction sets the ABRAM address to the data represented by the bits H_4 to H_0 (binary).
The ABRAM addresses are valid until CGRAM or DDRAM addresses are set.
The CPU writes or reads the Display-ON data starting from the one represented by the ABRAM address bits H_4 to H_0 set in the instruction code at that time.
When the ABRAM address represented by bits H_4 to H_0 (binary) is in the range "00" to "13" in hexadecimal, data is output to the LCD as the arbitrator.

Note: The execution time of this instruction is 37 μs at an oscillation frequency (OSC) of 270 kHz.

Examples of Combinations of ML9042 and LCD Panel

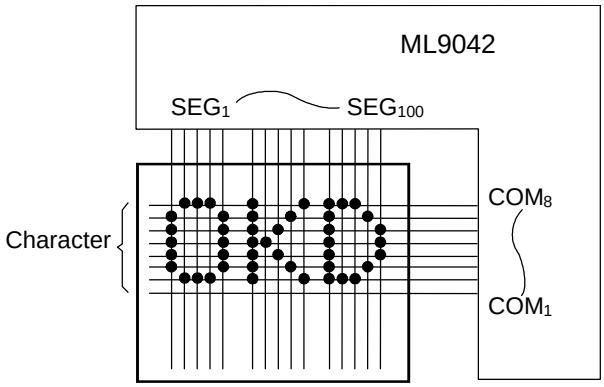
(1) Driving the LCD of one 20-character line under the conditions of the 1-line display mode and no arbitrator display

(1/8 duty, ABE = “0”, AS = “0” or “1”, CSR = “0”, SSR = “1”)



- COM_9 to COM_{17} output Display-OFF common signals.

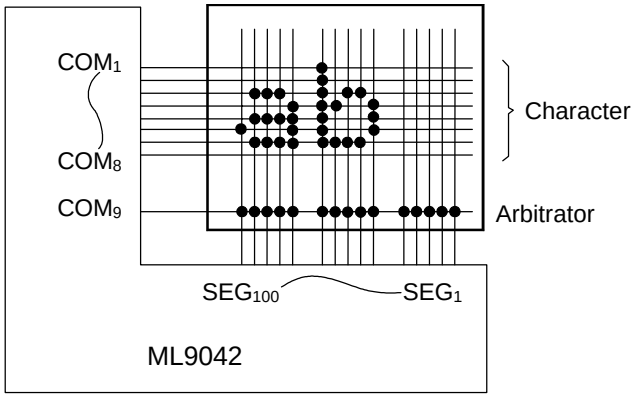
(1/8 duty, ABE = “0”, AS = “0” or “1”, CSR = “1”, SSR = “0”)



- COM_9 to COM_{17} output Display-OFF common signals.

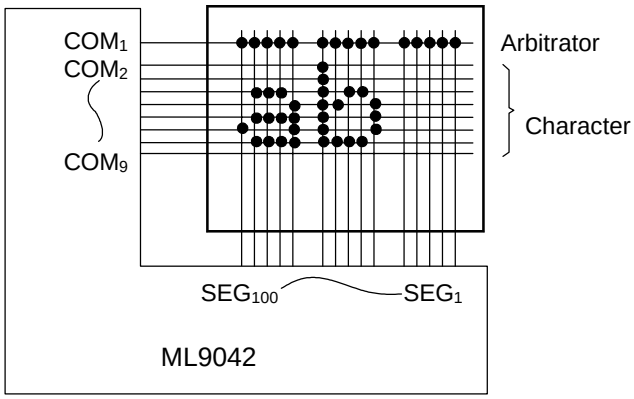
(2) Driving the LCD of one 20-character line under the conditions of the 1-line display mode and the arbitrator display

(1/9 duty, ABE = “1”, AS = “0”, CSR = “0”, SSH = “1”)



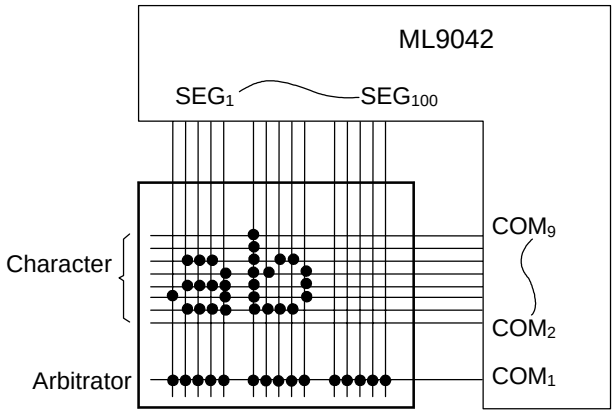
- COM_{10} to COM_{17} output Display-OFF common signals.

(1/9 duty, ABE = “1”, AS = “1”, CSR = “0”, SSR = “1”)



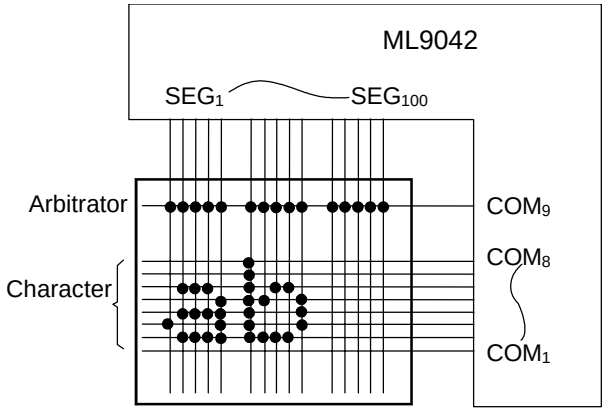
- COM_{10} to COM_{17} output Display-OFF common signals.

(1/9 duty, ABE = “1”, AS = “0”, CSR = “1”, SSR = “0”)



- COM_{10} to COM_{17} output Display-OFF common signals.

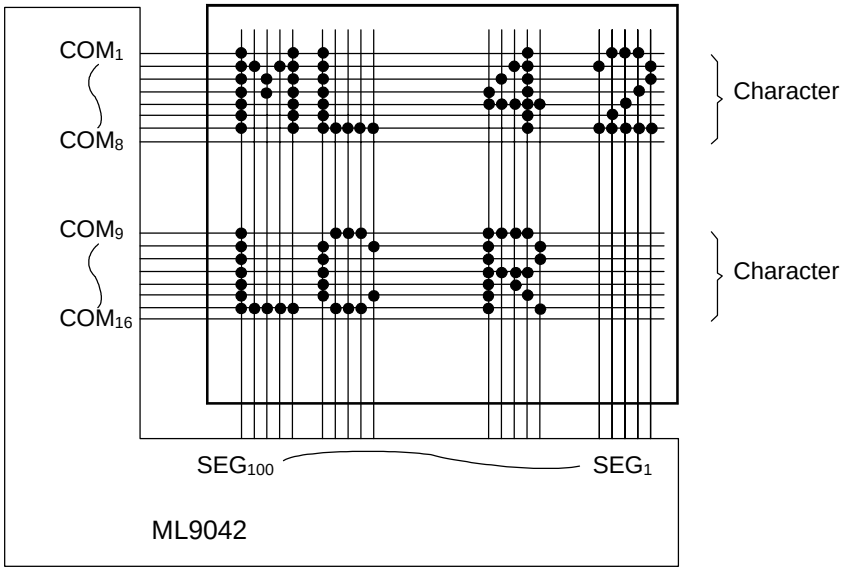
(1/9 duty, ABE = “1”, AS = “1”, CSR = “1”, SSR = “0”)



- COM_{10} to COM_{17} output Display-OFF common signals.

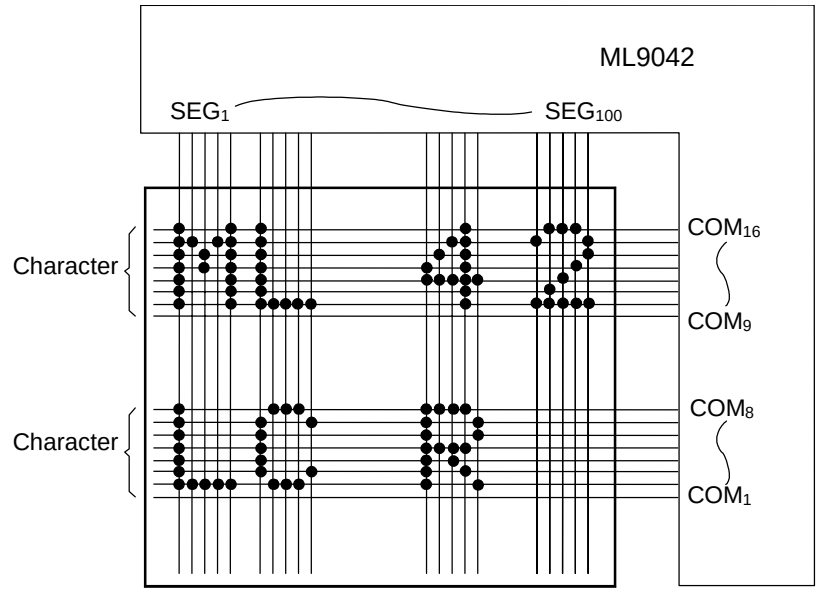
(3) Driving the LCD of two 20-character lines under the conditions of the 2-line display mode and no arbitrator display

(1/16 duty, ABE = “0”, AS = “0” or “1”, CSR = “0”, SSR = “1”)



- COM_{17} outputs Display-OFF common signal.

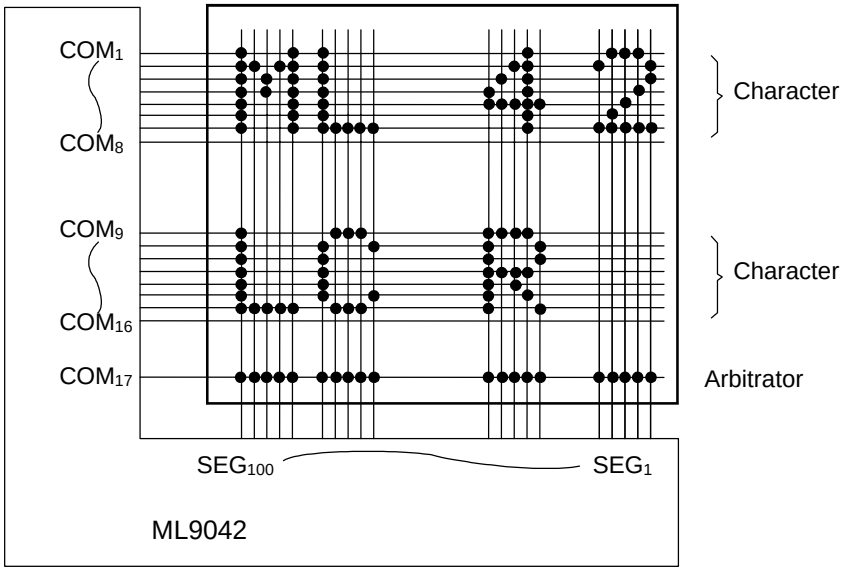
(1/16 duty, ABE = “0”, AS = “0” or “1”, CSR = “1”, SSR = “0”)



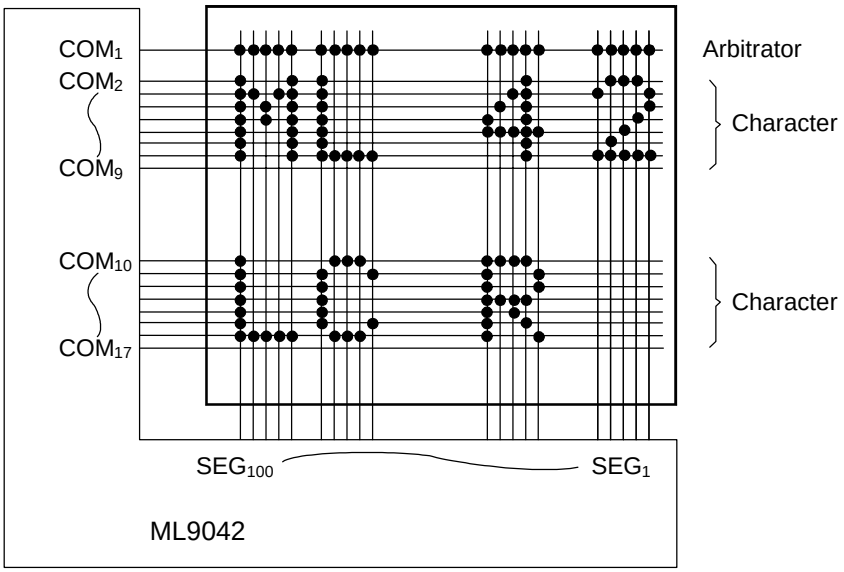
- COM_{17} outputs Display-OFF common signal.

(4) Driving the LCD of two 20-character lines under the conditions of the 2-line display mode and the arbitrator display

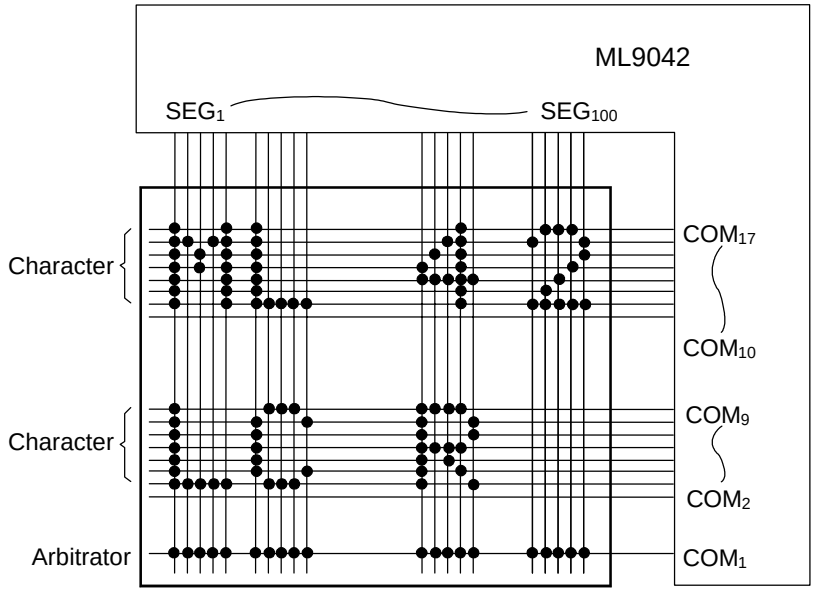
(1/17 duty, ABE = “1”, AS = “0”, CSR = “0”, SSR = “1”)



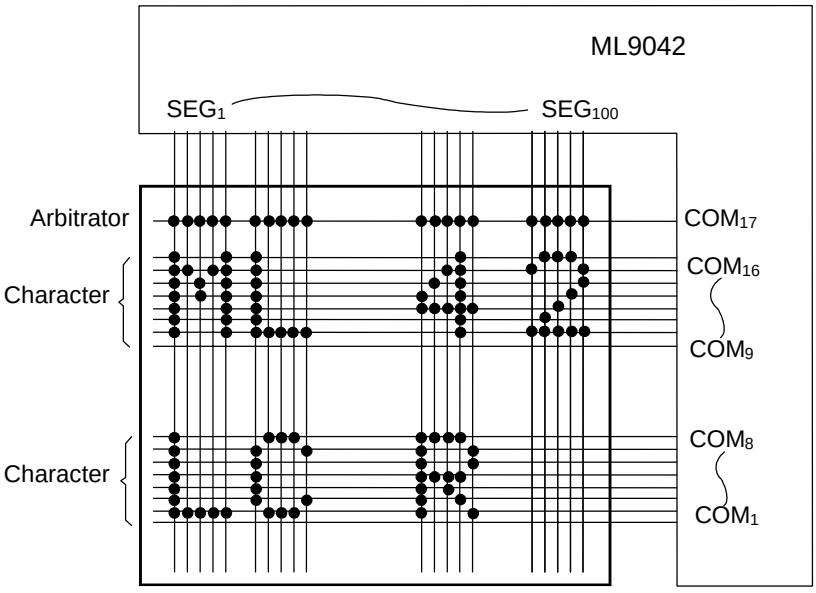
(1/17 duty, ABE = “1”, AS = “1”, CSR = “0”, SSR = “1”)



(1/17 duty, ABE = “1”, AS = “0”, CSR = “1”, SSR = “0”)

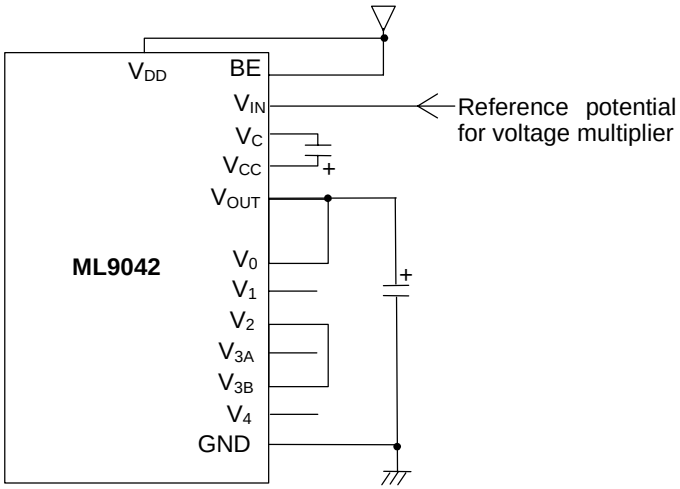


(1/17 duty, ABE = “1”, AS = “1”, CSR = “1”, SSR = “0”)

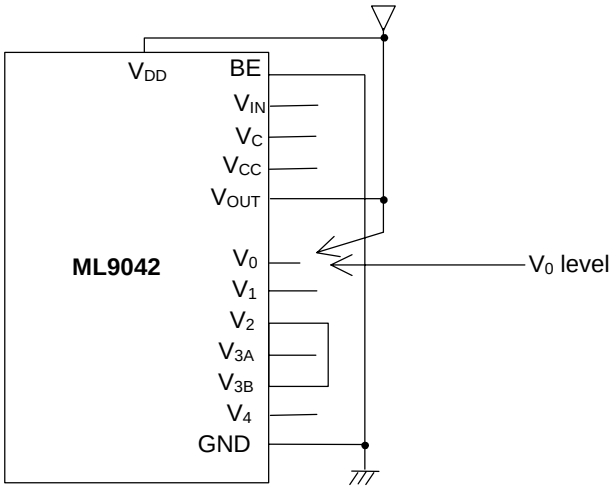


EXAMPLES OF VLCD GENERATION CIRCUITS

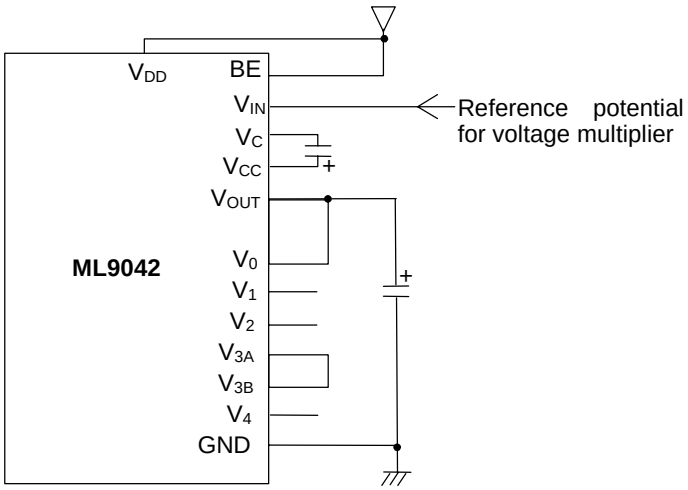
- With 1/4 bias, a voltage multiplier



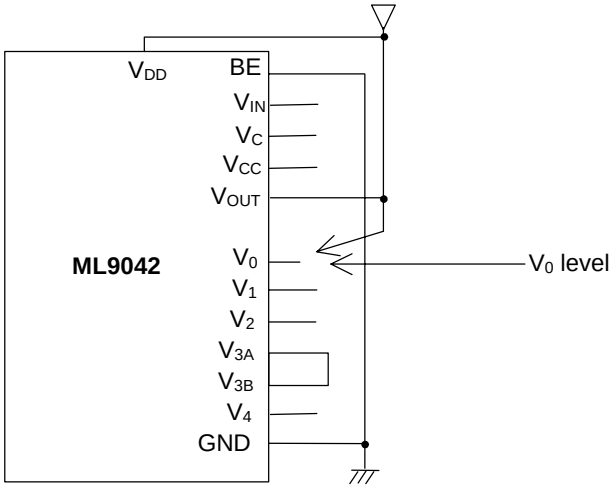
- With 1/4 bias, no voltage multiplier
  1) Apply V_{DD} to V_{OUT} and $V_{0.}$
  2) Apply V_{DD} to V_{OUT}, and apply the V_0 level to V_0 externally.



- With 1/5 bias, a voltage multiplier



- With 1/5 bias, no voltage multiplier
  1) Apply V_{DD} to V_{OUT} and $V_{0.}$
  2) Apply V_{DD} to V_{OUT}, and apply the V_0 level to V_0 externally.



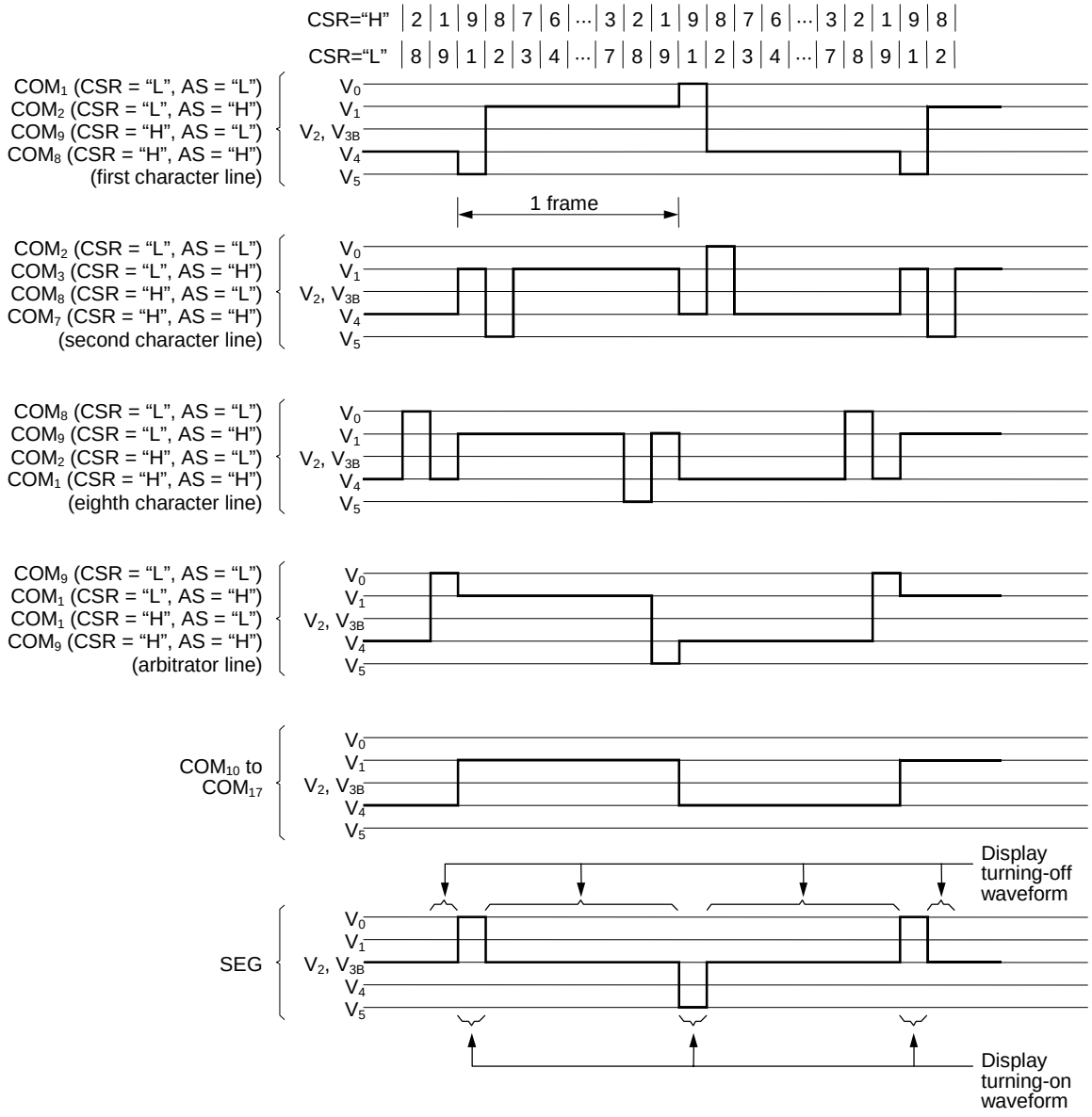
LCD Drive Waveforms

The COM and SEG waveforms (AC signal waveforms for display) vary according to the duty (1/9 and 1/17 duties). See 1) and 2) below.
The relationship between the duty ratio and the frame frequency is as follows:

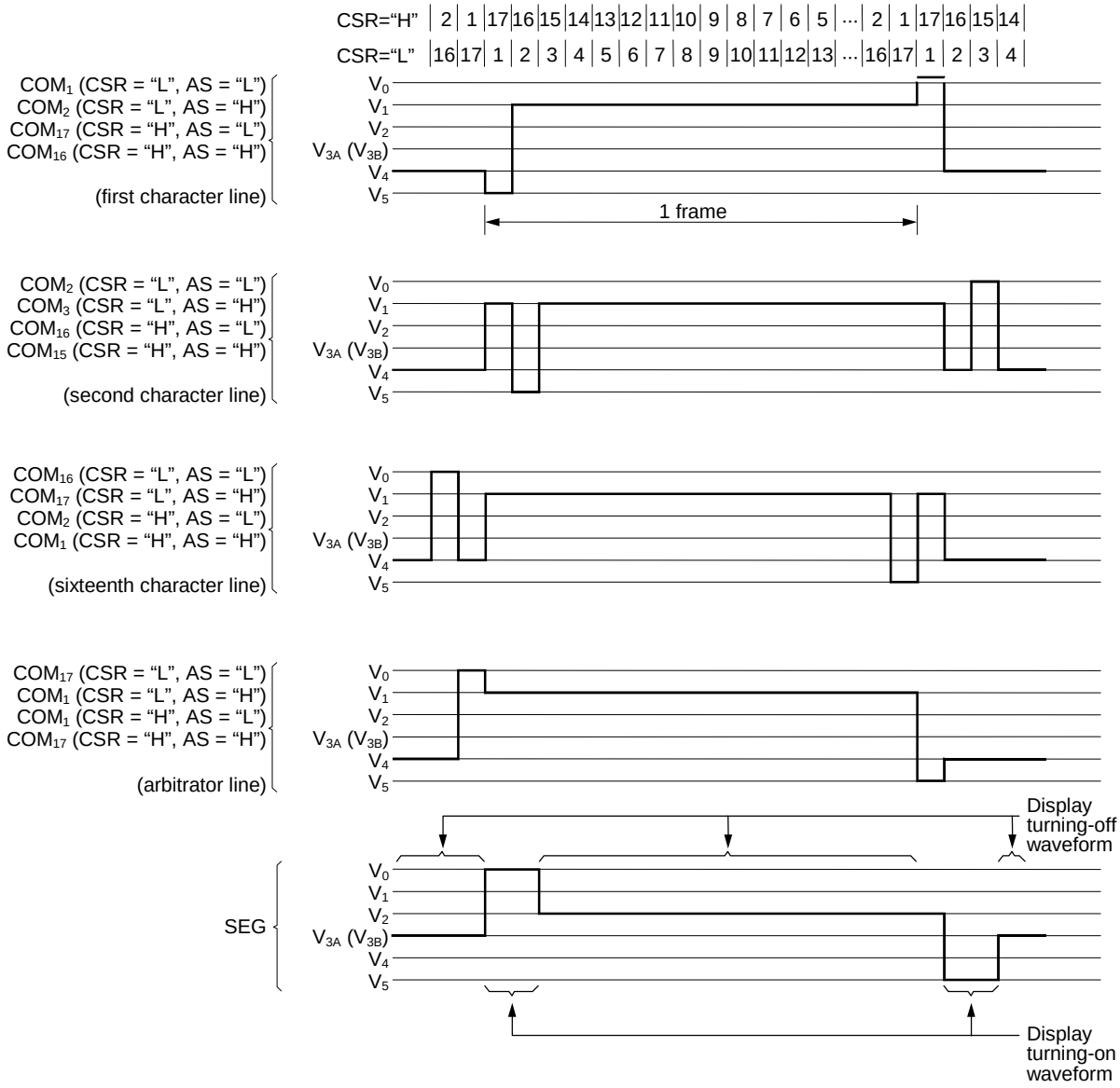
Duty ratio	Frame Frequency
1/8	84.4 Hz
1/9	75.0 Hz
1/16	84.4 Hz
1/17	79.4 Hz

Note: At an oscillation frequency (OSC) of 270 kHz

1) COM and SEG Waveforms on 1/9 Duty (ABE = "1")



2) COM and SEG Waveforms on 1/17 Duty (ABE = “1”)



Initial Setting of Instructions

(a) Data transfer from and to the CPU using 8 bits of DB_0 to DB_7

1) Turn on the power.
2) Wait for 15 ms or more after V_{DD} has reached 2.7 V or higher.
3) Set “8 bits” with the Function Setting instruction.
4) Wait for 4.1 ms or more.
5) Set “8 bits” with the Function Setting instruction.
6) Wait for 100 μs or more.
7) Set “8 bits” with the Function Setting instruction.
8) Check the Busy Flag for No Busy (or wait for 100 μs or more).
9) Set “8 bits”, “Number of LCD lines” and “Font size” with the Function Setting instruction. (After this, the number of LCD lines and the font size cannot be changed.)
10) Check the Busy Flag for No Busy.
11) Execute the Display ON/OFF control Instruction, Display Clear Instruction, Entry Mode Setting instruction and Arbitrator Display Line Setting Instruction.
12) Check the Busy Flag for No Busy.
13) Initialization is completed.

An example of instruction code for 3), 5) and 7)

RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
1	0	0	0	0	1	1	×	×	×	×

×: Don’t Care

(b) Data transfer from and to the CPU using 4 bits of DB_4 to DB_7

1) Turn on the power.
2) Wait for 15 ms or more after V_{DD} has reached 2.7 V or higher.
3) Set “8 bits” with the Function Setting instruction.
4) Wait for 4.1 ms or more.
5) Set “8 bits” with the Function Setting instruction.
6) Wait for 100 μs or more.
7) Set “8 bits” with the Function Setting instruction.
8) Check the Busy Flag for No Busy (or wait for 100 μs or longer).
9) Set “4 bits” with the Function Setting instruction.
10) Wait for 100 μs or longer.
11) Set “4 bits”, “Number of LCD lines” and “Font size” with the Function Setting instruction. (After this, the number of LCD lines and the font size cannot be changed.)
12) Check the Busy Flag for No Busy.
13) Execute the Display ON/OFF control Instruction, Display Clear Instruction, Entry Mode Setting instruction and Arbitrator Display Line Setting Instruction.
14) Check the Busy Flag for No Busy.
15) Initialization is completed.

An example of instruction code for 3), 5) and 7)

RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4
1	0	0	0	0	1	1

An example of instruction code for 9)

RS_1	RS_0	$R/\overline{W}$	DB_7	DB_6	DB_5	DB_4
1	0	0	0	0	1	0

*: From 11), input data twice by the use of 4-bit data.
*: In 13), check the Busy Flag for No Busy before executing each instruction.

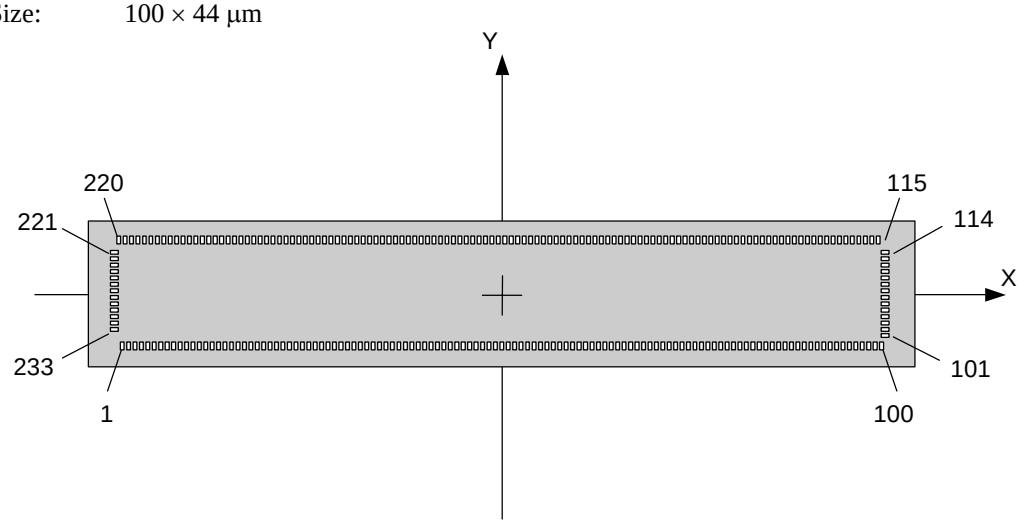
(c) Data transfer from and to the CPU using the serial I/F
1) Turn on the power.
2) Wait for 15 ms or more after V_{DD} has reached 2.7 V or higher.
3) Check the busy flag for No Busy.
4) Set “Number of LCD lines” and “Font size” with the Function Setting Instruction. (After this, the number of LCD lines and the font size cannot be changed.)
5) Check the busy flag for No Busy.
6) Execute the Display ON/OFF control Instruction, the Display Clear Instruction, the Entry Mode Instruction and the Arbitrator Display Line Setting Instruction.
7) Check the busy flag for No Busy.
8) Initialization is completed.

*: In 6), check the Busy Flag for No Busy before executing each instruction.

ML9042-xx CVWA/DVWA PAD CONFIGURATION

Pad Layout

Chip Size: 7.8 × 1.8 mm
Chip Thickness: 625±20 μm
Bump Size: 100 × 44 μm



Pad Coordinates

Pad	Symbol	X (μm)	Y (μm)	Pad	Symbol	X (μm)	Y (μm)
1	DUMMY	-3750	–750	21	DUMMY	-2250	–750
2	OSC2	-3675	–750	22	E/SHTB	-2175	–750
3	OSCR5	-3600	–750	23	E/SHTB	-2100	–750
4	OSCR3	-3525	–750	24	DUMMY	-2025	–750
5	OSC1	-3450	–750	25	DUMMY	-1950	–750
6	DUMMYGND	-3375	–750	26	DB0/SO	-1875	–750
7	T1	-3300	–750	27	DB0/SO	-1800	–750
8	T2	-3225	–750	28	DUMMY	-1725	–750
9	T3	-3150	–750	29	DUMMY	-1650	–750
10	ROM1S	-3075	–750	30	DB1	-1575	–750
11	$DUMMYV_{DD}$	-3000	–750	31	DB1	-1500	–750
12	RS1	-2925	–750	32	DUMMY	-1425	–750
13	RS1	-2850	–750	33	DUMMY	-1350	–750
14	RSO/CSB	-2775	–750	34	DB2	-1275	–750
15	RSO/CSB	-2700	–750	35	DB2	-1200	–750
16	DUMMY	-2625	–750	36	DUMMY	-1125	–750
17	DUMMY	-2550	–750	37	DUMMY	-1050	–750
18	RW/SI	-2475	–750	38	DB3	-975	–750
19	RW/SI	-2400	–750	39	DB3	-900	–750
20	DUMMY	-2325	–750	40	DUMMY	-825	–750

Pad	Symbol	X (μm)	Y (μm)
41	DUMMY	-750	–750
42	DB4	-675	–750
43	DB4	-600	–750
44	DUMMY	-525	–750
45	DUMMY	-450	–750
46	DB5	-375	–750
47	DB5	-300	–750
48	DUMMY	-225	–750
49	DUMMY	-150	–750
50	DB6	-75	–750
51	DB6	0	–750
52	DUMMY	75	–750
53	DUMMY	150	–750
54	DB7	225	–750
55	DB7	300	–750
56	DUMMYV_{DD}	375	–750
57	SP	450	–750
58	GND	525	–750
59	GND	600	–750
60	GND	675	–750
61	GND	750	–750
62	GND	825	–750
63	GND	900	–750
64	BE	975	–750
65	V_{DD}	1050	–750
66	V_{DD}	1125	–750
67	V_{DD}	1200	–750
68	V_{DD}	1275	–750
69	V_{DD}	1350	–750
70	V_{DD}	1425	–750
71	$TEST_{IN}$	1500	–750
72	$TEST_{IN}$	1575	–750
73	$TEST_{OUT}$	1650	–750
74	$TEST_{OUT}$	1725	–750
75	V_{IN}	1800	–750
76	V_{IN}	1875	–750
77	V_{OUT}	1950	–750
78	V_{OUT}	2025	–750
79	V0	2100	–750
80	V0	2175	–750

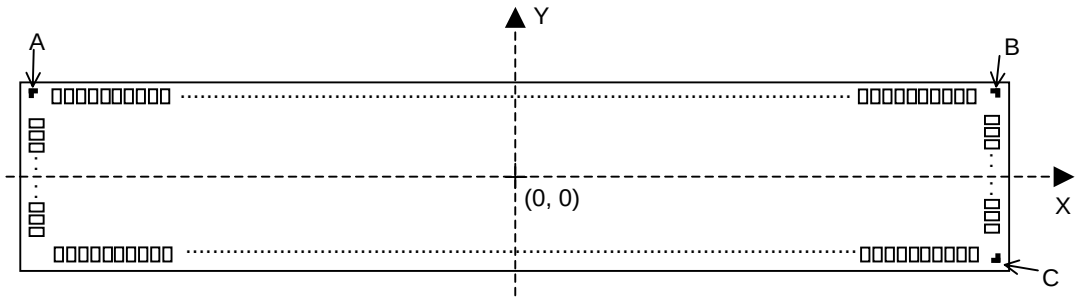
Pad	Symbol	X (μm)	Y (μm)
81	V0	2250	-750
82	V0	2325	-750
83	V0	2400	-750
84	V0	2475	-750
85	V1	2550	-750
86	V2	2625	-750
87	V2	2700	-750
88	V3A	2775	-750
89	V3A	2850	-750
90	V3B	2925	-750
91	V3B	3000	-750
92	V4	3075	-750
93	V_C	3150	-750
94	V_C	3225	-750
95	V_C	3300	-750
96	V_C	3375	-750
97	V_{CC}	3450	-750
98	V_{CC}	3525	-750
99	V_{CC}	3600	-750
100	DUMMY	3675	-750
101	DUMMY	3750	-462
102	COM_{17}	3750	-392
103	COM_{16}	3750	-322
104	COM_{15}	3750	-252
105	COM_{14}	3750	-182
106	COM_{13}	3750	-112
107	COM_{12}	3750	-42
108	COM_{11}	3750	28
109	COM_{10}	3750	98
110	COM_9	3750	168
111	DUMMY	3750	238
112	DUMMY	3750	308
113	DUMMY	3750	378
114	DUMMY	3750	448
115	DUMMY	3675	750
116	DUMMY	3605	750
117	DUMMY	3535	750
118	SEG_{100}	3465	750
119	SEG_{99}	3395	750
120	SEG_{98}	3325	750

Pad	Symbol	X (μm)	Y (μm)	Pad	Symbol	X (μm)	Y (μm)
121	SEG_{97}	3255	750	161	SEG_{57}	455	750
122	SEG_{96}	3185	750	162	SEG_{56}	385	750
123	SEG_{95}	3115	750	163	SEG_{55}	315	750
124	SEG_{94}	3045	750	164	SEG_{54}	245	750
125	SEG_{93}	2975	750	165	SEG_{53}	175	750
126	SEG_{92}	2905	750	166	SEG_{52}	105	750
127	SEG_{91}	2835	750	167	SEG_{51}	35	750
128	SEG_{90}	2765	750	168	SEG_{50}	-35	750
129	SEG_{89}	2695	750	169	SEG_{49}	-105	750
130	SEG_{88}	2625	750	170	SEG_{48}	-175	750
131	SEG_{87}	2555	750	171	SEG_{47}	-245	750
132	SEG_{86}	2485	750	172	SEG_{46}	-315	750
133	SEG_{85}	2415	750	173	SEG_{45}	-385	750
134	SEG_{84}	2345	750	174	SEG_{44}	-455	750
135	SEG_{83}	2275	750	175	SEG_{43}	-525	750
136	SEG_{82}	2205	750	176	SEG_{42}	-595	750
137	SEG_{81}	2135	750	177	SEG_{41}	-665	750
138	SEG_{80}	2065	750	178	SEG_{40}	-735	750
139	SEG_{79}	1995	750	179	SEG_{39}	-805	750
140	SEG_{78}	1925	750	180	SEG_{38}	-875	750
141	SEG_{77}	1855	750	181	SEG_{37}	-945	750
142	SEG_{76}	1785	750	182	SEG_{36}	-1015	750
143	SEG_{75}	1715	750	183	SEG_{35}	-1085	750
144	SEG_{74}	1645	750	184	SEG_{34}	-1155	750
145	SEG_{73}	1575	750	185	SEG_{33}	-1225	750
146	SEG_{72}	1505	750	186	SEG_{32}	-1295	750
147	SEG_{71}	1435	750	187	SEG_{31}	-1365	750
148	SEG_{70}	1365	750	188	SEG_{30}	-1435	750
149	SEG_{69}	1295	750	189	SEG_{29}	-1505	750
150	SEG_{68}	1225	750	190	SEG_{28}	-1575	750
151	SEG_{67}	1155	750	191	SEG_{27}	-1645	750
152	SEG_{66}	1085	750	192	SEG_{26}	-1715	750
153	SEG_{65}	1015	750	193	SEG_{25}	-1785	750
154	SEG_{64}	945	750	194	SEG_{24}	-1855	750
155	SEG_{63}	875	750	195	SEG_{23}	-1925	750
156	SEG_{62}	805	750	196	SEG_{22}	-1995	750
157	SEG_{61}	735	750	197	SEG_{21}	-2065	750
158	SEG_{60}	665	750	198	SEG_{20}	-2135	750
159	SEG_{59}	595	750	199	SEG_{19}	-2205	750
160	SEG_{58}	525	750	200	SEG_{18}	-2275	750

Pad	Symbol	X (μm)	Y (μm)
201	SEG_{17}	-2345	750
202	SEG_{16}	-2415	750
203	SEG_{15}	-2485	750
204	SEG_{14}	-2555	750
205	SEG_{13}	-2625	750
206	SEG_{12}	-2695	750
207	SEG_{11}	-2765	750
208	SEG_{10}	-2835	750
209	SEG_{9}	-2905	750
210	SEG_{8}	-2975	750
211	SEG_{7}	-3045	750
212	SEG_{6}	-3115	750
213	SEG_{5}	-3185	750
214	SEG_{4}	-3255	750
215	SEG_{3}	-3325	750
216	SEG_{2}	-3395	750
217	SEG_{1}	-3465	750
218	DUMMY	-3535	750
219	DUMMY	-3605	750
220	DUMMY	-3675	750
221	DUMMY	-3750	448
222	DUMMY	-3750	378
223	DUMMY	-3750	308
224	DUMMY	-3750	238
225	COM_{1}	-3750	168
226	COM_{2}	-3750	98
227	COM_{3}	-3750	28
228	COM_{4}	-3750	-42
229	COM_{5}	-3750	-112
230	COM_{6}	-3750	-182
231	COM_{7}	-3750	-252
232	COM_{8}	-3750	-322
233	DUMMY	-3750	-392

ML9042-xx CVWA/DVWA ALIGNMENT MARK SPECIFICATION

Alignment Mark Coordinates



Alignment Mark	X (μm)	Y (μm)
A	–3770	770
B	3770	770
C	3770	–770

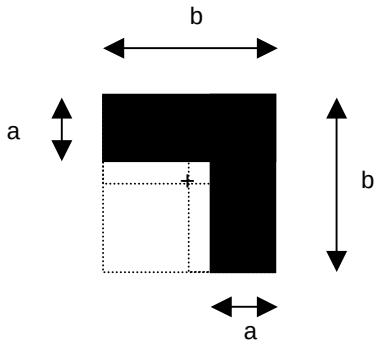
The coordinates (X, Y) indicate the distances to the center of an alignment mark (the center of the maximum outline of the L shape).

Alignment Mark Layer

Gold bump

Alignment Mark Gold Bump Specification

Symbol	Parameter	Mark	Size (μm)
a	Alignment Mark Width	A, B, C	30
b	Alignment Mark Size	A, B, C	80



ML9042-xx CVWA GOLD BUMP SPECIFICATION (HIGH HARDNESS)

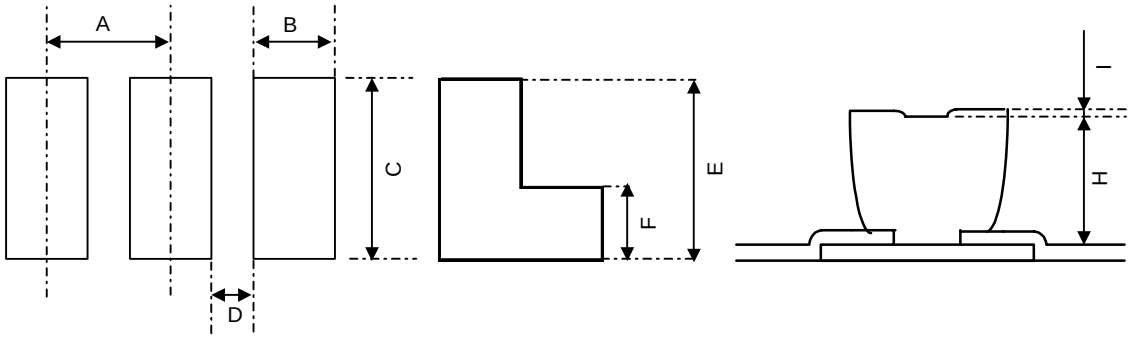
Gold Bump Specification

(Unit: μm)

Symbol	Parameter	MIN	TYP	MAX
A	Bump Pitch (I/O Section: Pitch Direction)	70	—	—
B	Bump Size (I/O Section: Pitch Direction)	40	44	48
C	Bump Size (I/O Section: Depth Direction)	96	100	104
D	Bump-to-Bump Distance (I/O Section: Pitch Direction)	22	26	30
E	Bump Size (L-mark Section: Length)	76	80	84
F	Bump Size (L-mark Section: Width)	26	30	34
G	Sliding of Total Bump Pitches	—	—	2
H	Bump Height	10	15	20
	Bump Height Dispersion Inside Chip (Range)	—	—	4
I	Bump Edge Height	—	—	5
J	Shear Strength (g)	27	—	—
K	Bump Hardness (Hv: 25 g load)	50	90	130

■ Wafer Thickness; 625 ±20 μm
■ Chip Size; 7.80 mm × 1.80 mm

Top View and Cross Section View



[I/O Section] [L-Alignment Mark] [Cross Section View]

ML9042-xx CVWA GOLD BUMP SPECIFICATION (LOW HARDNESS)

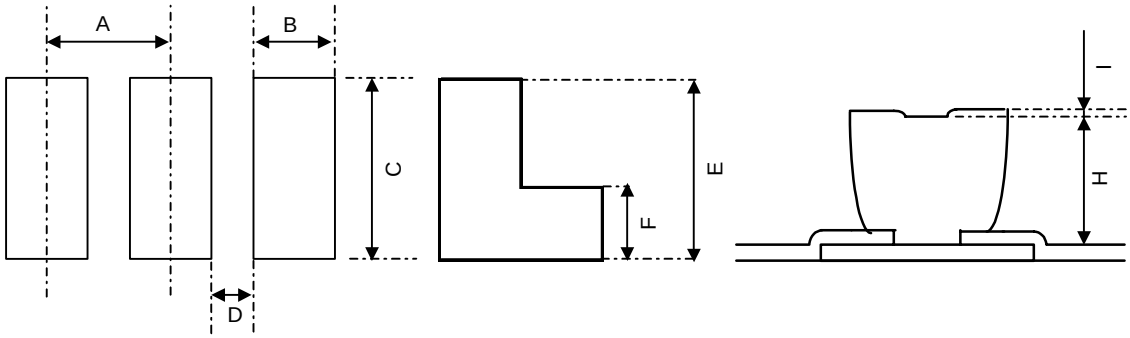
Gold Bump Specification

(Unit: μm)

Symbol	Parameter	MIN	TYP	MAX
A	Bump Pitch (I/O Section: Pitch Direction)	70	—	—
B	Bump Size (I/O Section: Pitch Direction)	40	44	48
C	Bump Size (I/O Section: Depth Direction)	96	100	104
D	Bump-to-Bump Distance (I/O Section: Pitch Direction)	22	26	30
E	Bump Size (L-mark Section: Length)	76	80	84
F	Bump Size (L-mark Section: Width)	26	30	34
G	Sliding of Total Bump Pitches	—	—	2
H	Bump Height	10	15	20
	Bump Height Dispersion Inside Chip (Range)	—	—	4
I	Bump Edge Height	—	—	5
J	Shear Strength (g)	27	—	—
K	Bump Hardness (Hv: 25 g load)	30	—	80

■ Wafer Thickness; 625 ±20 μm
■ Chip Size; 7.80 mm × 1.80 mm

Top View and Cross Section View



[I/O Section] [L-Alignment Mark] [Cross Section View]

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9042-01	Jun. 16, 2003	–	–	Preliminary first edition
FEDL9042-01	Nov. 19, 2003	5	5	Changed descriptions of Symbols V_C and V_{CC}
		8	8	Changed DC Characteristics Condition VDD = 4.5 to 5.5V→VDD = 4.0 to 5.5V Ta = 25°C→Ta =- 20 to 75°C Spec Min. 175 Typ. 270 Max. 365 →Min. 200 Typ. 270 Max. 351 Min. 175 Typ. 270 Max. 365 →Min. 200 Typ. 280 Max. 364
		25	25	Added of table
		44	44	Partially changed figure of generation circuits (V_C+)→(V_{CC}+) and V_2,V_{3A},V_{3B}
		45	45	Partially changed figure of generation circuits (V_C+)→(V_{CC}+)

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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