MN3890S

NTSC-Compatible CCD 1 H Video Signal Delay Element

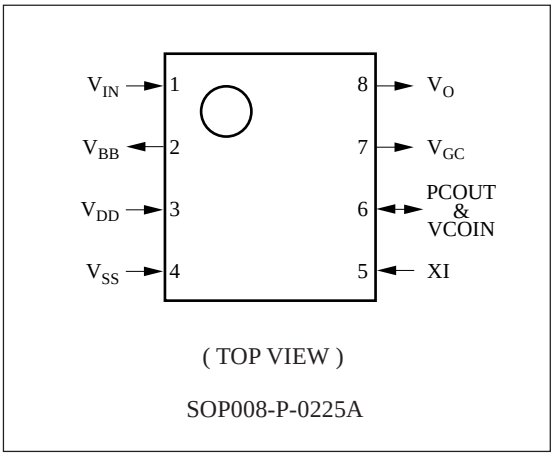
■ Overview

The MN3890S is a 1 H image delay element of a 4 f_{SC} CMOS CCD and suitable for video signal processing applications.

It contains such components as a frequency-doubler circuit, a shift register clock driver, a 906-stage CCD analog shift register, and a resampling output amplifier.

The MN3885S drives and samples the 906-stage analog shift register using a redoubled version of the supplied clock signal with a frequency 7.16 MHz of twice the NTSC color signal subcarrier frequency, and after adding in the attached filter delay, produces a delay of 1 H (the horizontal scan period).

■ Pin Assignment



(TOP VIEW)

SOP008-P-0225A

■ Features

- Single 5.0 V power supply
- Energy-saving design based on CMOS process
- Low EMI levels from clock during driving

■ Applications

- VCRs, Video cameras

■ Structure and Operation

The MN3890S consists of the operational blocks shown in the block diagram.

- Frequency-doubler circuit

When the 7.16 MHz of the doubled NTSC color signal subcarrier frequency is inputted from the clock input pin XI, 14.32 MHz clock of fourfold frequency of color signal subcarrier is generated by this circuit.

- Clock driver

This block generates two transfer clock signals, ø1 and ø2, synchronized with the 14.32 MHz clock signal from the frequency-doubler circuit.

It also generates the sampling clock signals øS and øS', resampling clock signal øSH, and reset clock signal øR that have adjusted timing relations with ø1 and ø2.

- CCD analog shift register

This block first converts the analog signal from the V_{IN} input signal pin into a voltage signal, and inputs it into 906-stage analog shift register.

The shift register samples the shift register input with the sampling clock øS, and converts the results to charges, and uses transfer clocks ø1 and ø2 to transfer the results to the following block, the charge detection block, where the charges is converted into a voltage signal.

- Resampling output amplifier

In the output amplifier, this voltage signal is done Sample-and-Hold by resampling, and Y-signal as it is outputted at Vo.

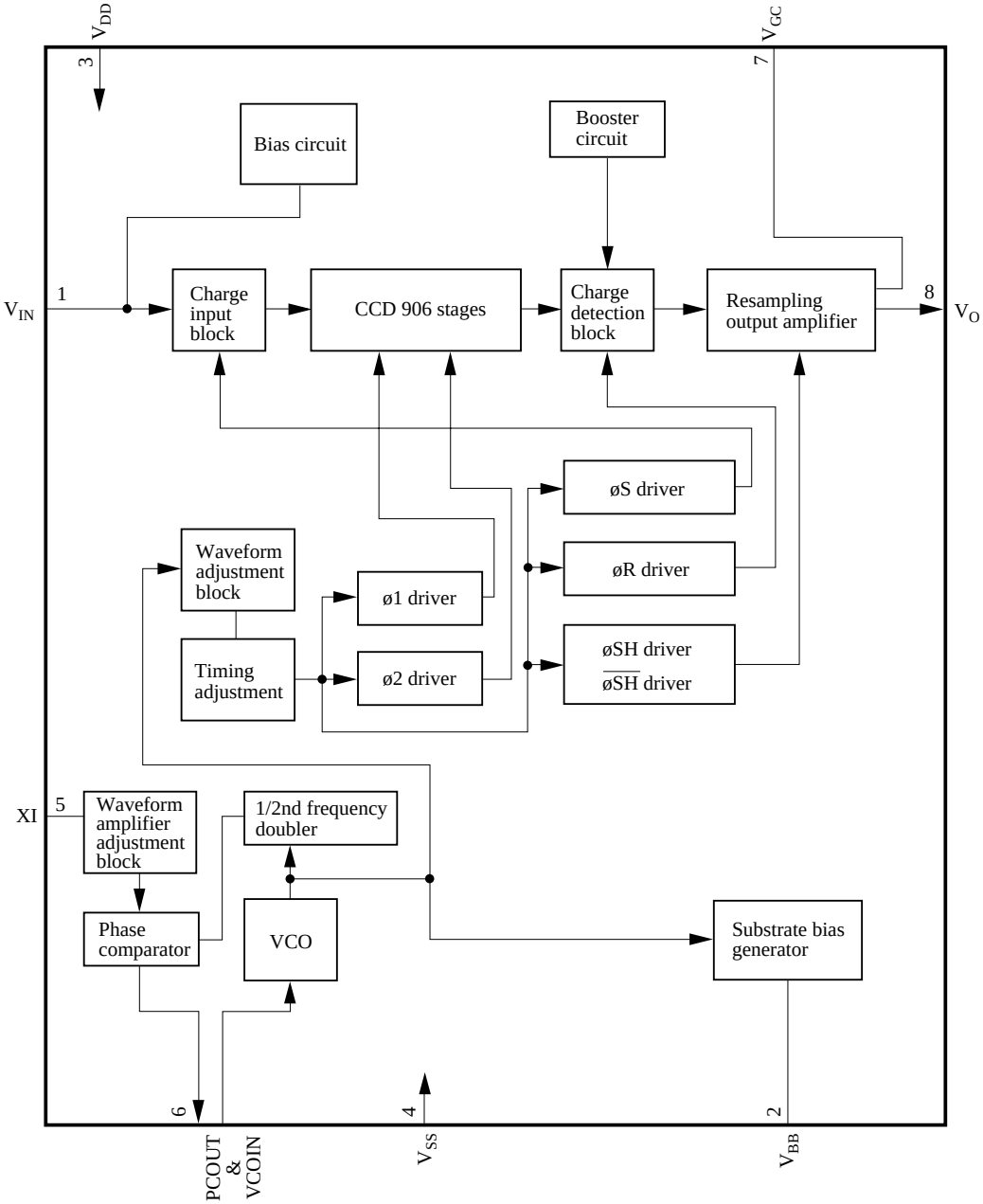
- Operation

The following is an explanation of delay line operation.

The waveforms driving the shift registers are as shown in the timing chart on page 622.

The input signal voltage sampled during the interval between t=0 and t=τc (where τc is one-half the sampling interval) appears at the V_O output pin at the point t=1813τc.

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description	Remarks
1	V_{IN}	Signal input pin	
2	V_{BB}	Substrate connection pin	Negative voltage pin
3	V_{DD}	Power supply	
4	V_{SS}	Ground	
5	XI	7.16 MHz clock input pin	
6	PCOUT & VCOIN	Phase comparator output and voltage controlled oscillator input	
7	V_{GC}	Output gate connection pin	
8	V_O	Signal output pin	

■ Operating Conditions

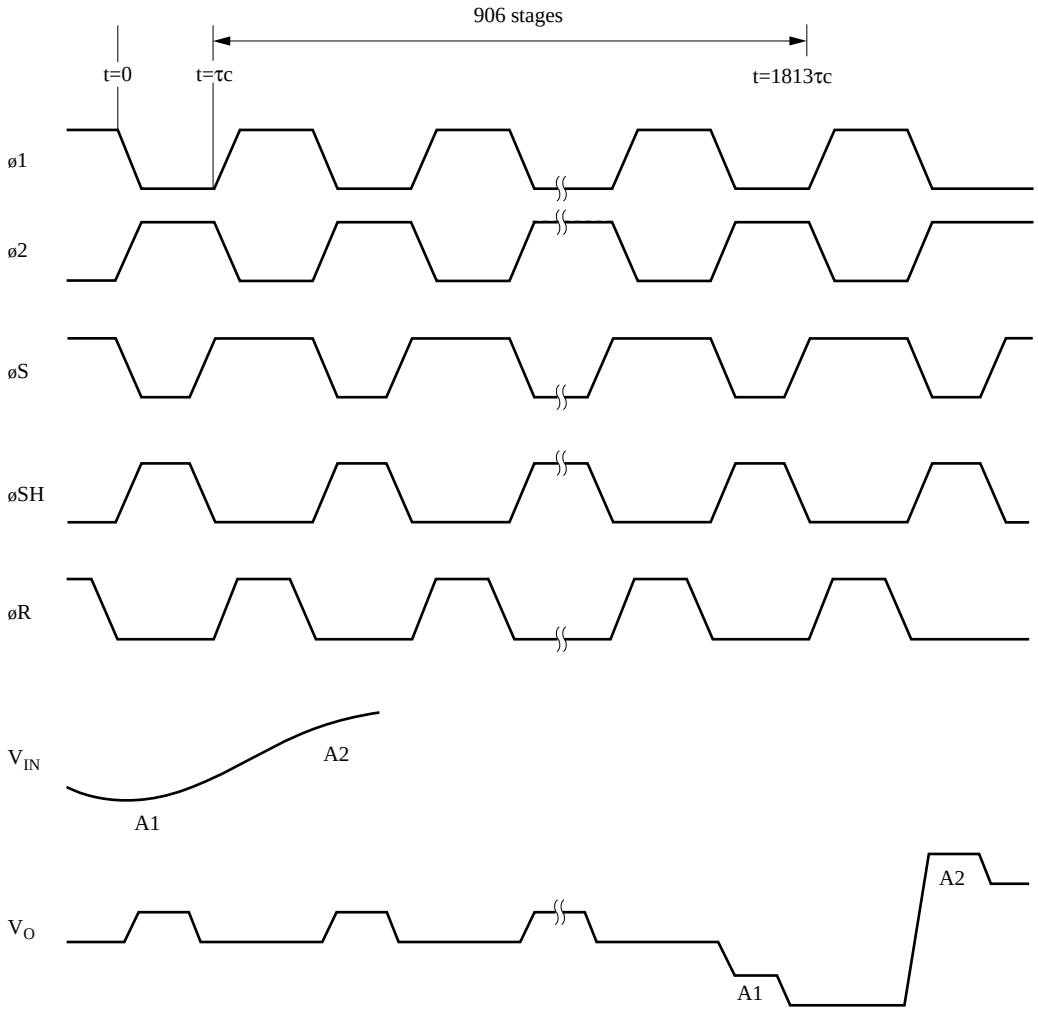
Parameter	Symbol	min	typ	max	Unit
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Input clock frequency	f_{ck}		7.15909		MHz
Signal bandwidth Input clock amplitude (sine wave)	V_{ck}	0.2	0.3	1.0	V_{P-P}
Ambient temperature	Ta	–20		60	˚C

■ Electrical Characteristics

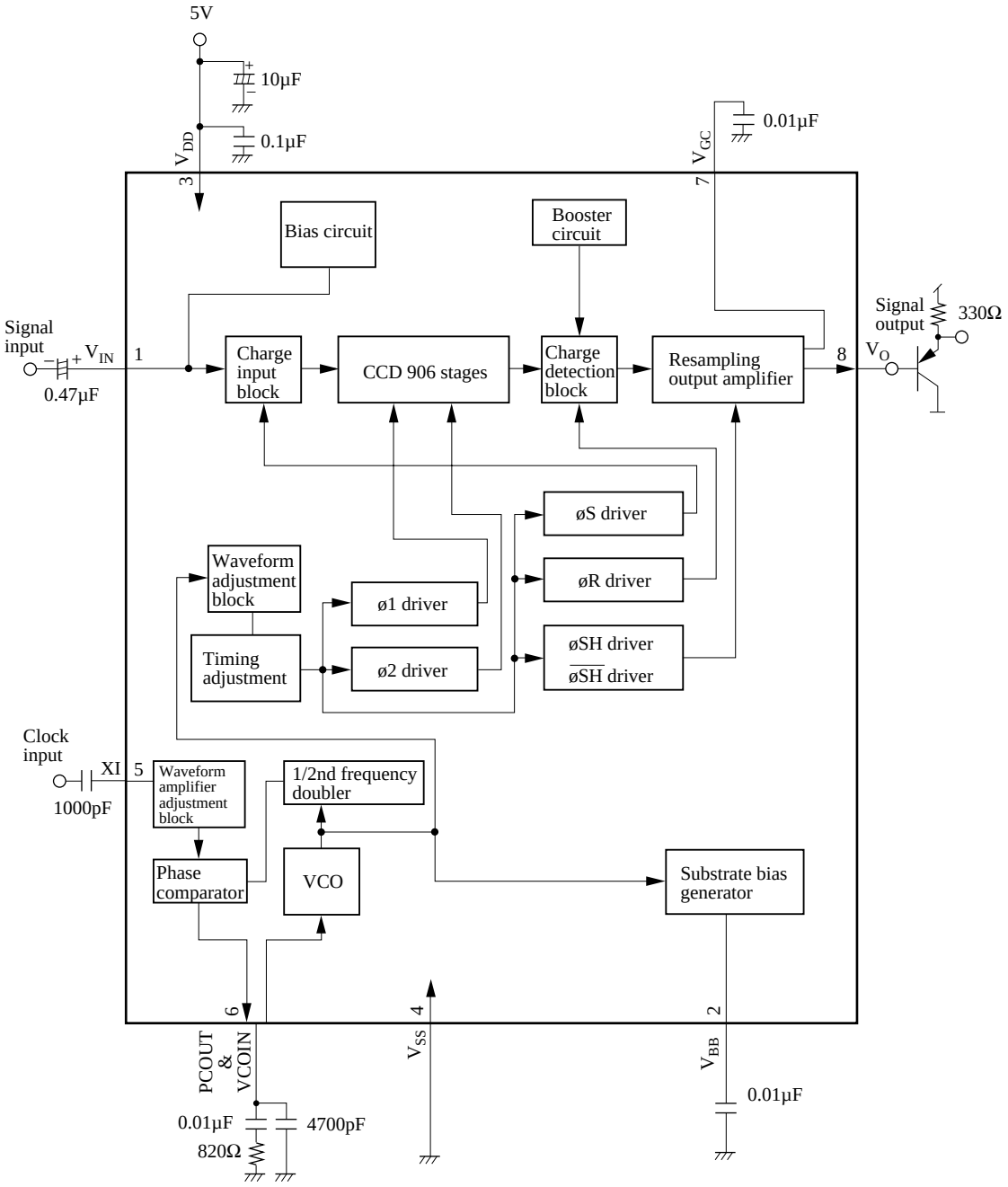
V_{DD}=5.0V, V_{ck}=0.3V_{P-P} (sine wave), V_{in}=0.5V_{P-P} (sine wave), f_{ck}=7.15909MHz, f_{sig}=200kHz, Ta=25˚C

Parameter	Symbol	Conditions	min	typ	max	Unit
Power supply current	I_{DD}			23	46	mA
Signal bandwidth	BW	–3 dB for 200 kHz value	2.5	5.5		MHz
Insertion gain	IG	f_{sig}=200kHz	–1.5	1.5	4.5	dB
Total harmonic distortion	THD	f_{sig}=200kHz		1	4.5	%
Signal-to-noise ratio	S/N	Signal output (V_{P-P})/noise output (rms)	48	56		dB
Clock leak 1	NC1	7.16 MHz component/main output signal		–50	–40	dB
Clock leak 2	NC2	14.32 MHz component/main output signal		–20	–10	dB
Delay	τ_D			63.32		µs
Output impedance	Zo			0.5	0.9	kΩ
Input bias voltage	V_{BIN}	Applied to input from V_{IN} signal input pin		2.85		V
Output bias voltage	V_{BO}	Applied to output from V_O signal output pin		2.85		V
Substrate voltage	$–V_{BB}$			–2.8		V

■ Timing Chart



■ Application Circuit Example



■ Package Dimensions (Unit:mm)

SOP008-P-0225A