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MVTX1100

9-Port Home PNA Packet Concentrator

Data Sheet

November 2003

Features

- 8 1/10 Mbps Serial ports direct interface with Home PNA PHY or 8 10/100 Mbps RMII ports
- Ideal for MDU (Multiple Dwelling Unit) application with Home PNA PHY
- 1 10/100 Mbps auto-negotiating MII/serial port (port 8) that can be used as uplink port
- Up to 8 port-based VLANs can be configured from EEPROM
- Internal 1 k MAC address table
  - Auto address learning
  - Auto address aging
- Leading edge QoS capabilities provided based on 802.1 p and IP TOS/DS field
  - 2 queues per output port
  - Packet scheduling based on Weighted Round-Robin (WRR)
  - Weighted Random Early Detection/Drop (WRED) to drop packets during traffic congestion
  - 2 levels of packet drop provided
- Supports both Full/Half duplex ports
- Full wire-speed layer 2 switching on all ports

Ordering Information

MVTX1100AL 208 Pin PQFP

-40°C to +85°C

- Ability to support WinSock 2.0 and Windows 98 & Windows 2000 smart applications
- Transmit delay control capabilities
  - Provides maximum delay guarantee (<1 ms)(Last bit in to first bit out)
  - Supports mixed voice-data networks
- Support Concentrator mode
- Ports 0 & 1 can be trunked to provide a 2x1/10 Mbps link to another switch or server
- Utilizes a single low-cost external pipelined, SyncBurst SRAM (SBRAM) for buffer memory
  - 56 k bytes or 512 k bytes (1 chip)
- External I^2C EEPROM for power-up configuration
- Support external parallel port for configuration updates
- Optimized pin-out for easy board layout
- Packaged in a 208 PQFP

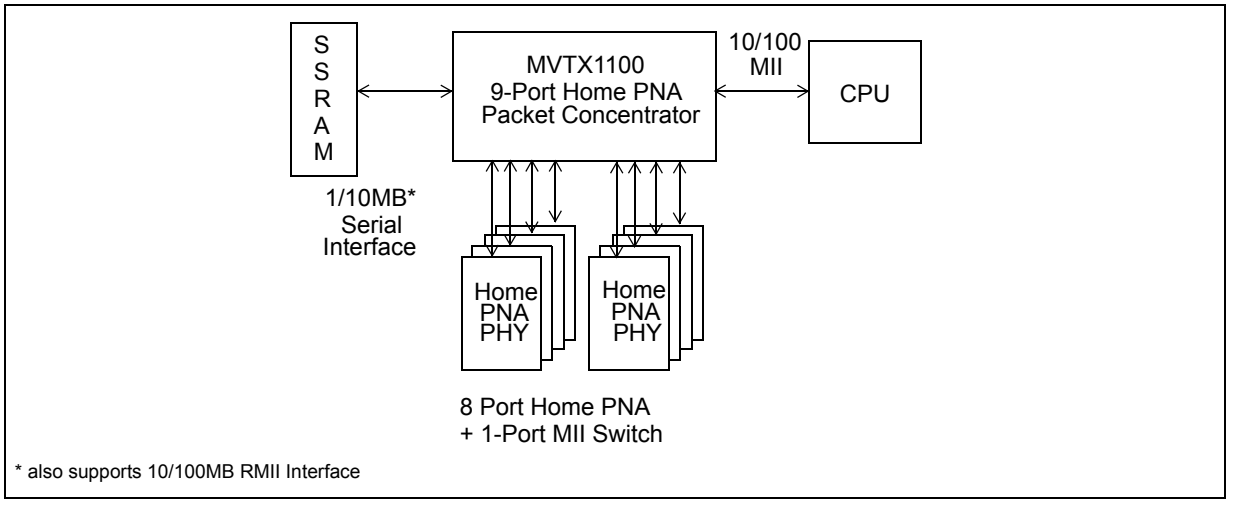


Figure 1 - System Block Diagram

Description

The MVTX1100 is a fully integrated 9-port Ethernet packet concentrator designed to support Home Networking. It is ideal for Multiple Dwelling Units (MDU) application. The MVTX1100 provides features normally not associated with plug-and-play technology without requiring an external processor to facilitate their utilization.

The MVTX1100 begins operating immediately at power-up, learning addresses automatically and forwarding packets at full wire speed to any of its 8 output ports or the uplink expansion port. At power-up, MVTX1100 configures itself from the EEPROM, and can then provide port trunking, port-based VLANs, and Quality of Service (QoS) capabilities, usually associated only with managed switches.

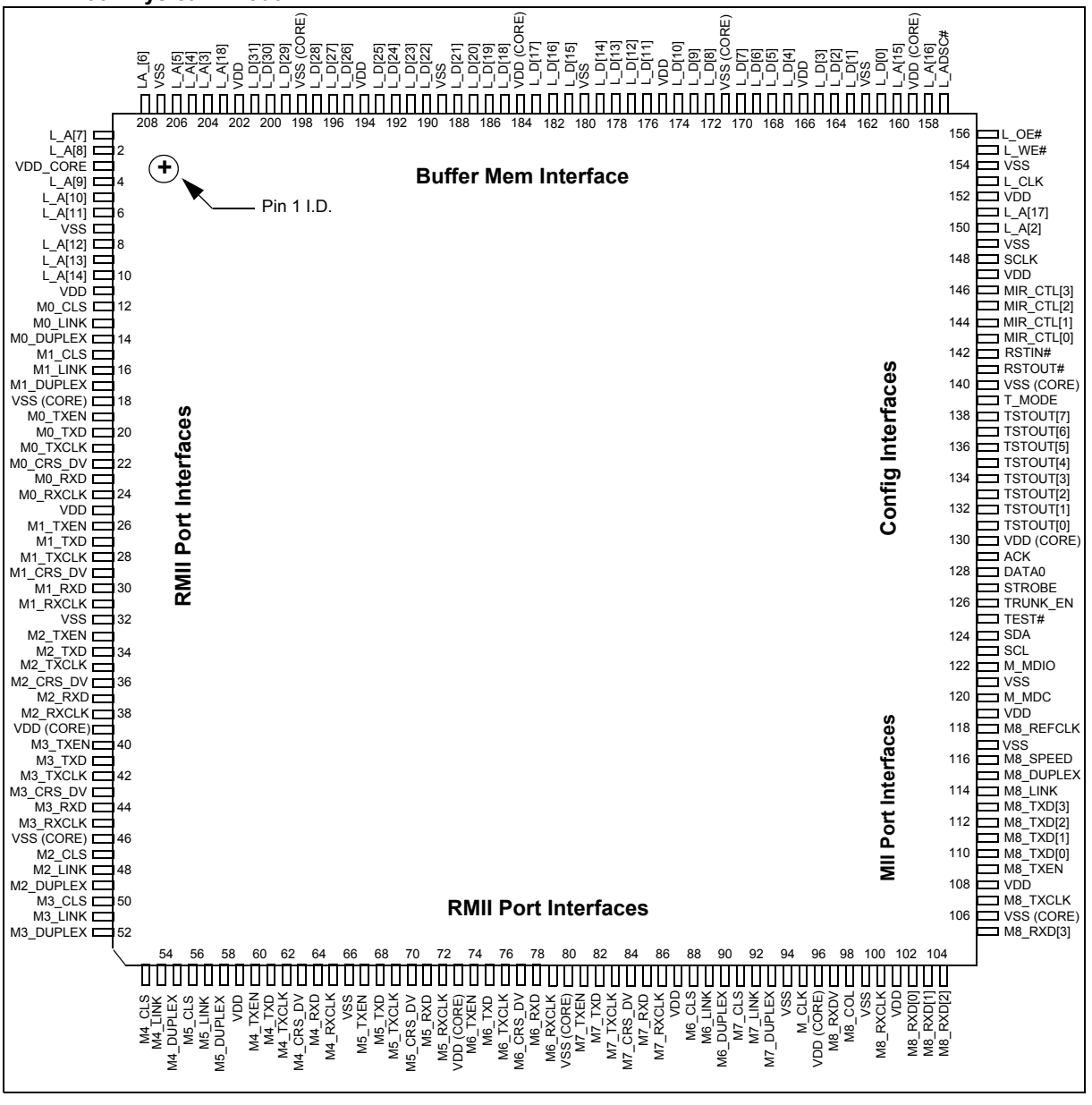
The proprietary built-in intelligence of the MVTX1100 allows it to recognize and offer packet prioritization QoS. Packets are prioritized based on their layer 2 VLAN priority tag or layer 3 Type-Of Service/ Differentiated Services (TOS/DS) field. This priority can be defined as transmit and/or drop priority.

The MVTX1100 can be used to create an 8-port unmanaged switch with one WAN router port by adding a CPU (ARM or MPC 850) connected to the additional MII port (port 8). The only external components needed for a low cost MDU system are the Home PNA physical layer transceivers and a single SBRAM per MVTX1100.

Operating at 50 MHz internally, and with a 50 MHz interface to the external SBRAM, the MVTX1100 sustains full wire-speed switching on all 9 ports. When the system supports 8 ports of 1 M Home PNA PHY with the 10M Serial uplink, the system clock can be operated to 20 MHz and still achieve full wire-speed switching on all nine ports.

The chip is packaged in a small 208 pin Plastic Quad Flat-Pak (PQFP) package.

MVTX1100 Physical Pinout



Pin Reference Table

Pin #	Pin Name
1	L_A[7]
2	L_A[8]
3	VDD (CORE)
4	L_A[9]
5	L_A[10]
6	L_A[11]
7	VSS
8	L_A[12]
9	L_A[13]
10	L_A[14]
11	VDD
12	M0_CLS
13	M0_LINK
14	M0_DUPLEX
15	M1_CLS
16	M1_LINK
17	M1_DUPLEX
18	VSS (CORE)
19	M0_TXEN
20	M0_TXD/(M0_TXD[0])[1]
21	M0_TXCLK/(M0_TXD[1])
22	M0_CRS_DV
23	M0_RXD/(M0_RXD[0])
24	M0_RXCLK/(M0_RXD[1])
25	VDD
26	M1_TXEN
27	M1_TXD/(M1_TXD[0])
28	M1_TXCLK/(M1_TXD[1])
29	M1_CRS_DV
30	M1_RXD/(M1_RXD[0])
31	M1_RXCLK/(M1_RXD[1])
32	VSS
33	M2_TXEN
34	M2_TXD/(M2_TXD[0])
35	M2_TXCLK/M2_TXD[1])
36	M2_CRS_DV
37	M2_RXD/(M2_RXD[0])
38	M2_RXCLK/ (M2_RXD[1])
39	VDD (CORE)
40	M3_TXEN
41	M3_TXD/(M3_TXD[0])
42	M3_TXCLK/(M3_TXD[1])
43	M3_CRS_DV
44	M3_RXD/(M3_RXD[0])
45	M3_RXCLK/(M3_RXD[1])
46	VSS (CORE)
47	M2_CLS
48	M2_LINK
49	M2_DUPLEX
50	M3_CLS
51	M3_LINK
52	M3_DUPLEX
53	M4_CLS
54	M4_LINK
55	M4_DUPLEX
56	M5_CLS
57	M5_LINK
58	M5_DUPLEX
59	VDD
60	M4_TXEN
61	M4_TXD/(M4_TXD[0])
62	M4_TXCLK/(M4_TXD[1])
63	M4_CRS_DV
64	M4_RXD/(M4_RXD[0])
65	M4_RXCLK/(M4_RXD[1])
66	VSS
67	M5_TXEN
68	M5_TXD/(M5_TXD[0])
69	M5_TXCLK/M5_TXD[1])
70	M5_CRS_DV
71	M5_RXD/(M5_RXD[0])
72	M5_RXCLK/ (M5_RXD[1])
73	VDD (CORE)
74	M6_TXEN
75	M6_TXD/(M6_TXD[0])
76	M6_TXCLK/ (M6_TXD[1])
77	M6_CRS_DV
78	M6_RXD/(M6_RXD[0])
79	M6_RXCLK/ (M6_RXD1])
80	VSS (CORE)
81	M7_TXEN
82	M7_TXD/(M7_TXD[0])
83	M7_TXCLK/(M7_TXD[1])
84	M7_CRS_DV
85	M7_RXD/(M7_RXD[0])
86	M7_RXCLK/(M7_RXD[1])
87	VDD
88	M6_CLS
89	M6_LINK
90	M6_DUPLEX
91	M7_CLS
92	M7_LINK
93	M7_DUPLEX
94	VSS
95	M_CLK
96	VDD (CORE)
97	M8_RXDV/S8_CRS_DV
98	M8_COL/S8_COL
99	VSS
100	M8_RXCLK/S8_RXCLK
101	VDD
102	M8_RXD[0]/S8_RXD
103	M8_RXD[1]

104	M8_RXD[2]
105	M8_RXD[3]
106	VSS (CORE)
107	M8_TXCLK/S8_TXCLK
108	VDD
109	M8_TXEN[0]/S8_TXEN
110	M8_TXD[0]/S8_TXD
111	M8_TXD[1]
112	M8_TXD[2]
113	M8_TXD[3]
114	M8_LINK/S8_LINK
115	M8_DUPLEX/S8_DUPLEX
116	M8_SPEED
117	VSS
118	M8_REFCLK
119	VDD
120	M_MDC
121	VSS
122	M_MDIO
123	SCL
124	SDA
125	TEST#
126	TRUNK_ENABLE
127	STROBE
128	DATA0
129	ACK
130	VDD (CORE)
131	TSTOUT[0]
132	TSTOUT[1]
133	TSTOUT[2]
134	TSTOUT[3]
135	TSTOUT[4]
136	TSTOUT[5]
137	TSTOUT[6]
138	TSTOUT[7]

139	T_MODE
140	VSS (CORE)
141	RSTOUT#
142	RSTIN#
143	(MIRROR_CONTROL[0])
144	(MIRROR_CONTROL[1])
145	(MIRROR_CONTROL[2])
146	(MIRROR_CONTROL[3])
147	VDD
148	SCLK
149	VSS
150	L_A[2]
151	L_A[17]
152	VDD
153	L_CLK
154	VSS
155	L_WE#
156	L_OE#
157	L_ADSC#
158	L_A[16]
159	VDD (CORE)
160	L_A[15]
161	L_D[0]
162	VSS
163	L_D[1]
164	L_D[2]
165	L_D[3]
166	VDD
167	L_D[4]
168	L_D[5]
169	L_D[6]
170	L_D[7]
171	VSS (CORE)
172	L_D[8]
173	L_D[9]
174	L_D[10]

175	VDD
176	L_D[11]
177	L_D[12]
178	L_D[13]
179	L_D[14]
180	VSS
181	L_D[15]
182	L_D[16]
183	L_D[17]
184	VDD (CORE)
185	L_D[18]
186	L_D[19]
187	L_D[20]
188	L_D[21]
189	VSS
190	L_D[22]
191	L_D[23]
192	L_D[24]
193	L_D[25]
194	VDD
195	L_D[26]
196	L_D[27]
197	L_D[28]
198	VSS (CORE)
199	L_D[29]
200	L_D[30]
201	L_D[31]
202	VDD
203	L_A[18]
204	L_A[3]
205	L_A[4]
206	L_A[5]
207	VSS
208	L_A[6]

Note 1: Pin names inside ( ) indicate RMII pins for ports 0-7.

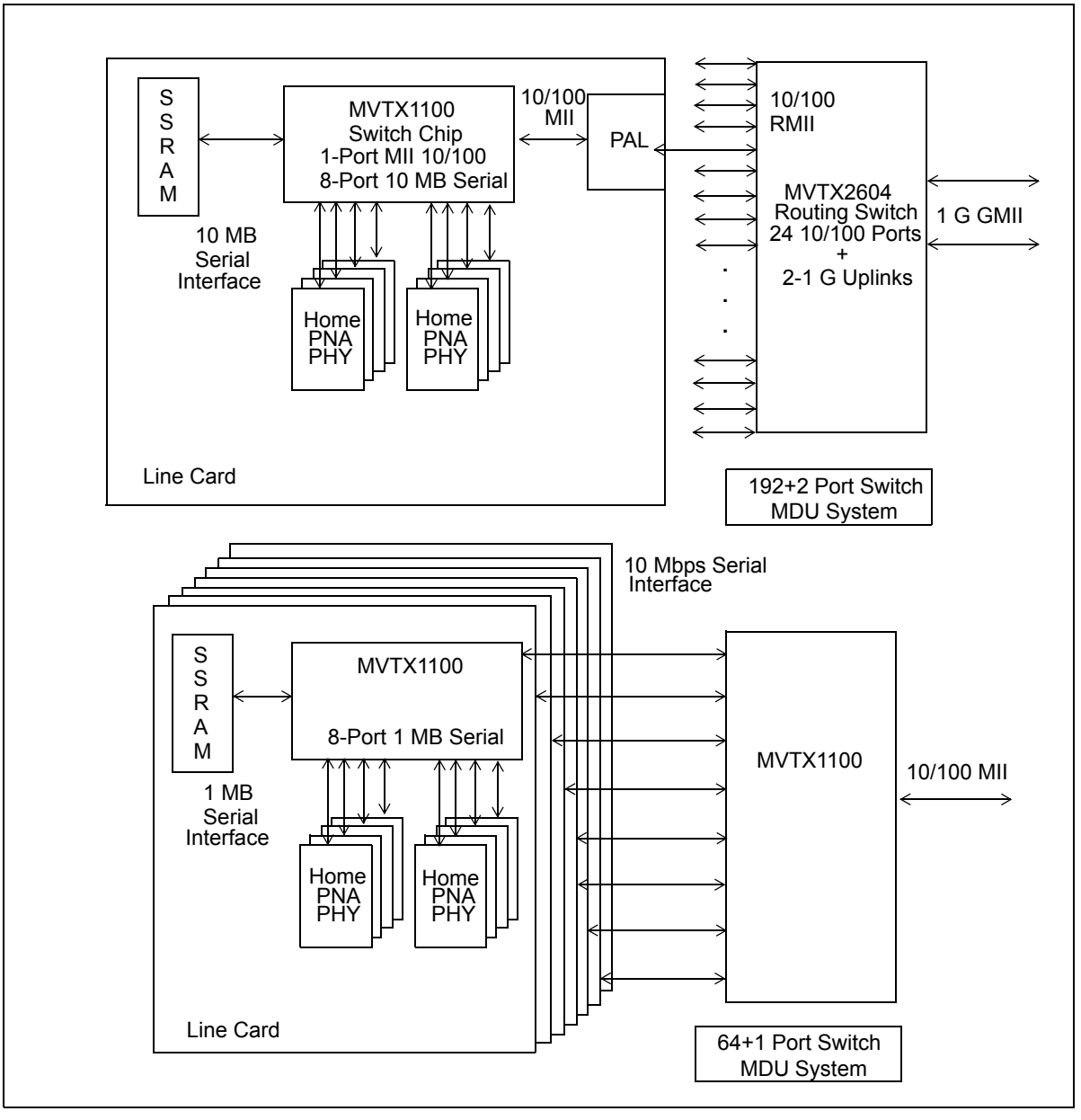


Figure 2 - System Block Diagram (High Port Density MDU System)

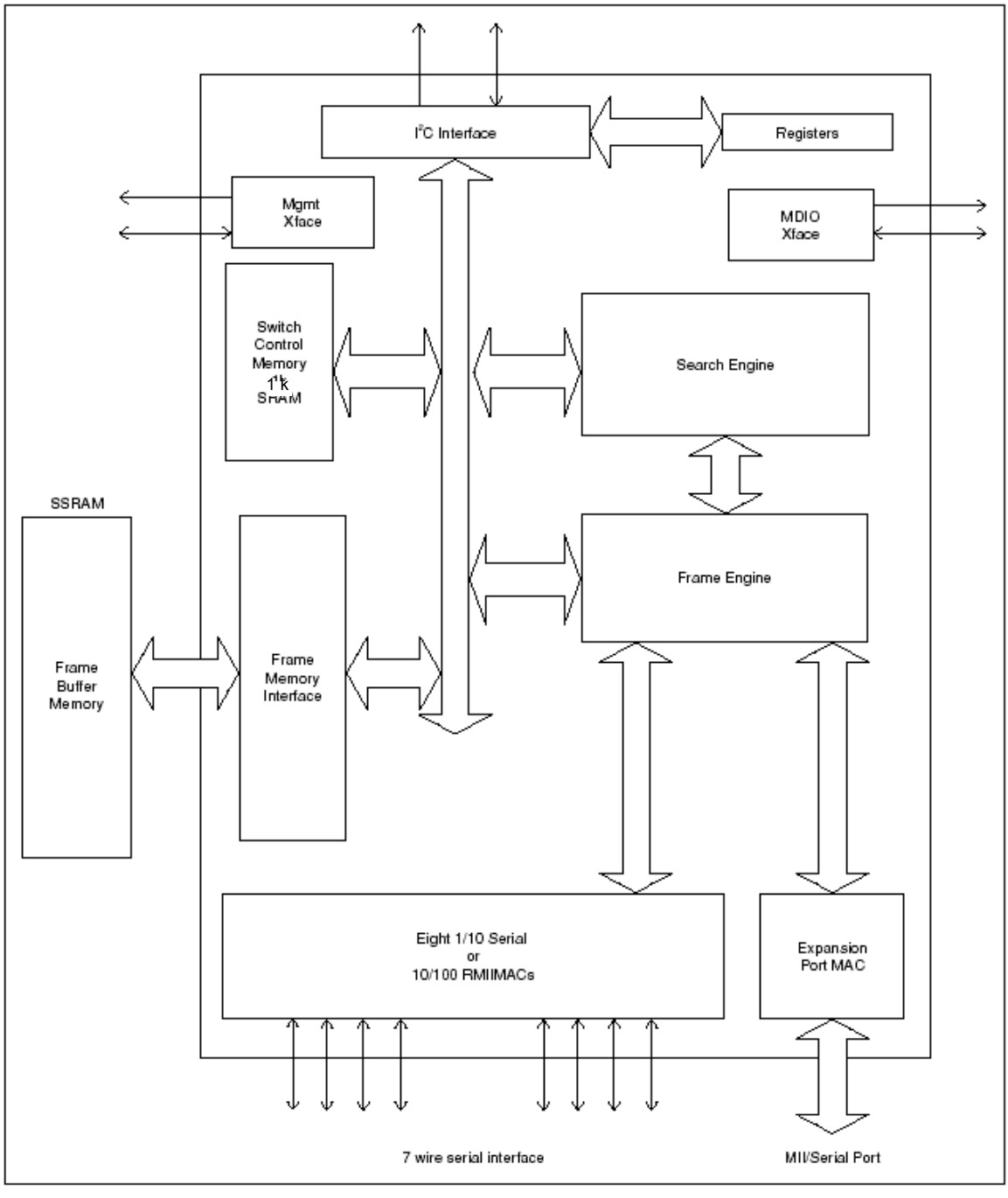


Figure 3 - MVTX1100 Block Diagram

1.0 Functional Operation

The MVTX1100 was designed to provide a cost-effective layer 2 switching solution, using technology from the Zarlink family to offer a highly integrated product for the unmanaged, DiffServ ready, Ethernet switching market.

Nine 1/10 Media Access Controllers (MAC) provide the protocol interface into the MVTX1100. These MACs perform the required packet checks to ensure that each packet provided to the Frame Engine meets all the IEEE 802.1 standards. Data packets longer than 1518 (1522 with VLAN tag) bytes and shorter than 64 bytes are dropped and MVTX1100 has been designed to support minimum inter-frame gaps between incoming packets.

The PHY addresses for the 8 RMII MACs are from 08h to 0Fh. These eight ports are denoted as ports 0 to 7. The PHY address for the uplink MAC is 10h. This port is denoted as port 8.

The Frame Engine (FE) is the primary packet buffering and forwarding engine within the MVTX1100. As such, the FE controls the storage of packets in and out of the external frame buffer memory, keeps track of frame buffer availability and schedules output packet transmissions. While packet data is being buffered, the FE extracts the necessary information from each packet header and sends it to the Search Engine for processing. Search results returned to the FE ensue the scheduling of packet transmission and prioritization. When a packet is chosen for transmission, the FE reads the packet from external buffer memory and places it in the output FIFO of the output port.

2.0 Address Learning and Aging

The MVTX1100 is able to begin address learning and packet forwarding shortly after powerup has been completed. The Search Engine examines the contents of its internal Switch Database Memory for each valid packet received on an input port.

Unknown source and destination MAC addresses are detected when the Search Engine does not find a match within its database. These unknown source MAC addresses are learned by creating a new entry in the switch database memory, and storing the necessary resulting information in that location. Subsequent searches to a learned destination MAC address will return the new contents of that MAC Control Table (MCT) entry.

After each source address search the MCT entry aging flag is updated. MCT entries that have not been accessed during a user configurable time period (2 to 67,108 seconds) will be removed. This aging time period can be configured using the 16-bit value stored in the registers MAC Address Aging Time Low and High (MATL[7:0], MATH[7:0]). The aging period is defined by the following equation:

{MATH[7:0]&MATL[7:0]} x 1024ms = Tage

The aging of all MCT entries is checked once during each time period. If the MCT entry has not been utilized before the end of the next time period, it will be deleted.

Note that when the system clock operates at 20 MHz, the aging period will be increased, compared with 50 MHz of system clock. One should adjust the MATH and MATHL content variable accordingly.

3.0 Quality of Service

The MVTX1100 utilizes Zarlink's architecture that provides a new level of (QoS) capability to unmanaged switch applications. Similar in operation to the QoS capabilities of other Zarlink chipset members, MVTX1100 provides two transmit queues per output port.

The Frame Engine manages the output transmission queues for all the MVTX1100 ports. Once the destination address search is complete, and the switch decision is passed back to the FE, the packet is inserted into the appropriate output queue. The packet entry into the high or low priority queue is controlled by either the VLAN tag information or the Type of Service/Differentiated Service (TOS/DS) field in the IP header. Either of these priority fields can be used to select the transmission priority, and the mapping of the priority field values into either the high or low priority queue can be configured using the MVTX1100 configuration registers.

If the system uses the TOS/DS field to prioritize packets, there are two choices regarding which bits of the TOS/DS field are used. Bits [0:2] of the TOS byte (known as the IP precedence field) or bits [3:5] of the TOS byte (known as the DRT field) can be used to map the transmission queue priority. Either bits, [0:2] or [3:5], can also be used as a packet drop precedence, by using bits 6 and 7 of the FCB Buffer Low Threshold register (FCBST).

MVTX1100 utilizes Weighted Round Robin (WRR) and Weighted Random Early Detection/Drop (WRED) to schedule packets for transmission. To enable MVTX1100's QoS capabilities requires the use of an external EEPROM to change the default register configurations and turn on QoS.

Weighted Round Robin is an efficient method to ensure that each of the transmission queues gets at least a minimum service level. With two output transmission queues, MVTX1100 will transmit "X" packets from the high priority queue before transmitting "Y" packets from the low priority queue. MVTX1100 allows the designer to set the high priority weight to a value between 0 and 16. The low priority weight is fixed at the value 1. If the high priority weight is set to the value 4, then it will transmit 4 high priority packets before transmitting each low priority packet.

MVTX1100 also uses a proprietary mechanism to ensure the timely delivery of high priority packets. When the latency of high priority packets reaches a threshold, it will override the WRR weights and transmit only high priority packets until the high priority packet delays are below the threshold. This threshold limit is set at less than 1 ms (last bit in and first bit out).

The QoS capabilities of the MVTX1100 are enabled by loading the appropriate values into the configuration registers. QoS for packet transmission is enabled by performing the following four steps:

1. Select the TOS/DS or VLAN Priority Tag field as the control for IP packet transmission. The selection is made using bit 7 of the Flooding Control (FCR[7]) register.
   - FCR[7]=0, use VLAN Priority Tag field to map the transmission priority if this Tag field exists.
   - FCR[7]=1, use TOS/DS field for IP packet transmission priority mapping.
2. Select which TOS/DS field to use as the control for packet transmission priority if the TOS/DS field was selected in step 1. The selection is made using bit 6 of the FCB Buffer Low Threshold (FCBST[6]) register.
   - FCBST[6]=0, use DTR subfield to map the transmission priority.
   - FCBST[6]=1, use IP precedence subfield[1] to map the transmission priority.
3. Set the transmission queue weight for the high priority queue in the Transmission Scheduling Control (AXSC[3:0]) register.
4. Set the priority mappings from the TOS/DS or VLAN Priority Tag field to the high or low priority output queue. The selection is made using the VLAN Priority Map (AVPM) and TOS Priority Map (TOSPML) registers.

Note that, for half duplex operation, the priority queues[2] must be enabled using bit 7 in the Transmission Scheduling Control (AXSC[7]) register to utilize the QoS function.

When QoS is enabled, MVTX1100 will utilize WRR to schedule packet transmission, and will use Weighted Random Early Detection/Drop (WRED) to drop random packets in order to handle buffer memory congestion. In this method, only certain packet flows are slowed down while the remaining see no impact from the network traffic congestion.

Weighted Random Early Detection/Drop (WRED) is a method of handling traffic congestion in the absence of flow control mechanisms. When flow control is enabled, all devices that are connected to a switch node that is exercising flow control are effectively unable to transmit, including nodes that are not directly responsible for the congestion problem. This inability to transmit during flow control periods would play havoc with voice packets, or other high priority packet flows, and therefore flow control is not recommended for networks that mix voice and data traffic.

1. IP precedence and DTR subfields are referred to as TOS/DS[0:2] and TOS/DS[3:5] in the IP TOS/DS byte.
2. In Half Duplex mode, the QoS functions are disabled by default.

WRED allows traffic to continue flowing into ports on a switch, and randomly drops packets with different probabilities based upon each packet's priority markings. As the switch congestion increases, the probability of dropping an input packet increases, and as congestion decreases, the probability of dropping an input packet decreases. In this manner, only traffic flows that have had packets dropped will be affected by the congestion. Other traffic flows will see no effect.

The following table summarizes the WRED operation of the MVTX1100. It lists the buffer thresholds at which each drop probability takes effect.

	WRED Threshold		Drop Percentage	
	Condition for High Priority Queue	**Condition for Low Priority Queue**	**Drop Percentage for High-Drop Packet**	**Drop Percentage for Low-Drop Packet**
Level 0	Total buffer space available in device is ≤LPBT		50%	0%
Level 1	24 buffers occupied	72 buffers occupied	75%	25%
Level 2		84 buffers occupied	100%	50%

Table 1 - WRED Operation of the MVTX1100

The WRED packet drop capabilities of MVTX1100 are enabled by performing the following three steps:

1. Select the TOS/DS or VLAN Tag field as the control for packet dropping. The selection is made using bit 7 of the Flooding Control (FCR[7]) register.
   - FCR[7]=0, use VLAN Priority Tag field to map the drop priority if this Tag field exists
   - FCR[7]=1, use ToS/DS field for IP packet transmission priority mappin.
2. Select which TOS/DS Tag field to use for packet dropping provided that the TOS/DS field was selected in step 1. The selection is made using bit 7 of the FCB Buffer Low Threshold (FCBST[7]) register.
   - FCBST[7]=0, use DTR subfield to map the drop priority
   - FCBST[7]=1, use IP precedence subfield to map the drop priority
3. Set the drop mappings from the TOS/DS or VLAN Tag field to the high or low drop priority output flag. The selection is made using the VLAN Drop Map (AVDM) and TOS Discard Map (TOSDML) registers.

Note that to utilize the QoS function of the MVTX1100, flow control has to be disabled.

4.0 Buffer Management

MVTX1100 stores each input packet into the external frame buffer memory while determining the destination the packet is to be forwarded to. The total number of packets that can be stored in the frame buffer memory depends upon the size of the external SBRAM that is utilized. For a 256 k byte SBRAM MVTX1100 can buffer 170 packets. For a 512 K byte SBRAM MVTX1100 can buffer 340 packets.

In order to provide good QoS characteristics, MVTX1100 must allocate the available buffer space to low and high priority unicast and multicast traffic. This can be accomplished using the external EEPROM to load the appropriate values into MVTX1100 configuration registers. To allow the designer to set the minimum number of buffers provided for low drop priority unicast traffic, use the Low Drop Priority Buffer Threshold (LPBT[7:0]) register. To set the maximum number of buffers allocated for all multicast packets, use the Multicast Buffer Control (MBCR[7:0]) register. During operation MVTX1100 will continuously monitor the amount of frame buffer memory that is available, and when the unused buffer space falls below a designer configurable threshold, MVTX1100 will begin to drop incoming packets (WRED). This threshold is set using the FCB Buffer Low Threshold (FCBST[5:0]) register.

5.0 Virtual LANs

MVTX1100 provides the designer the ability to define a single port-based Virtual LAN (VLAN) for each of the nine ports. This VLAN is individually defined for each port using the Port Control Registers (ECR1Px[6:4]). Bits [6:4] allow the designer to define a VLAN ID (value between 0-7) for each port.

When packets arrive at an input of MVTX1100, the search engine will determine the VLAN ID for that port, and then determine which of the other ports also are members of that VLAN by matching their assigned VLAN Id values. The packet will then be transmitted to each port with the same VLAN ID as the source port.

6.0 Concentration Mode

MVTX1100 supports a Concentration Mode, where each of the 0-7 port is only allowed to directly communicate with the uplink port 8. This mode ensures that data from any of ports 0-7 cannot be directly seen by any other port. This feature is used in MDU applications to provide data privacy to subscribers.

To use this mode, a CONC (concentration) bit in each ECR1 register of ports 0-8 must be enabled, i.e., ECR1 [7]=1, and ports 0-7 must each be set on a separate VLAN. Note that, in concentration mode, the VLAN of port 8 will be ignored.

A more flexible concentration mode can be set up. For this mode, ports 0–7 are partitioned into several groups, sharing the same VLAN ID. This will allow traffic within the same group to freely communicate with each other, while continuing to communicate outside the group in concentration mode.

7.0 Port Trunking

Port trunking allows the designer to configure the MVTX1100, such that ports 0 and 1 are defined as a logical port. This provides a 20Mb/s link to a switch or server using two 10Mb/s ports in parallel.

Ports 0 and 1 can be trunked by pulling the TRUNK_EN pin to the high state. In this mode, the source MAC address of all packets received from the trunk are checked against the MCT database to ensure that they have a port ID of 0 or 1. Packets that have a port ID other than 0 and 1 will effect the MVTX1100 to learn the new MAC address for this port change.

On transmission, the selected trunk port is determined by hashing the source and destination MAC addresses. This provides a one-to-one mapping between the trunk port and the MAC addresses. Subsequent packets with the same MAC addresses will always utilize the same trunk port.

MVTX1100 also provides a safe fail-over mode for port trunking. If one of the two ports goes down, via the ports link signal, MVTX1100 will switch all traffic destined to the failed port over to the remaining port in the trunk. Thus maintaining the trunk link, albeit at a lower effective bandwidth.

8.0 Port Mirroring

The port mirroring function is only supported in RMII mode. Using the 4 port mirroring control pins provides the ability to enable or disable port mirroring, select which of the remaining 7 ports is to be mirrored and whether the received or transmitted data is being mirrored. The control for this function is shown in the following table.

Mirrored Port	Mirror_Control [3]	Mirror_Control [2]	Mirror_Control [1]	Mirror_Control [0]
Port 0 RX	1	0	0	0
Port 0 TX	0	0	0	0
Port 1 RX	1	0	0	1
Port 1 TX	0	0	0	1
Port 2 RX	1	0	1	0
Port 2 TX	0	0	1	0
Port 3 RX	1	0	1	1
Port 3 TX	0	0	1	1
Port 4 RX	1	1	0	0
Port 4 TX	0	1	0	0
Port 5 RX	1	1	0	1
Port 5 TX	0	1	0	1
Port 6 RX	1	1	1	0
Port 6 TX	0	1	1	0
Disabled	X	1	1	1

Table 2 - Port Mirroring Configuration

When enabled, port mirroring will allow the user to monitor traffic going through the switch on output Port 7. If the port mirroring control pins, Mirror_Control[3:0], are left floating, MVTX1100 will operate with the port mirroring function disabled.

When port mirroring is enabled, the user must configure Port 7 to operate in the same mode as the port it is mirroring (autoneg, duplex, speed, flow control).

9.0 Power Saving Mode in MAC

The power saving mode is activated only in RMII mode. MVTX1100 was designed to be power efficient. When the internal RMII MAC sections detect that the external port is not receiving or transmitting packets, it will shut down and conserve power. When new packet data is loaded into the output transmit FIFO of a MAC in power saving mode, the MAC will return to life and begin operating immediately.

When the MAC is in power saving mode and new packet data is received on the RMII interface, the MAC will return to life and receive data normally into the receive FIFO. This wake up occurs when the MAC sees the CRS_DV signal asserted.

Using this method, the switch will turn off all MAC sections during periods when there is no network activity (at night for example), and save power. For large networks this power savings can be significant. To achieve the maximum power efficiency, the designer should use a physical layer transceiver that utilizes “Wake-On-LAN” technology.

10.0 EEPROM I²C Interface

A simple 2 wire serial interface is provided to allow the configuration of the MVTX1100 via an external EEPROM. MVTX1100 utilizes a 1 K bit EEPROM with an I²C interface.

11.0 Management Interface

MVTX1100 uses a standard parallel port interface to provide external CPU access to the internal registers. This parallel interface consists of 3 pins: DATA0, STROBE and ACK. The DATA0 pin provides the address and data content input to MVTX1100, while the ACK pin provides the corresponding output to the external CPU. The STROBE pin is provided as the clock for both serial data streams. Any of its internal registers can be modified through this parallel port interface.

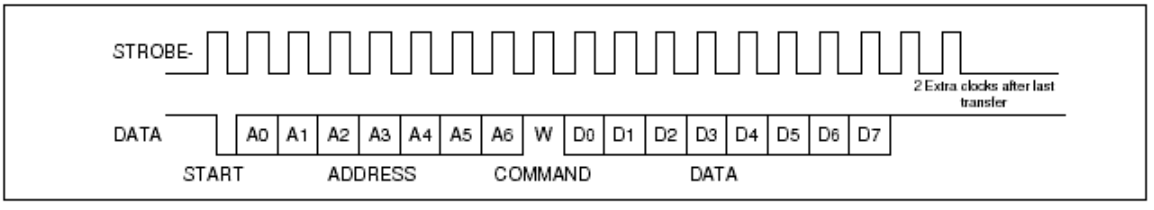


Figure 4 - Write Command

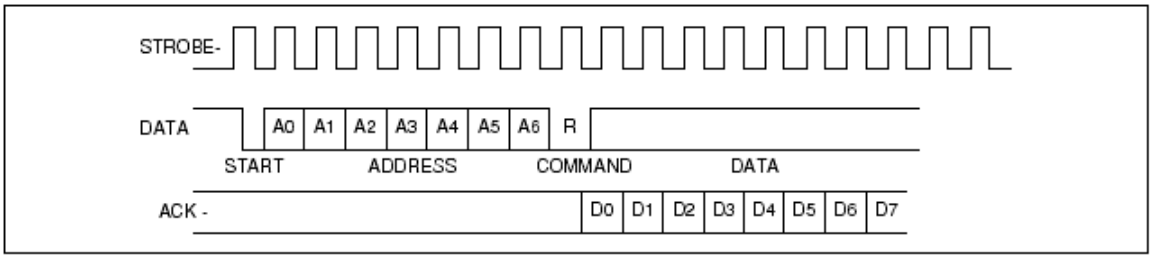


Figure 5 - Read Command

Each management interface transfer consists of four parts:

1. A START pulse – occurs when DATA is sampled high when STROBE is rising followed by DATA being sampled low when STROBE falls.
2. Register Address strobed into DATA0 pin by the high level of the STROBE pin.
3. Either a Read or Write Command (see waveforms above).
4. Data to be written provided on DATA0, or data to be read back provided on ACK.

Any command can be aborted in the middle by sending an ABORT pulse to MVTX1100. An ABORT pulse occurs when DATA is sampled low and STROBE is rising, then DATA is sampled high when STROBE falls.

12.0 Configuration Register Definitions

MVTX1100 registers can be accessed via the parallel interface and/or the I^2C interface. Some registers are only accessible through the parallel interface. The access method for each register is listed in the individual register definitions. Each register is 8-bit wide.

12.1 GCR - Global Control Register

- Access: parallel interface, Write Only
- Address: h30

Bit 0	Save configuration into EEPROM Write '1' followed by a '0'	(Default = 0)
Bit 1	Save configuration into EEPROM and reset system Write '1' (self-clearing due to reset)	(Default = 0)
Bit 2	Start Built-In Self-Test (BIST) Write '1' followed by a '0'	(Default = 0)
Bit 3	Reset system Write '1' (self-clearing due to reset)	(Default = 0)
Bit [7:4]	Reserved	

12.2 DCR - Device Status and Signature Register

- Access: parallel interface, Read Only
- Address: h31

Bit 0	Busy writing configuration from I^2C 1: Activity 0: No Activity
Bit 1	Busy reading configuration from I^2C 1: Activity 0: No Activity
Bit 2	Built-In Self-Test (BIST) in progress 1: BIST In-Progress 0: Normal Mode
Bit 3	RAM error during BIST 1: RAM Error 0: No Error
Bit [5:4]	Reserved
Bit [7:6]	Revision number 00: Initial Silicon 01: Second Silicon

12.3 DA – DA Register

- Access: parallel interface, Read Only
- Address: h36

Always returns 8-bit value hDA. Indicates the (Default DA) parallel port connection is good.

12.4 MBCR – Multicast Buffer Control Register (Address H00)

- Access: parallel interface and I^2C, Read/Write
- Address: h00

Bit [7:0]	MAX_CNT_LMT	Maximum number of multicast frames allowed	(Default = 80)

12.5 FCBST – FCB Buffer Low Threshold

- Access: parallel interface and I^2C, Read/Write
- Address: h01

Bits [5:0]	BUF_LOW_TH	Buffer Low Threshold – number of FCB left before triggering WRED	(Default = 3F)
Bit 6		Use IP precedence field (TOS[0:2]) for Priority	(Default = 0)
Bit 7		Use IP precedence subfield (TOS[0:2]) for Drop	(Default = 0)
	Note that, for Bits 6 and 7, Default = 0 means to use DTR filed (TOS[3:5]).		

12.6 LPBT – Low Drop Priority Buffer Threshold

- Access: parallel interface and I^2C, Read/Write
- Address: h02

Bit [7:0]	LOW_PRI_CNT	Number of frame buffers reserved for low-dropping traffic	(Default 3F)

12.7 FCR – Flooding Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h03

Bits [3:0]	U2MR	Unicast to Multicast Rate	(Default = 8)
Bits [6:4]	TimeBase	000 = 100 μs 001 = 200 μs 010 = 400 μs 011 = 800 μs 100 = 1.6 ms 101 = 3.2 ms 110 = 6.4 ms 111 = 100 μs	(Default = 000)
Bit 7	USE_TOS	Pick TOS over VLAN priority for IP Packet.	(Default = 0)

12.8 AVTCL – VLAN Type Code Register Loq

- Access: parallel interface and I^2C, Read/Write
- Address: h04

Bit [7:0]	VLANType_LOW	Lower 8 bits of VLAN type code.	(Default 00)

12.9 AVTCH – VLAN Type Code Register High

- Access: parallel interface and I^2C, Read/Write
- Address: h05

Bit [7:0]	VLANType_HIGH	Upper 8 bits of the VLAN type code	(Default 81)

12.10 AVPM – VLAN Priority Map

- Access: parallel interface and I^2C, Read/Write
- Address: h06

Map VLAN tag into 2 transmit queues (0 = low priority, 1 = high priority)

Bit 0	Mapped priority of tag value 0	(Default 0)
Bit 1	Mapped priority of tag value 1	(Default 0)
Bit 2	Mapped priority of tag value 2	(Default 0)
Bit 3	Mapped priority of tag value 3	(Default 0)
Bit 4	Mapped priority of tag value 4	(Default 0)
Bit 5	Mapped priority of tag value 5	(Default 0)
Bit 6	Mapped priority of tag value 6	(Default 0)
Bit 7	Mapped priority of tag value 7	(Default 0)

12.11 AVDM – VLAN Discard Map

- Access: parallel interface and I^2C, Read/Write
- Address: h07

Map VLAN tag into frame discard when low priority buffer usage is above threshold

Bit 0	Frame discard for tag value 0	(Default 0)
Bit 1	Frame discard for tag value 1	(Default 0)
Bit 2	Frame discard for tag value 2	(Default 0)
Bit 3	Frame discard for tag value 3	(Default 0)
Bit 4	Frame discard for tag value 4	(Default 0)
Bit 5	Frame discard for tag value 5	(Default 0)
Bit 6	Frame discard for tag value 6	(Default 0)
Bit 7	Frame discard for tag value 7	(Default 0)

12.12 TOSPML – TOS/DS Priority Map Low

- Access: parallel interface and I2 C, Read/Write
- Address: h08

Map TOS field in IP packet into 2 transmit queues (0 = low priority, 1 = high priority).

Bit 0	Mapped priority when TOS is 0	(Default 0)
Bit 1	Mapped priority when TOS is 1[1]	(Default 0)
Bit 2	Mapped priority when TOS is 2	(Default 0)
Bit 3	Mapped priority when TOS is 3	(Default 0)
Bit 4	Mapped priority when TOS is 4	(Default 0)
Bit 5	Mapped priority when TOS is 5	(Default 0)
Bit 6	Mapped priority when TOS is 6	(Default 0)
Bit 7	Mapped priority when TOS is 7	(Default 0)

1. TOS = 1 means the appropriate 3-bit TOS subfield is “001.

12.13 TOSDML – TOS/DS Discard Map

- Access: parallel interface and I^2C, Read/Write
- Address: h0A

Map TOS into frame discard when low priority buffer usage is above threshold

Bit 0	Frame discard when TOS is 0	(Default 0)
Bit 1	Frame discard when TOS is 1	(Default 0)
Bit 2	Frame discard when TOS is 2	(Default 0)
Bit 3	Frame discard when TOS is 3	(Default 0)
Bit 4	Frame discard when TOS is 4	(Default 0)
Bit 5	Frame discard when TOS is 5	(Default 0)
Bit 6	Frame discard when TOS is 6	(Default 0)
Bit 7	Frame discard when TOS is 7	(Default 0)

12.14 AXSC – Transmission Scheduling Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h0B

Bits [3:0]:	Transmission Queue Service Weight for high priority queue	(Default F)
Bit [4]	Reserved	
Bit [5]	Reserved	
Bit [6]:	Global Flow Control	(Default 0, enable)
Bit [7]:	Half Duplex Priority Enable	(Default 0)

12.15 MII_OP0 – MII Register Option 0

- Access by parallel interface and I^2C, Read/Write
- Address: h0C

To provide a non-standard address for the Phy Status Register. When low and high Address bytes are 0, MVTX1100 will use the standard address. Bit [7:0] Low order address byte (Default 00)

12.16 MII_OP1 – MII Register Option 1

- Access: parallel interface and I^2C, Read/Write
- Address: h0D

Bit [7:0]	High order address byte	(Default 00)

12.17 AGETIME_LOW – Mac Address Aging Timer Low

Access: parallel interface and I^2C, Read/Write

Address: h0E

Bit [7:0]	Low byte of the MAC address aging timer.	(Default 25)

12.18 AGETIME_HIGH – Mac Address Aging Timer High

- Access: parallel interface and I^2C, Read/Write
- Address: h0F

Bit [7:0]	High byte of the MAC address aging timer. The aging time is based on the following formula: {AGETIME_HIGH, AGETIME_LOW} x 1024 ms.	(Default 01)

12.19 ECR1P0 – Port 0 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h10

Bits [3:0]		RMII Port Mode Only for RMII mode, Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Auto and advertise based on Bits [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	

12.20 ECR1P1 – Port 1 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h11

Bits [3:0]	RMII Port Mode	Only for RMII mode, Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Auto and advertise based on Bits [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.21 ECR1P2 – Port 2 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h12

Bits [3:0]	RMII Port Mode	Only for RMII mode,(Default 0000) Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Auto and advertise based on Bits [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.22 ECR1P3 – Port 3 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h13

Bits [3:0]	RMII Port Mode	Only for RMII mode, Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bits [2:0] 0 – Auto and advertise based on Bits [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.23 ECR1P4 – Port 4 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h14

Bits [3:0]	RMII Port Mode	Only for RMII mode, (Default 0000) Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bit [2:0] 0 – Auto and advertise based on Bit [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	Reserved	Enable Concentration Mode	(Default 0)

12.24 ECR1P5 – Port 5 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h15

Bits [3:0]	RMII Port Mode	Only for RMII mode, Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bit [2:0] 0 – Auto and advertise based on Bits [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.25 ECR1P6 – Port 6 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h16

Bits [3:0]	RMII Port Mode	Only for RMII mode, Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bit [2:0] 0 – Auto and advertise based on Bit [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.26 ECR1P7 – Port 7 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h17

Bits [3:0]	RMII Port Mode	Only for RMII mode, Serial Mode DON'T CARE	(Default 0000)
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [3]		1 – Force configuration based on Bit [2:0] 0 – Auto and advertise based on Bit [2:0]	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.27 ECR1P8 – Port 8 Control Register

- Access: parallel interface and I^2C, Read/Write
- Address: h18

Bits [3:0]	Port Mode		(Default 0000)
Bit [3]		1 – Force configuration based on Bit [2:0] 0 – Autonegotiate and advertise based on Bit[2:0]	
Bit [2]		1 – 10 Mbps 0 – 100 Mbps	
Bit [1]		1 – Half Duplex 0 – Full Duplex	
Bit [0]		1 – Flow Control Off 0 – Flow Control On	
Bits [6:4]	PVID	Port-based VLAN ID	(Default 000)
Bit [7]	CONC:	Enable Concentration Mode	(Default 0)

12.28 FC_0 – Flow Control Byte 0

- Access: parallel interface and I^2C, Read/Write
- Address: h19

The flow control hold time parameter is the length of time a flow control message is effectual (i.e. halts incoming traffic) after being received. The hold time is measured in units of “slots,” the time it takes to transmit 64 bytes at wire speed. The default setting is 32 slots, or for a 100 Mbps port, approximately 164 s.

Bits [7:0] Flow control hold time byte 0 (Default FF)

12.29 FC_1 – Flow Control Byte 1

- Access: parallel interface and I^2C, Read/Write
- Address: h1A

Bits [7:0] Flow control hold time byte 1 (Default 00)

12.30 FC_2 – Flow Control CRC Byte 0

- Access: parallel interface and I^2C, Read/Write
- Address: h1B

Bits [7:0] Flow control frame CRC byte 0 (Default 96)

12.31 FC_3 – Flow Control CRC Byte 1

- Access: parallel interface and I^2C, Read/Write
- Address: h1C

Bits [7:0] Flow control frame CRC byte 1 (Default 8E)

12.32 FC_4 – Flow Control CRC Byte 2

- Access: parallel interface and I^2C, Read/Write
- Address: h1D

Bits [7:0] Flow control frame CRC byte 2 (Default 99)

12.33 FC_5 – Flow Control CRC Byte 3

- Access: parallel interface and I^2C, Read/Write
- Address: h1E

Bits [7:0] Flow control frame CRC byte 3 (Default 9A)

12.34 CHECKSUM - EEPROM Checksum

- • Access: parallel interface and I^2C, Read/Write
- • Address: h24

The calculation is [0x100 - ((sum of registers 0x00~0x23) & 0xFF)]. For example, based on the default register settings, the CHECKSUM value would be 0xEE.

Bits [7:0] Checksum (Default 00)

13.0 MVTX1100 Pin Descriptions

Note:

- # Active low signal
- I Input signal
- S Input signal with Schmitt-Trigger
- O Output signal
- OD Open-Drain driver
- I/O Input & Output signal
- SL Slew Rate Controlled
- D Pulldown
- U Pullup
- 5 5V Tolerance

Pin No(s).	Symbol	Type	Name & Functions
Frame Buffer Memory Interface			
201, 200, 199, 197, 196, 195, 193, 192, 191, 190, 188, 187, 186, 185, 183, 182, 181, 179, 178, 177, 176, 174, 173, 172, 170, 169, 168, 167, 165, 164, 163, 161	L_D[31:0]	I/O, U, SL	Databus to Frame Buffer Memory
203, 151, 158, 160, 10, 9, 8, 6, 5, 4, 2, 1, 208, 206, 205, 204, 150	L_A[18:2]	I/O, U, SL	Address Pins for Buffer Memory
153	L_CLK	O	Frame Buffer Memory Clock
155	L_WE#	O, SL	Frame Buffer Memory Write Enable
156	L_OE#	O	Frame Buffer Memory Output Enable
157	L_ADSC#	O, SL	Address Status Control
MII Management Interface			
120	M_MDC	O	MII Management Data Clock
122	M_MDIO	I/O, U	MII Management Data I/O
I^2C Interface (Serial EEPROM Interface)			
123	SCL	O, U, 5	I^2C Data Clock
124	SDA	I/O, U, OD, 5	I^2C Data I/O
Parallel Port Management Interface			
127	STROBE	I, U, S, 5	Strobe Pin
128	DATA0	I, U, 5	Data Pin
129	ACK	O, U, OD, 5	Acknowledge Pin
Port 0 Serial Interface			
23	M0_RXD	I, U	Port 0 Receive Data

Pin No(s).	Symbol	Type	Name & Functions
24	M0_RXCLK	I, U	Port 0 Receive Clock
22	M0_CRS_DV	I, D	Port 0 Carrier Sense and Data Valid
20	M0_TXD	O	Port 0 Transmit Data
21	M0_TXCLK	I	Port 0 Transmit Clock
19	M0_TXEN	O	Port 0 Transmit Enable
12	M0_CLS	I, U	Port 0 Collision Detection
13	M0_LINK	I, U	Port 0 Link Status
14	M0_DUPLEX	I, U	Port 0 Full Duplex Select (half-duplex = 0)
Port 1 Serial Interface			
30	M1_RXD	I, U	Port 1 Receive Data
31	M1_RXCLK	I, U	Port 1 Receive Clock
29	M1_CRS_DV	I, D	Port 1 Carrier Sense and Data Valid
27	M1_TXD	O	Port 1 Transmit Data
28	M1_TXCLK	I	Port 1 Transmit Clock
26	M1_TXEN	O	Port 1 Transmit Enable
15	M1_CLS	I, U	Port 1 Collision Detection
16	M1_LINK	I, U	Port 1 Link Status
17	M1_DUPLEX	I, U	Port 1 Full-Duplex Select (half-duplex = 0)
Port 2 Serial Interface			
37	M2_RXD	I, U	Port 2 Receive Data
38	M2_RXCLK	I, U	Port 2 Receive Clock
36	M2_CRS_DV	I, D	Port 2 Carrier Sense and Data Valid
34	M2_TXD	O	Port 2 Transmit Data
35	M2_TXCLK	I	Port 2 Transmit Clock
33	M2_TXEN	O	Port 2 Transmit Enable
47	M2_CLS	I, U	Port 2 Collision Detection
48	M2_LINK	I, U	Port 2 Link Status
49	M2_DUPLEX	I, U‘	Port 2 Full-Duplex Select (half-duplex = 0)
Port 3 Serial Interface			
44	M3_RXD	I, U	Port 3 Receive Data

Pin No(s).	Symbol	Type	Name & Functions
45	M3_RXCLK	I, U	Port 3 Receive Clock
43	M3_CRS_DV	I, D	Port 3 Carrier Sense and Data Valid
41	M3_TXD	O	Port 3 Transmit Data
42	M3_TXCLK	I	Port 3 Transmit Clock
40	M3_TXEN	O	Port 3 Transmit Enable
50	M3_CLS	I, U	Port 3 Collision Detection
51	M3_LINK	I, U	Port 3 Link Status
52	M3_DUPLEX	I, u	Port 3 Full-Duplex Select (half-duplex = 0)
Port 4 Serial Interface			
64	M4_RXD	I, U	Port 4 Receive Data
65	M4_RXCLK	I, U	Port 4 Receive Clock
63	M4_CRS_DV	I, U	Port 4 Carrier Sense and Data Valid
61	M4_TXD	O	Port 4 Transmit Data
62	M4_TXCLK	I	Port 4 Transmit Clock
60	M4_TXEN	O	Port 4 Transmit Enable
53	M4_CLS	I, U	Port 4 Collision Detection
54	M4_LINK	I, U	Port 4 Link Status
55	M4_DUPLEX	I, U	Port 4 Full-Duplex Select (half-duplex = 0)
Port 5 Serial Interface			
71	M5_RXD	I, U	Port 5 Receive Data
72	M5_RXCLK	I, U	Port 5 Receive Clock
70	M5_CRS_DV	I, D	Port 5 Carrier Sense and Data Valid
68	M5_TXD	O	Port 5 Transmit Data
69	M5_TXCLK	I	Port 5 Transmit Clock
67	M5_TXEN	O	Port 5 Transmit Enable
56	M5_CLS	I, U	Port 5 Collision Detection
57	M5_LINK	I, U	Port 5 Link Status
58	M5_DUPLEX	I, U	Port 5 Full-Duplex Select (half-duplex = 0)
Port 6 Serial Interface			
78	M6_RXD	I, U	Port 6 Receive Data

Pin No(s).	Symbol	Type	Name & Functions
79	M6_RXCLK	I, U	Port 6 Receive Clock
77	M6_CRS_DV	I, D	Port 6 Carrier Sense and Data Valid
75	M6_TXD	O	Port 6 Transmit Data
76	M6_TXCLK	I	Port 6 Transmit Clock
74	M6_TXEN	O	Port 6 Transmit Enable
88	M6_CLS	I, U	Port 6 Collision Detection
89	M6_LINK	I, U	Port 6 Link Status
90	M6_DUPLEX	I, U	Port 6 Full-Duplex Select (half-duplex = 0)
Port 7 Serial Interface			
85	M7_RXD	I, U	Port 7 Receive Data
86	M7_RXCLK	I, U	Port 7 Receive Clock
84	M7_CRS_DV	I, D	Port 7 Carrier Sense and Data Valid
82	M7_TXD	O	Port 7 Transmit Data
83	M7_TXCLK	I	Port 7 Transmit Clock
81	M7_TXEN	O	Port 7 Transmit Enable
91	M7_CLS	U	Port 7 Collision Detection
92	M7_LINK	I, U	Port 7 Link Status
93	M7_DUPLEX	I, U	Port 7 Full-Duplex Select (half-duplex = 0)
Port 0 RMII Interface			
24, 23	M0_RXD[1:0]	I, U	Port 0 Receive Data
22	M0_CRS_DV	I, D	Port 0 Carrier Sense and Data Valid
21, 20	M0_TXD[1:0]	O	Port 0 Transmit Data
19	M0_TXEN	O	Port 0 Transmit Enable
Port 1 RMII Interface			
31, 30	M1_RXD[1:0]	I, U	Port 1 Receive Data
29	M1_CRS_DV	I, D	Port 1 Carrier Sense and Data Valid
28, 27	M1_TXD[1:0]	O	Port 1 Transmit Data
26	M1_TXEN	O	Port 1 Transmit Enable
Port 2 RMII Interface			
38, 27	M2_RXD[1:0]	I, U	Port 2 Receive Data

Pin No(s).	Symbol	Type	Name & Functions
36	M2_CRS_DV	I, D	Port 2 Carrier Sense and Data Valid
35, 34	M2_TXD[1:0]	O	Port 2 Transmit Data
34	M2_TXEN	O	Port 2 Transmit Enable
Port 3 RMII Interface			
45, 44	M3_RXD[1:0]	I, U	Port 3 Receive Data
43	M3_CRS_DV	I, D	Port 3 Carrier Sense and Data Valid
42, 41	M3_TXD[1:0]	O	Port 3 Transmit Data
40	M3_TXEN	O	Port 3 Transmit Enable
Port 4 RMII Interface			
65, 64	M4_RXD[1:0]	I, U	Port 4 Receive Data
63	M4_CRS_DV	I, D	Port 4 Carrier Sense and Data Valid
62, 61	M4_TXD[1:0]	O	Port 4 Transmit Data
60	M4_TXEN	O	Port 4 Transmit Enable
Port 5 RMII Interface			
72, 71	M5_RXD[1:0]	I, U	Port 5 Receive Data
70	M5_CRS_DV	I, D	Port 5 Carrier Sense and Data Valid
69, 68	M5_TXD[1:0]	O	Port 5 Transmit Data
67	M5_TXEN	O	Port 5 Transmit Enable
Port 6 RMII Interface			
79, 78	M6_RXD[1:0]	I, U	Port 6 Receive Data
77	M6_CRS_DV	I, D	Port 6 Carrier Sense and Data Valid
76, 75	M6_TXD[1:0]	O	Port 6 Transmit Data
74	M6_TXEN	O	Port 6 Transmit Enable
Port 7 RMII Interface			
86, 85	M7_RXD[1:0]	I, U	Port7 Receive Data
84	M7_CRS_DV	I, D	Port 7 Carrier Sense and Data Valid
83, 82	M7_TXD[1:0]	O	Port 7 Transmit Data
81	M7_TXEN	O	Port 7 Transmit Enable
Port 8 MII Interface			
105, 104, 103, 102	M8_RXD[3:0]	I, U	Port 8 Receive Data

Pin No(s).	Symbol	Type	Name & Functions
113, 112, 111, 110	M8_TXD[3:0]	O	Port 8 Transmit Data
109	M8_TXEN	O	Port 8 Transmit Enable
97	M8_RXDV	I, D	Port 8 Receive Data Valid
100	M8_RXCLK	I, U	Port 8 Receive Clock
107	M8_TXCLK	I/O, U	Port 8 Transmit Clock
114	M8_LINK	I, U	Port 8 Link Status
116	M8_SPEED	I/O, U	Port 8 Speed Select (100Mb = 1)
115	M8_DUPLEX	I, U	Port 8 Full-Duplex Select (half-duplex = 0)
98	M8_COL	I, U	Port 8 Collision Detect
118	M8_REFCLK	O, U	Port 8 Reference Clock M8_REFCLK=1/2 M_CLK
Port 8 Serial Interface			
102	S8_RXD	I, U	Port 8 Serial Receive Data
100	S8_RXCLK	I, U	Port 8 Serial Receive Clock
97	S8_CRS_DV	I, D	Port 8 Serial Carrier Sense and Data Valid
110	S8_TXD	O	Port 8 Serial Transmit Data
107	S8_TXCLK	I	Port 8 Serial Transmit Clock
109	S8_TXEN	O	Port 8 Serial Transmit Enable
98	S8_COL	I, U	Port 8 Serial Collision Detect
114	S8_LINK	I, U	Port 8 Link Status
115	S8_DUPLEX	I, U	Port 8 Full-Duplex Select (half-duplex = 0)
Miscellaneous Control Pins			
95	M_CLK	I	Reference Clock for Serial interface = 50 MHz±50 ppm
148	SCLK	I	System Clock (50 - 80 MHz)
126	TRUNK_EN	I, D	Port Trunking Enable
142	RESIN#	I, S	Reset Pin
141	RESETOUT#	O	PHY Reset Pin
146, 145, 144, 143	MIR_CTL[3:0]	I/O, U	Port Mirroring Control (only for RMII mode)

Pin No(s).	Symbol	Type	Name & Functions
Test Pins			
125	TEST#		Manufacturing Pin. Leave as No Connect (NC)
139	TMODE#	I/O, U	Manufacturing Pin. Puts device into test mode for ATE test. Leave as No Connect (NC)
138, 137, 136, 135	TSTOUT[7:4]	O	Test Outputs
134, 133, 132, 131	TSTOUT[3:0]	I/O, U	Test Outputs
Power Pins			
3, 39, 73, 96, 130, 159, 184	VDD (Core)	Input	+3.3 Volt DC Supply for Core Logic (7 pins)
11, 25, 59, 87, 101, 108, 119, 147, 152, 166, 175, 194, 202	VDD	Input	+3.3 Volt DC Supply for I/O Pads (13 pins)
18, 46, 80, 106, 140, 171, 198	VSS (Core)	Input	Ground for Core Logic (7 pins)
7, 32, 66, 94, 99, 117, 121, 149, 154, 162, 180, 189, 207	VSS	Input	Ground for I/O Pads (13 pins)

13.1 STRAP Options

The Strap options are relevant during the initial power-on period, when reset is asserted. During reset, MVTX1100 will examine the boot strap address pin to determine its value and modify the internal configuration of the chip accordingly.

"1" means Pull Up

"0" means Pull Down with an external 1 K Ohm

Default value is 1, (all boot strap pins have internal pull up resistor).

Pin No(s)	Symbol	Name & Functions
206 (L_A[5])	Memory Size	1 - Memory size = 256 KB, 0 - Memory size = 512 KB
208 (L_A [6])	EEPROM	1 - NO EEPROM Installed 0 - EEPROM Installed[1]
1 (L_A [7])	MII Management via MDIO	1 - Enable 0 - Disable
5, 4 (L_A [10:9])	XLINK Speed	11 - 100 Mbps 10 - 200 Mbps 01 - 300 Mbps 00 - 400 Mbps (0 - Pull down, 1 - Pull up)
160 (L_A[15])	Ports 0-7 RMII/Serial	1 - RMII Mode for ports 0-7 0 - Serial mode for ports 0-7
151 (L_A[17])	Port 8 MII/Serial	1 - MII Mode for port 8 0 - Serial mode for port 8
150 (L_A[2])	Link Polarity	Link Polarity for serial interface 1 - Active Low 0 - Active High
204 (L_A[3])	FDX Polarity	Full/Half Duplex Polarity for serial interface 1 - Active Low 0 - Active High
205 (L_A[4])	SPD100 Polarity	Speed polarity for serial interface 1 - Active Low 0 - Active High
2 (L_A[8])	Device ID	Use in cascade mode only
133 (TST[2])	SBRAM Self Test	For Board/System Manufacturing Test[2] 1 - Disable 0 - Enable

Note 1: 1. If the MVTX1100 is configured from EEPROM preset (L_A[6] pulled down at reset), it will try to load its configuration from the EEPROM. If the EEPROM is blank or not preset, it will not boot up. The parallel port can be used to program the EEPROM at any time.

Note 2: During normal power-up the MVTX1100 will run through an external SBRAM memory test to ensure that there are no memory interface problems. If a problem is detected, the chip will stop functioning. To facilitate board debug in the event that a system stops functioning, the MVTX1100 can be put into a continuous SBRAM self test mode to allow an operator to determine if there are stuck pins in the memory interface (using network analyzer).

14.0 DC Electrical Characteristics

14.1 Absolute Maximum Ratings

Storage Temperature	-65°C to +150C
Operating Temperature	-40°C to +85C
Maximum Junction Temperature	+125C
Supply Voltage VDD with Respect to Vss	+3.0 V to +3.6 V
Voltage on 5V Tolerant Input Pins	-0.5 V to (VDD + 3.3 V)
Voltage on Other Pins	-0.5 V to (VDD + 0.3 V)

Caution: Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the Absolute Maximum Ratings for extended periods may affect device reliability.

14.2 DC Electrical Characteristics

VDD = 3.0 V to 3.6 V (3.3v +/- 10%) $T_{AMBIENT}$ = -40C to +85C

14.3 Recommended Operating Conditions

Symbol	Parameter Description	Min.	Typ.	Max.	Unit
f_{OSC}	Frequency of Operation	50	66	80	MHz
I_{DD} V_{OH} V_{OL}	Supply Current - @ 55 MHz, 8x100 M, 100% Full Duplex Traffic (VDD = 3.3V)		580		mA
	Output High Voltage (CMOS)	2.4			V
	Output Low Voltage (CMOS)			0.4	V
V_{IH-TTL}	Input High Voltage (TTL 5 V tolerant)	2.0		VDD + 2.0	V
V_{IL-TTL}	Input Low Voltage (TTL 5 V tolerant)			0.8	V
I_{IL}	Input Leakage Current (0.1 V < V_{IN} < VDD) (all pins except those with internal pull-up/ pull-down resistors)			10	µA
I_{OL}	Output Leakage Current (0.1 V < V_{OUT} < VDD)			10	µA
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			5	pF
$C_{I/O}$	I/O Capacitance			7	pF
θ_{ja}	Thermal resistance with 0 air flow			29.7	C/W
θ_{ja}	Thermal resistance with 1 m/s air flow			28.8	C/W
θ_{ja}	Thermal resistance with 2 m/s air flow			26.8	C/W
θ_{jc}	Thermal resistance between junction and case			12.6	C/W

14.4 Clock Frequency Specifications

Symbol	Parameter	(Hz)	Note:
C1	SCLK - Core System Clock Input	50 M	
C2	M_CLK - RMII Port Clock	50 M	
C3	M8_REFCLK - MII Reference Clock	25 M	
C4	L_CLK - Frame Buffer Memory Clock	50 M	L_CLK = SCLK
C5	M_MDC - MII Management Data Clock	1.56 M	M_MDC = SCLK/32
C6	SCL - I^2C Data Clock	50 K	SCL = M_CLK/1000

Suggestion Clock rate for various configurations:

		Input			Output		
Configuration		SCLK	M_CLK (RMII)	M8_REF	L_CLK	M_MDC	SCL
Port 0-7	Port 8						
10 M RMII	10/100 M MII	50 M	50 M	--	=SCLK	=SCLK/32	50 K
100 M RMII	Not Used	55 M	50 M	--	=SCLK	=SCLK/32	50 K
100 M RMII	10/100 M MII	60 M	50 M	--	=SCLK	=SCLK/32	50 K
100 M RMII	200 M MII	66.66 M	50 M	50 M	=SCLK	=SCLK/32	50 K
100 M RMII	300 M MII	75 M	50 M	75 M	=SCLK	=SCLK/32	50 K
100 M RMII	400 M MII	80 M	50 M	100 M	=SCLK	=SCLK/32	50 K

15.0 AC Timing Characteristics

15.1 Frame Buffer Memory Interface:

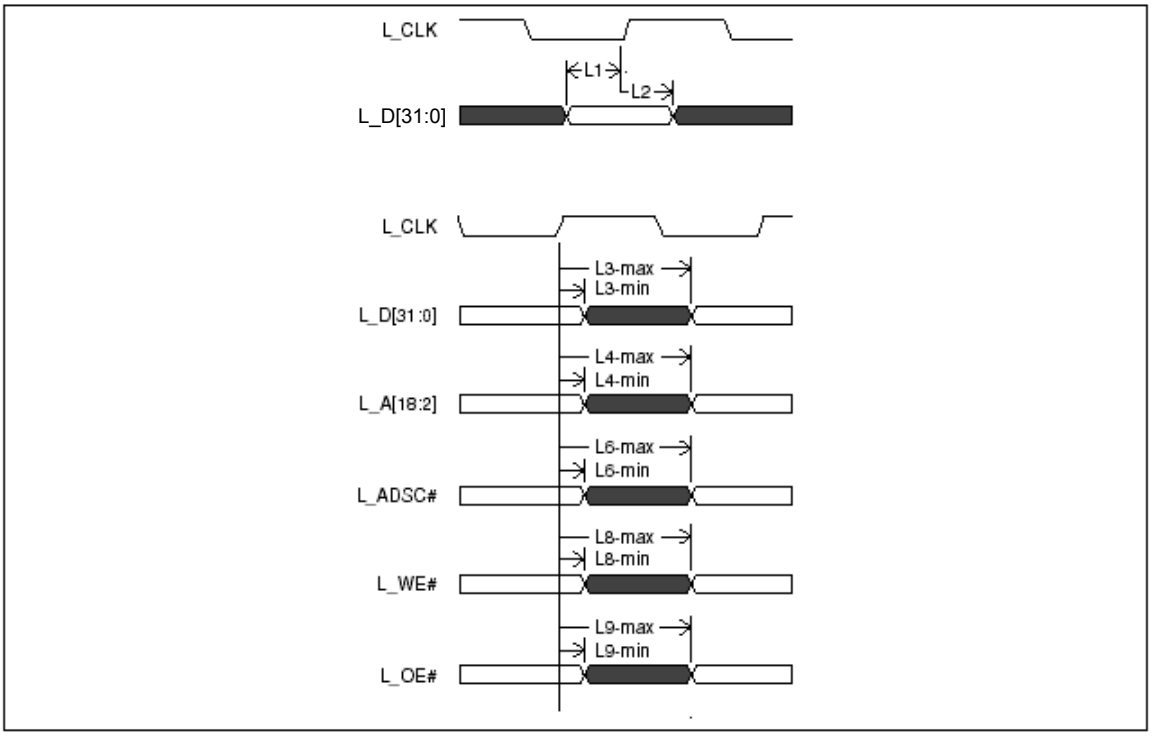


Figure 6 - Framer Buffer Memory Interface Timing

Symbol	Parameter	50 MHz		Note
		Min. (ns)	Max. (ns)	
L1	L_D[31:0] input setup time	5		
L2	L_D[31:0] input hold time	0		
L3	L_D[31:0] output valid delay	1	8	C_L = 30 pF
L4	L_A[18:2] output valid delay	1	8	C_L = 50 pF
L6	L_ADSC# output valid delay	1	8	C_L = 50 pF
L8	L_WE# output valid delay	1	8	C_L = 30 pF
L9	L_OE# output valid delay	1	8	C_L = 30 pF

Table 3 - Frame Buffer Memory Interface Timing

15.2 Serial Timing Requirements

Symbol	Parameter	50 MHz		Note:
		Min. (ns)	Max. (ns)	
M1	M_[8:0]_[TX/RX]CLK			Serial Input Clock
M2	M[8:0]_RXD input setup time	4		
M3	M[8:0]_RXD input hold time	1		
M4	M[8:0]_CRS_DV input setup time	4		
M5	M[8:0]_TXEN output delay time	1	11	C_L = 30 pF
M6	M[8:0]_TXD output delay time	1	11	C_L = 30 pF
M7	M[8:0]_LINK input setup time	4		

Table 4 - Serial Timing Requirements

15.3 RMII Timing Requirements

Symbol	Parameter	50 MHz		Note:
		Min. (ns)	Max. (ns)	
M1	M_CLK			Reference Input Clock
M2	M[7:0]_RXD[1:0] input setup time	4		
M3	M[7:0]_RXD[1:0] input hold time	1		
M4	M[7:0]_CRS_DV input setup time	4		
M5	M[7:0]_TXEN output delay time	1	11	C_L = 30 pF
M6	M[7:0]_TXD[1:0] output delay time	1	11	C_L = 30 pF
M7	M[7:0]_LINK input setup time	4		

Table 5 - RMII Timing Requirements

15.4 MII Timing Requirements

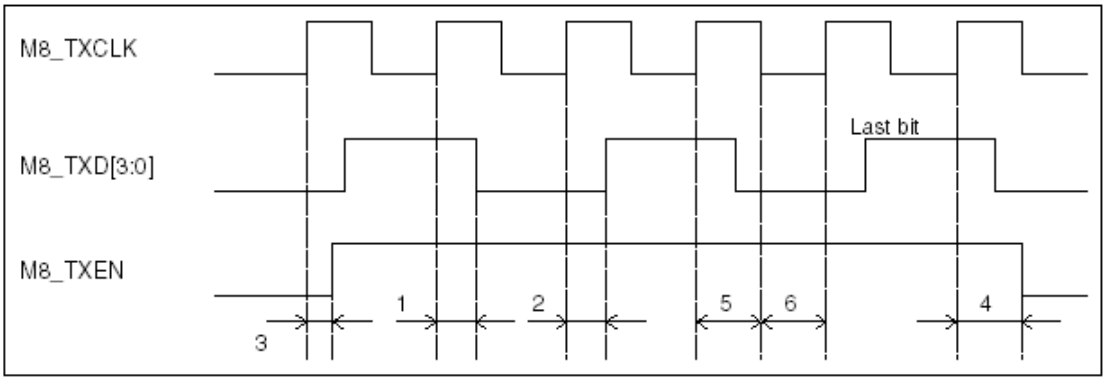


Figure 7 - Transmit Timing

Symbol	Parameter	Time		Unit
		Min.	Max.	
1	M8_TXCLK rise to M8_TXD[3:0] inactive delay	5	20	ns
2	M8_TXCLK rise to M8_TXD[3:0] active delay	5	20	ns
3	M8_TXCLK rise to M8_TXEN active delay	5	20	ns
4	M8_TXCLK rise of last M8_TXD bit to M8_TXEN inactive delay	5	20	ns
5	M8_TXCLK high wide	25	Inf.	ns
6	M8_TXCLK low wide	25	Inf.	ns
	M8_TXCLK input rise time require		5	ns
	M8_TXCLK input fall time require		5	ns

*Inf. = infinite

Table 6 - Transmit Timing Requirements

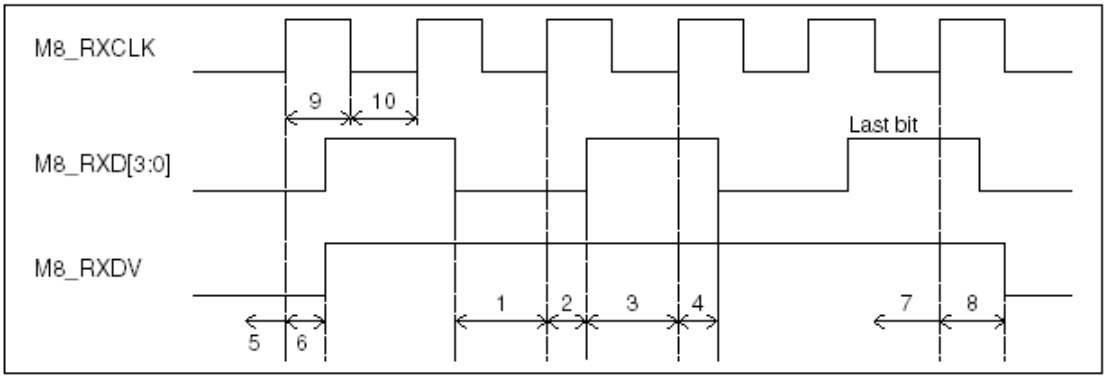
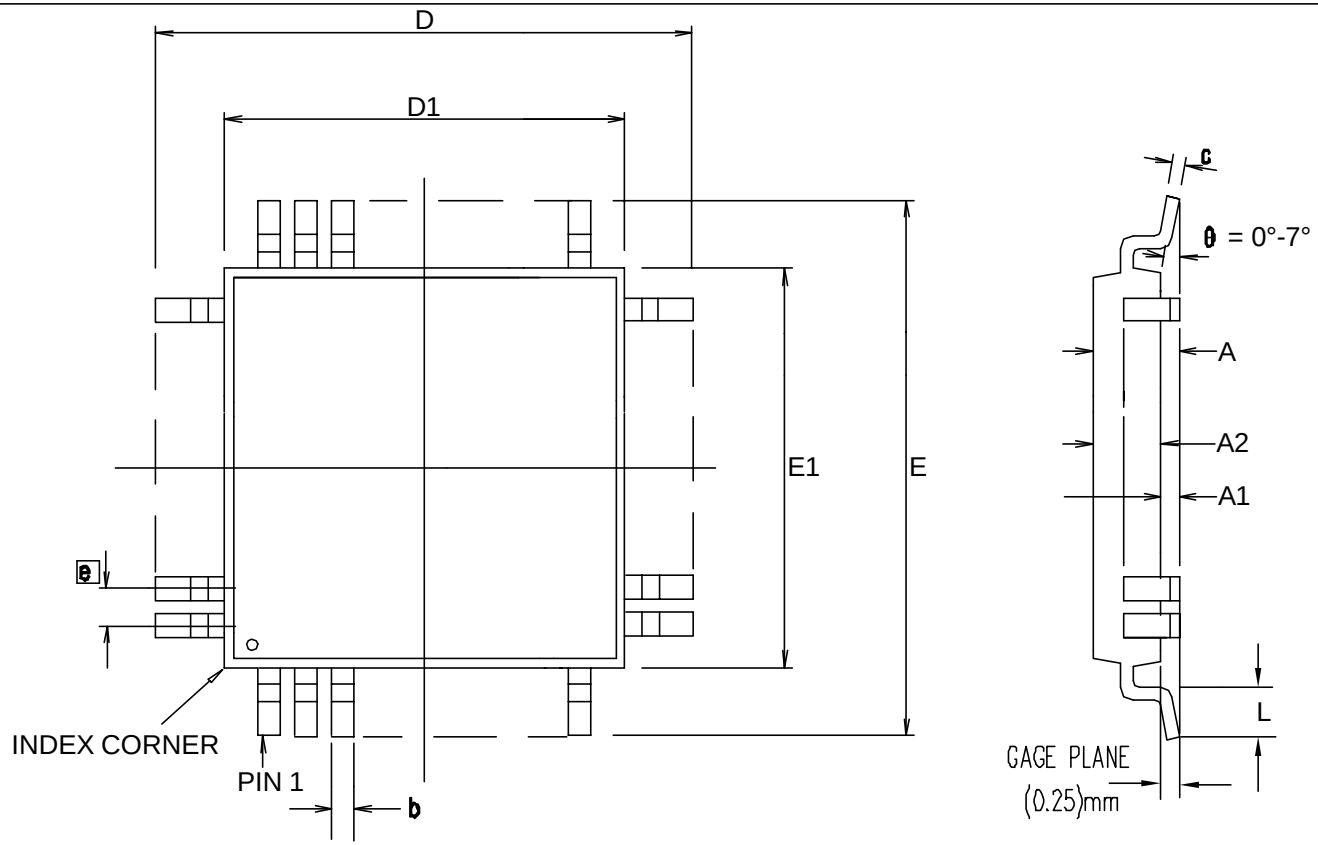


Figure 8 - Receive Timing

Symbol	Parameter	Time		Unit
		Min.	Max.	
1	M8_RXD[3:0] low input setup time	10		ns
2	M8_RXD[3:0] low input hold time		5	ns
3	M8_RXD[3:0] high input setup time	10		ns
4	M8_RXD[3:0] high input hold time		5	ns
5	M8_RXDV low input setup time	10		ns
6	M8_RXDV low input hold time		5	ns
7	M8_RXDV high input setup time	10		ns
8	M8_RXDV high input hold time		5	ns
9	M8_RXCLK high wide	25	Inf.	ns
10	M8_RXCLK low wide	25	Inf.	ns
	M8_RXCLK input rise time require		5	ns
	M8_RXCLK input fall time require		5	ns

Table 7 - Receive Timing Requirements



Symbol	Control Dimensions in millimetres		
	MIN	Nominal	MAX
A	–	–	4.10
A1	0.25	–	–
A2	3.20	3.32	3.60
D	30.60 BSC		
D1	28.00 BSC		
E	30.60 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
e	0.50 BSC		
b	0.17	0.20	0.27
c	0.09	0.15	0.20
θ	0°	–	7°
ccc	–	0.08	–
N	208		
ND	52		
NE	52		

Conforms to JEDEC MO-143

Notes:

1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.

ISSUE	1			
ACN	213984			
DATE	3Feb03			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes: GP / L

Package Code QB

Package Outline for 208 Lead MQFP (28x28x3.32mm) + 2.6 mm (footprint)

GPD00828

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