MX23L1610

3.3 Volt 16-Mbit (2M x 8 / 1M x 16) Mask ROM

FEATURES

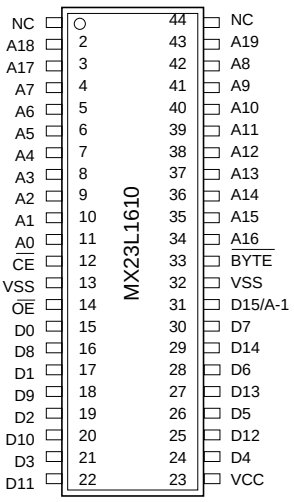
- Bit organization
  - 2M x 8 (byte mode)
  - 1M x 16 (word mode)
- Fast access time
  - 70ns (max.)@3.3V±10%
- Current
  - Operating:25mA
  - Standby:15uA
- Supply voltage
  - 3.0V ~ 3.6V
- Package
  - 44 pin SOP (500mil)
  - 42 pin DIP (600mil)
  - 48 pin TSOP (12mm x 20mm)
  - 44 pin TSOP (Type II)

PIN DESCRIPTION

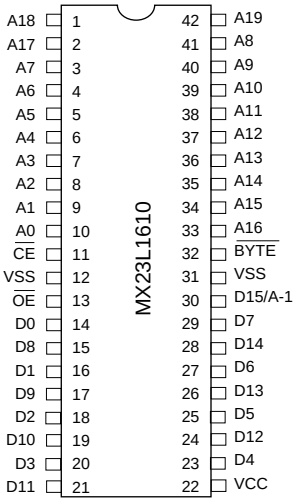
Symbol	Pin Function
A0~A19	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{Byte}$	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

PIN CONFIGURATION

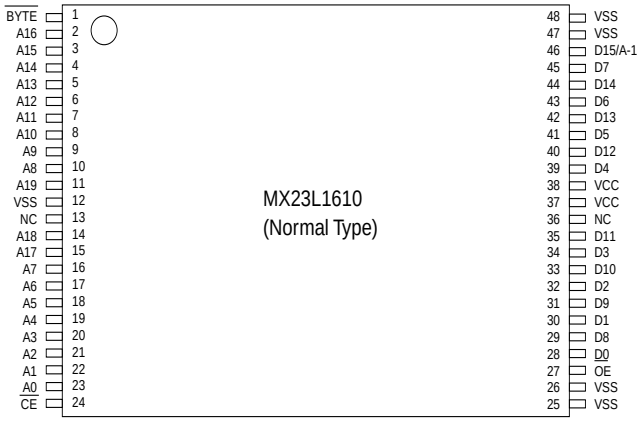
44 SOP/44 TSOP



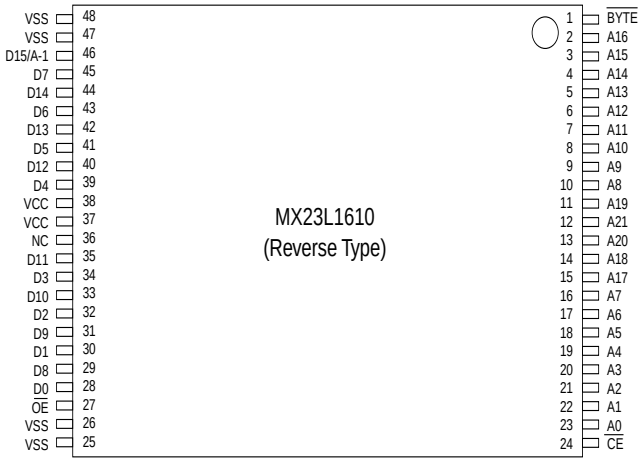
42 PDIP



48 TSOP (Normal Type)



48 TSOP (Reverse Type)



ORDER INFORMATION

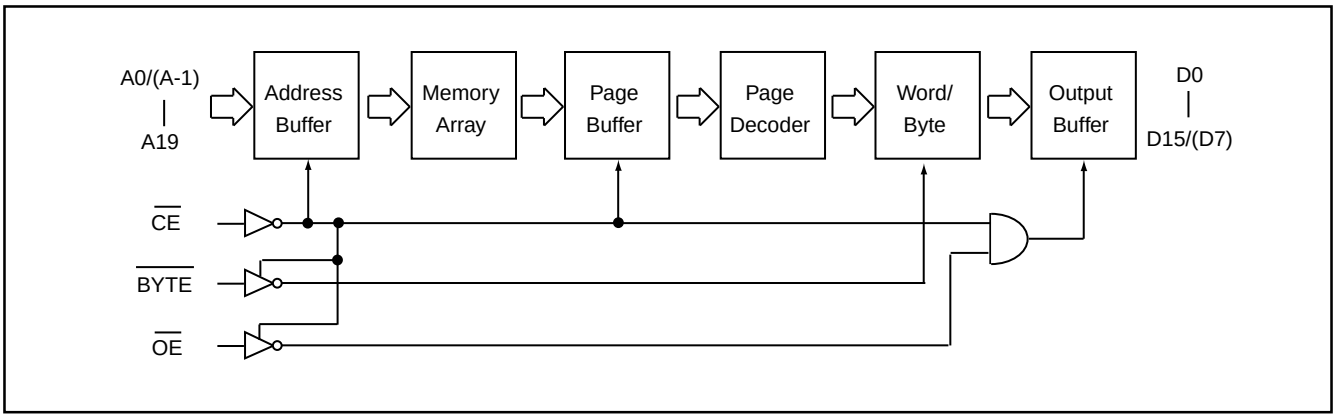
Part No.	Access	Package	Remark
MX23L1610MC-70	70ns	44 pin SOP	
MX23L1610MC-90	90ns	44 pin SOP	
MX23L1610MC-10	100ns	44 pin SOP	
MX23L1610MC-12	120ns	44 pin SOP	
MX23L1610MC-15	150ns	44 pin SOP	
MX23L1610PC-10	100ns	42 pin PDIP	
MX23L1610PC-12	120ns	42 pin PDIP	
MX23L1610PC-15	150ns	42 pin PDIP	
MX23L1610TC-70	70ns	48 pin TSOP	
MX23L1610TC-90	90ns	48 pin TSOP	
MX23L1610TC-10	100ns	48 pin TSOP	
MX23L1610TC-12	120ns	48 pin TSOP	
MX23L1610TC-15	150ns	48 pin TSOP	
MX23L1610RC-10	100ns	48 pin TSOP(Reverse type)	
MX23L1610RC-90	90ns	48 pin TSOP(Reverse type)	
MX23L1610RC-12	120ns	48 pin TSOP(Reverse type)	
MX23L1610RC-15	150ns	48 pin TSOP(Reverse type)	
MX23L1610TI-12*	120ns	48 pin TSOP	
MX23L1610YC-10	100ns	44 pin TSOP	
MX23L1610YC-12	120ns	44 pin TSOP	
MX23L1610YC-15	150ns	44 pin TSOP	
MX23L1610MI-12G*	120ns	44 pin SOP	Pb-free
MX23L1610MC-10G	100ns	44 pin SOP	Pb-free
MX23L1610MC-12G	120ns	44 pin SOP	Pb-free
MX23L1610PC-10G	100ns	42 pin PDIP	Pb-free
MX23L1610PC-12G	120ns	42 pin PDIP	Pb-free
MX23L1610TC-10G	100ns	48 pin TSOP	Pb-free
MX23L1610TC-12G	120ns	48 pin TSOP	Pb-free
MX23L1610TC-15G	150ns	48 pin TSOP	Pb-free

*Note:Temperature: -40~85° C

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Byte}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 4.3V
Ambient Operating Temperature	Topr	0° C to 70° C
Storage Temperature	Tstg	-65° C to 125° C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0° C ~ 70° C, VCC = 3.0V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V*	MAX. number:VCC+0.3V is under normal operation mode, and VCC+0.7V is under non-operating mode
Input Low Voltage	VIL	-0.3V	0.2 x VCC	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	25mA	tRC = 120ns, all output open
Standby Current (TTL)	ISTB1	-	0.5mA	$\overline{CE}$ = VIH
Standby Current (cmos)	ISTB2	-	15uA	$\overline{CE}$>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25° C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25° C, f = 1MHZ

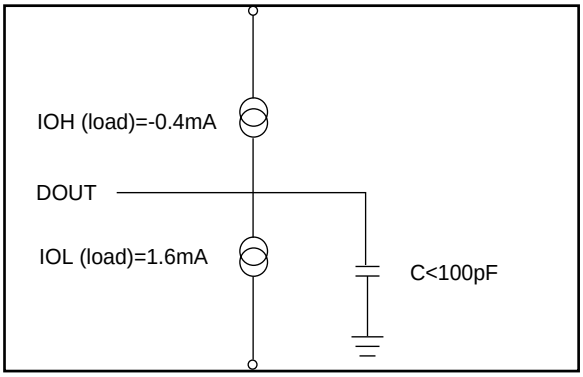
AC CHARACTERISTICS (Ta = 0° C ~ 70° C, VCC = 3.0V~3.6V)

Item	Symbol	23L1610-70		23L1610-90		23L1610-10		23L1610-12		23L1610-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	70ns	-	90ns	-	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	70ns	-	90ns	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	35ns	-	45ns	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note:

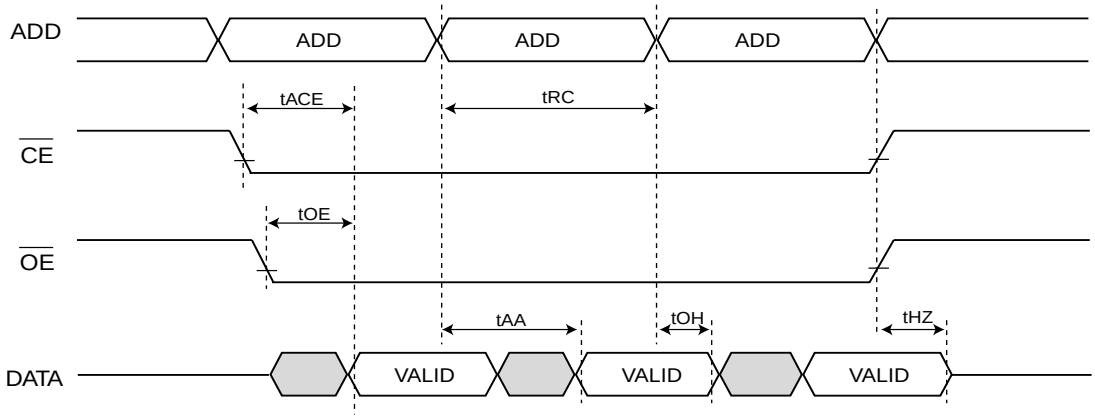
No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

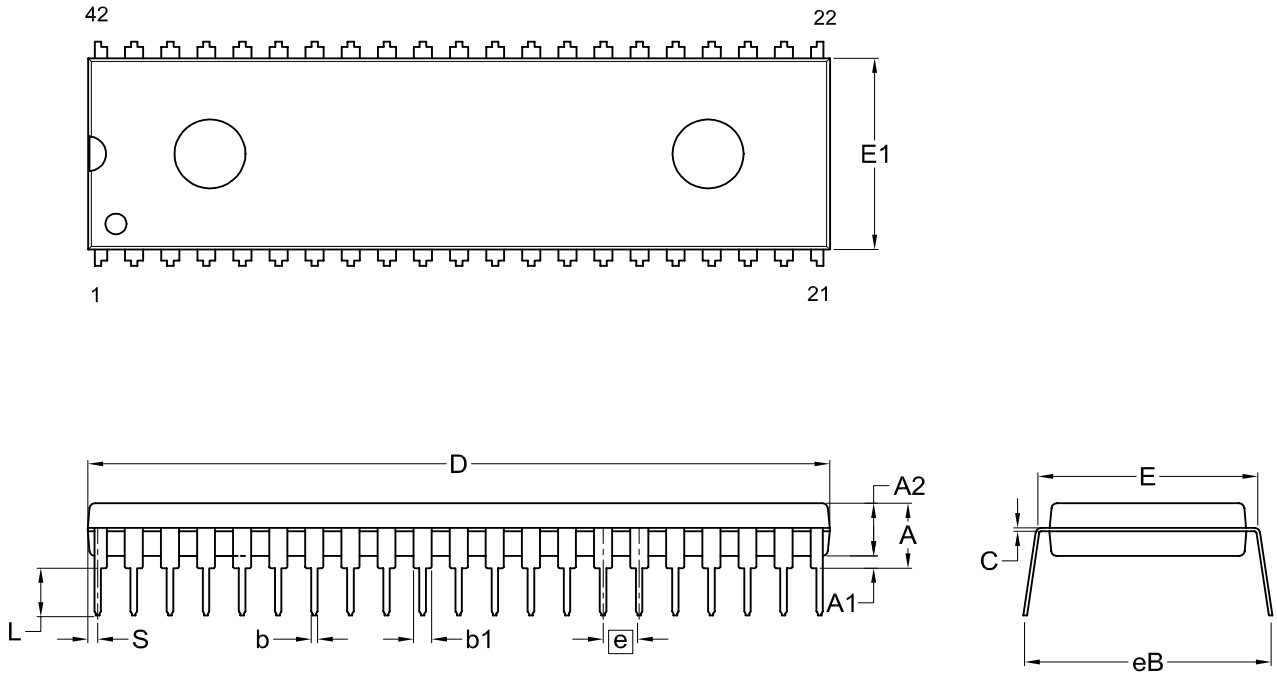
RANDOM READ



Note:$\overline{CE}$, $\overline{OE}$ are enable

PACKAGE INFORMATION

Title: **Package Outline for PDIP 42L (600MIL)**

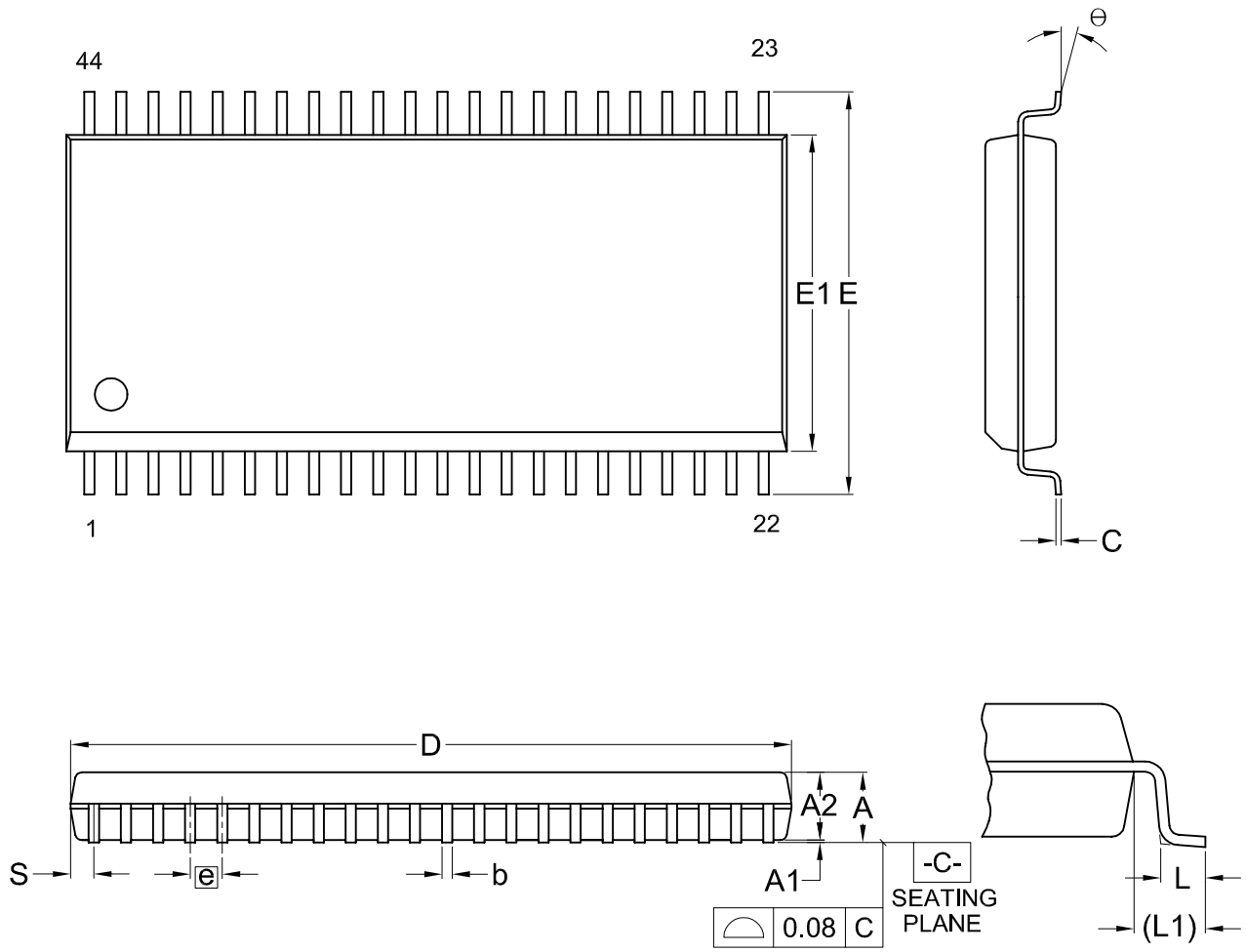


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.25	3.73	0.38	1.14	0.20	51.31	15.11	13.84		15.75	2.92	0.38
	Nom.	---	---	3.94	0.46	1.27	0.25	51.94	15.24	13.97	2.54	16.51	3.30	0.64
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.57	15.37	14.10		17.27	3.68	0.89
Inch	Min.	—	0.010	0.147	0.015	0.045	0.008	2.020	0.595	0.545		0.620	0.115	0.015
	Nom.	—	—	0.155	0.018	0.050	0.010	2.045	0.600	0.550	0.100	0.650	0.130	0.025
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.070	0.605	0.555		0.680	0.145	0.035

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.5	8				11-24-'03

Title: **Package Outline for SOP 44L (500MIL)**

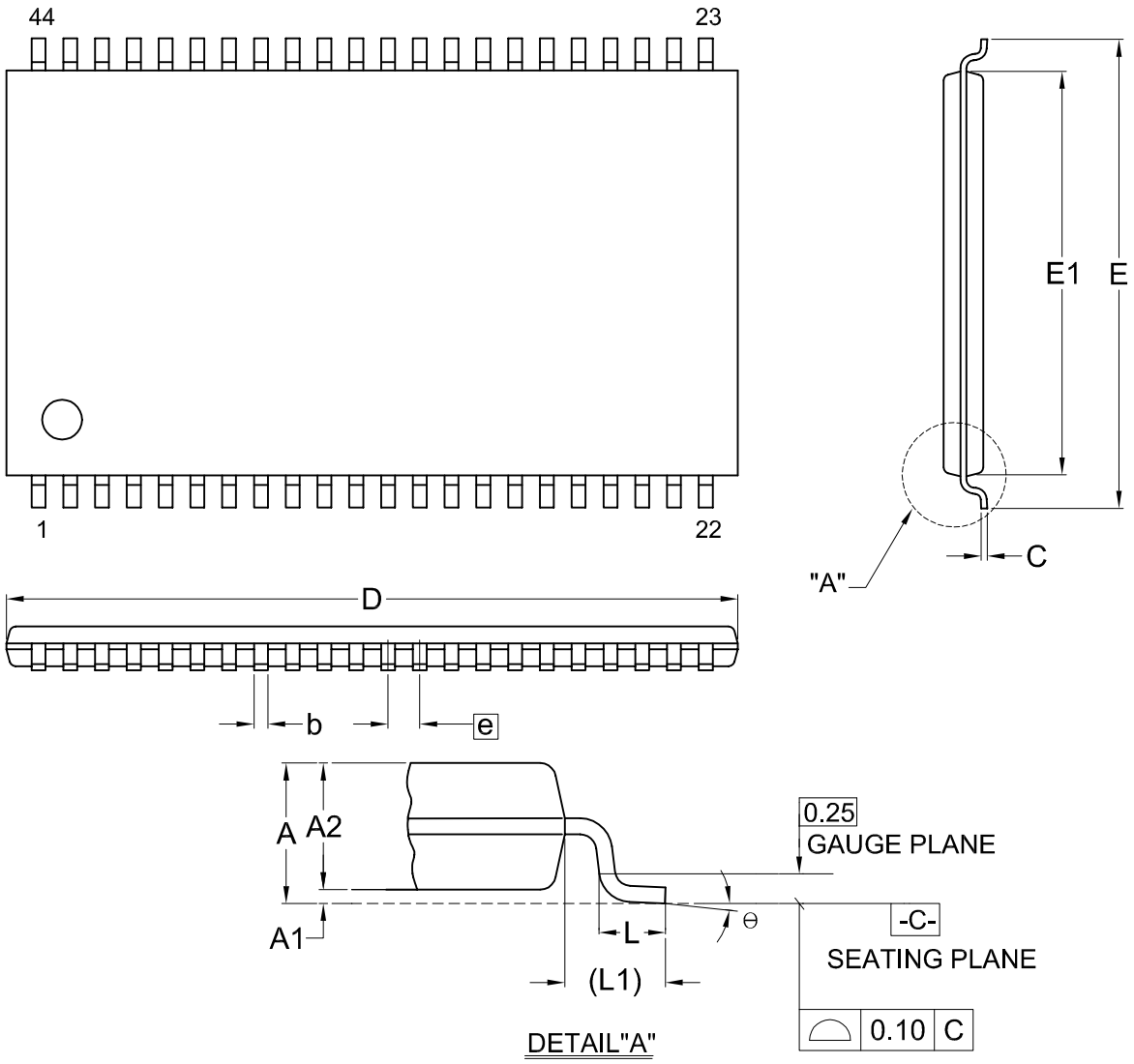


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	6	MO-175			11-26-'03

Title: **Package Outline for TSOP(II) 44L (400MIL)**

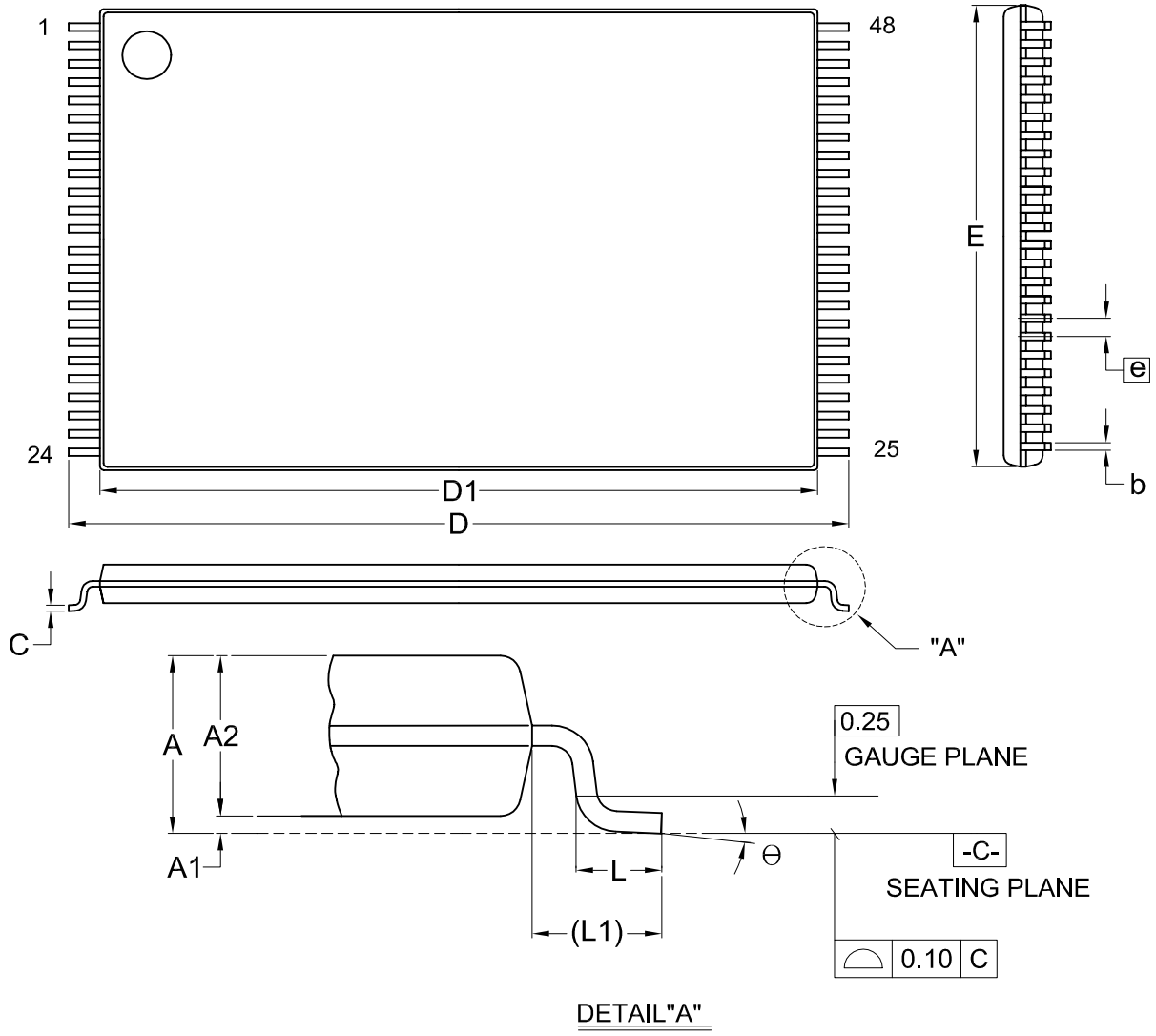


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.30	0.12	18.31	11.56	10.06		0.40	0.70	0
	Nom.	---	0.10	1.00	0.35	0.15	18.41	11.76	10.16	0.80	0.50	0.80	5
	Max.	1.20	0.15	1.05	0.45	0.21	18.51	11.96	10.26		0.60	0.90	8
Inch	Min.	---	0.002	0.037	0.012	0.005	0.721	0.455	0.396		0.016	0.028	0
	Nom.	---	0.004	0.039	0.014	0.006	0.725	0.463	0.400	0.031	0.020	0.031	5
	Max.	0.047	0.006	0.041	0.018	0.008	0.729	0.471	0.404		0.024	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1701	6	MS-024			12-01-'03

Title: **Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM**



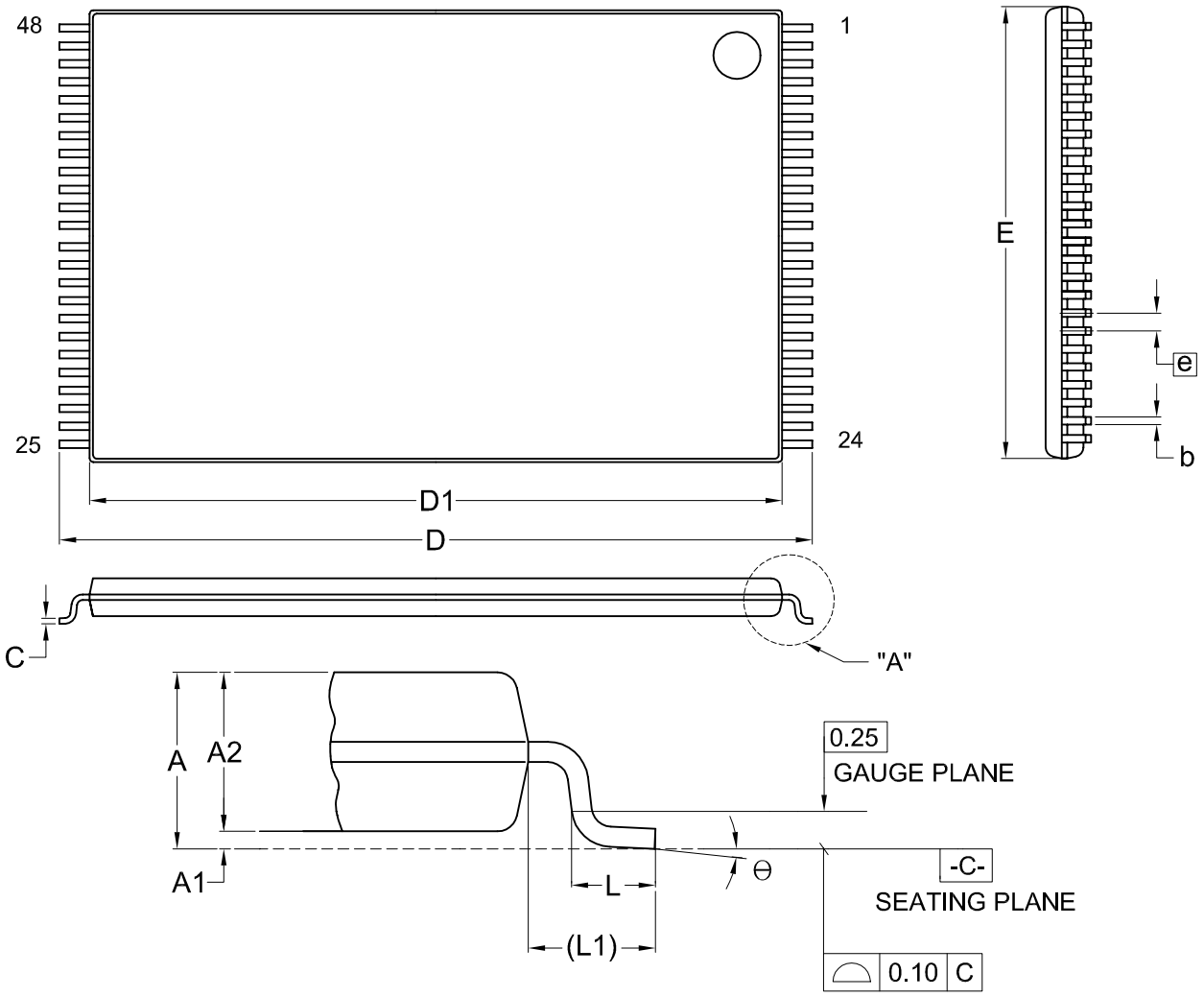
DETAIL"A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	7	MO-142			12-01-'03

Title: Package Outline for TSOP(I) 48L (12X20mm)REVERSE FORM



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	—	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	—	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607.1	7	MO-142			12-01-'03

REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
1.9	1. Package Type:Add 42-PDIP package type. 2. DC Characteristics:The input low voltage VIL Max. value is changed as 0.2xVCC instead of 0.8V. 3. AC Characteristics:The output high Z delay is changed as 20ns instead of 70ns. 4. Add 105ns speed grade. 5. Add 100ns speed grade @3.3V±5% 6. AC Test Conditions:The output timing level is changed as 1.4V instead of 0.8V and 2.0V.		JUN/11/1998
2.0	AC CHARACTERISTICS tOH 10ns-->0ns	P4	FEB/01/1999
2.1	Typing error correction	P1	JAN/18/2000
2.2	1.Added 44-pin TSOP (Type II) Package 2.Modify Package Information	P1,8 P5~7	JUL/18/2001
2.3	1.Add 90ns speed grade 2.Delete 105ns speed grade	P1,3 P1,3	JUL/31/2001
2.4	1.Added 70ns speed grade	P1,3	AUG/14/2001
2.5	Change VOH(MIN.):2.3V-->2.4V; VIH(MIN.):2.1V-->2.2V	P3	AUG/15/2001
2.6	Modify Package Information	P5~9	NOV/21/2002
2.7	Modify 42-PDIP Package Information	P5	JUN/20/2003
2.8	1. Add Pb-free in ordering information	P2	JUN/30/2004
2.9	Correct typo error	P2	NOV/09/2004
3.0	1. Added MX23L1610MI-12G in order information	P2	JUL/08/2005

MACRONIX INTERNATIONAL CO., LTD.

Headquarters:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

Europe Office :
TEL:+32-2-456-8020
FAX:+32-2-456-8021

Hong Kong Office :
TEL:+86-755-834-335-79
FAX:+86-755-834-380-78

Japan Office :
Kawasaki Office :
TEL:+81-44-246-9100
FAX:+81-44-246-9105
Osaka Office :
TEL:+81-6-4807-5460
FAX:+81-6-4807-5461

Singapore Office :
TEL:+65-6346-5505
FAX:+65-6348-8096

Taipei Office :
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-262-8887
FAX:+1-408-262-8810

http : //www.macronix.com