

DPDT SWITCH GaAs MMIC

■GENERAL DESCRIPTION

NJG1524APC1 is a DPDT switch GaAs MMIC.

The two same switches are merged into one package and functionally linked. It is useful for switching two circuits in-line.

Each switches feature very bw loss, high isolation and wide frequency coverage from 50MHz to 3GHz at low control voltage of 2.5V.

The ultra small & thin FFP16-C1package is adopted.

■PACKAGE OUTLINE



NJG1524APC1

■FEATURES

●Single low voltage control

●Low insertion loss

●High isolation

●Handling power

●Low current consumption

●Ultra small & thin package

+2.5~+6.5V

0.3dB typ. @f=1GHz, $P_{IN}=0dBm$, each switch

0.5dB typ. @f=2GHz, $P_{IN}=0dBm$, each switch

42dB typ. @f=2GHz, PC1-PC2

27dB typ. @f=2GHz, PC1-PA1 PC1-PA2, PC2-PB1, PC2-PB2, PA1-PA2, PB1-PB2

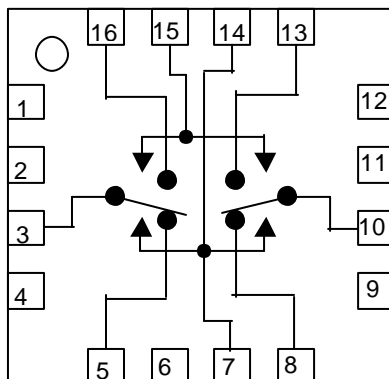
20dBm max. @f=2GHz, $V_{CTL}=2.7V$

16uA typ. @f=2GHz, $P_{IN}=10dBm$

FFP16-C1 (Package size: 2.5x2.5x0.85mm)

■PIN CONFIGURATION

FFP16 Type
(Top View)



Pin Connection

| | |
|---------|----------|
| 1.GND | 9.GND |
| 2.GND | 10.PC1 |
| 3.PC2 | 11.GND |
| 4.GND | 12.GND |
| 5.PB1 | 13.PA2 |
| 6.NC | 14.VCTL1 |
| 7.VCTL1 | 15.VCTL2 |
| 8.PA1 | 16.PB2 |

■TRUTH TABLE

“H”= $V_{CTL(H)}$, “L”= $V_{CTL(L)}$

| VCTL1 | H | L |
|------------------------|-----|-----|
| VCTL2 | L | H |
| PC1 – PA1 PC2 – PB1 | ON | OFF |
| PC1 – PA2 PC2 – PB2 | OFF | ON |

NOTE: Please note that any information on this catalog will be subject to change.

NJG1524APC1

■ABSOLUTE MAXIMUM RATINGS

($T_a=25^{\circ}\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | RATINGS | UNITS |
|-------------------|-----------|---|----------|--------------------|
| Input Power | P_{IN} | $V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=2.7\text{V}$ | 28 | dBm |
| Control voltage | V_{CTL} | $V_{CTL(H)} - V_{CTL(L)}$ | 7.5 | V |
| Power Dissipation | P_D | | 400 | mW |
| Operating Temp. | T_{opr} | | -40~+85 | $^{\circ}\text{C}$ |
| Storage Temp. | T_{stg} | | -55~+125 | $^{\circ}\text{C}$ |

■ELECTRICAL CHARACTERISTICS (EACH SWITCH)

($V_{CTL(L)}=0\text{V}$, $V_{CTL(H)}=2.7\text{V}$, $Z_S=Z_O=50\Omega$, $T_a=25^{\circ}\text{C}$)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|-------------------|--|------|-----|-----|---------------|
| Operating voltage (L) | $V_{CTL(L)}$ | | -0.2 | 0 | 0.2 | V |
| Operating voltage (H) | $V_{CTL(H)}$ | | 2.5 | 2.7 | 6.5 | V |
| Control Current | I_{CTL} | $f=2\text{GHz}$, $P_{IN}=10\text{dBm}$ | - | 16 | 28 | μA |
| Insertion loss1 | Loss1 | PC1-PA1, PC1-PA2, PC2-PB1, PC2-PB2 ON, $f=1\text{GHz}$, $P_{IN}=0\text{dBm}$ | - | 0.3 | 0.6 | dB |
| Insertion loss2 | Loss2 | PC1-PA1, PC1-PA2, PC2-PB1, PC2-PB2 ON, $f=2\text{GHz}$, $P_{IN}=0\text{dBm}$ | - | 0.5 | 0.8 | dB |
| Isolation1 | ISL1 | PC1-PA1, PC1-PA2, PC2-PB1, PC2-PB2 OFF, $f=1\text{GHz}$, $P_{IN}=0\text{dBm}$ | 25.5 | 27 | - | dB |
| Isolation2 | ISL2 | PC1-PA1, PC1-PA2, PC2-PB1, PC2-PB2 OFF, $f=2\text{GHz}$, $P_{IN}=0\text{dBm}$ | 25 | 27 | - | dB |
| Isolation3 | ISL3 | PA1, PA2, PB1, PB2 port 50 Ω terminal, PC1-PC2 port, $f=2\text{GHz}$, $P_{IN}=0\text{dBm}$ $V_{CTL1}=2.7\text{V}$ | 39 | 42 | - | dB |
| Pin at 1dB compression point | $P_{-1\text{dB}}$ | $f=2\text{GHz}$ | 20 | 23 | - | dBm |
| VSWR (PC, P1, P2) | VSWR | $f=0.05\sim 2\text{GHz}$, ON State | - | 1.3 | 1.6 | |
| Switch time | T_{sw} | $f=0.05\sim 2.5\text{GHz}$ | - | 40 | 60 | ns |

■ TERMINAL INFORMATION

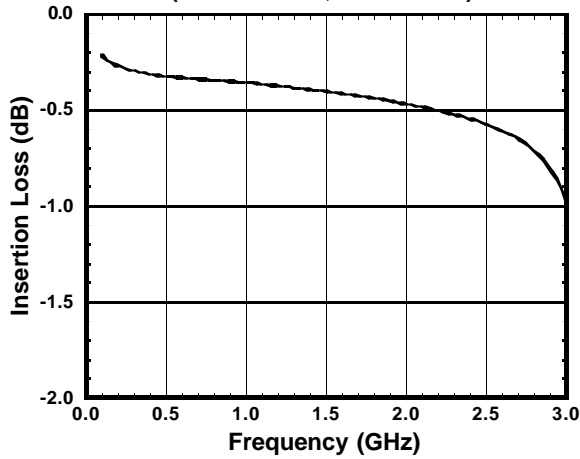
| No. | SYMBOL | DESCRIPTIONS |
|--------------------|--------|---|
| 3 | PC2 | Common RF port C2. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 5 | PB1 | RF port B1. This port is connected with PC1 port by controlling VCTL2 to -0.2~+0.2V and VCTL1 to 2.5~6.5V. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 6 | NC | No connected terminal. |
| 7 | VCTL1 | Control port 1. The voltage of this port controls PC1 to PA1/PA2 and PC2 to PB1/PB2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal to high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of VCTL2 should be set to opposite state. The bypass capacitor should be connected with GND as close as possible for excellent RF performance. |
| 8 | PA1 | RF port A1. This port is connected with PC1 port by controlling VCTL2 to -0.2~+0.2V and VCTL1 to 2.5~6.5V. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 10 | PC1 | Common RF port C1. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 13 | PA2 | RF port A2. This port is connected with PC1 port by controlling $V_{CTL(L)}$ to -0.2~+0.2V and $V_{CTL(H)}$ to 2.5~6.5V. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 14 | VCTL1 | Control port 1. The voltage of this port controls PC1 to PA1/PA2 and PC2 to PB1/PB2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal to high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of VCTL2 should be set to opposite state. The bypass capacitor should be connected with GND as close as possible for excellent RF performance. |
| 15 | VCTL2 | Control port 2. The voltage of this port controls PC1 to PA1/PA2 and PC2 to PB1/PB2 state. The 'ON' and 'OFF' state is toggled by controlling voltage of this terminal to high-state (2.5~6.5V) or low-state (-0.2~+0.2V). The voltage of VCTL1 should be set to opposite state. The bypass capacitor should be connected with GND as close as possible for excellent RF performance. |
| 16 | PB2 | RF port B2. This port is connected with PC2 port by controlling VCTL1 to -0.2~+0.2V and VCTL2 to 2.5~6.5V. In order to block the DC bias voltage of internal circuit, an external capacitor is required. |
| 1, 2, 4, 9, 11, 12 | GND | Ground terminal. Please connect this terminal with ground plane as close as possible for excellent RF performance. |

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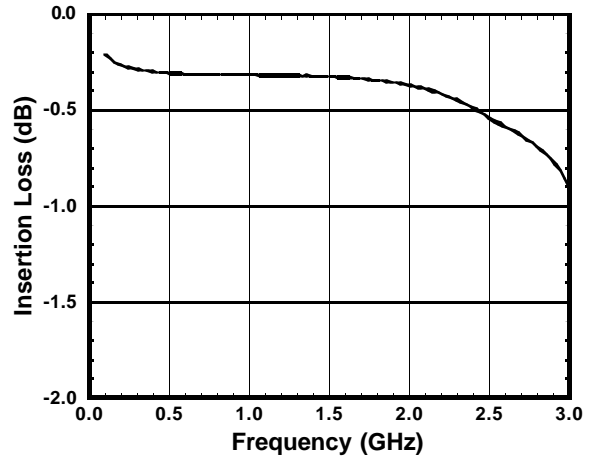
■ TYPICAL CHARACTERISTICS

(50MHz~3GHz, with application circuit, without DC blocking capacitor, losses of circuit are excluded.)

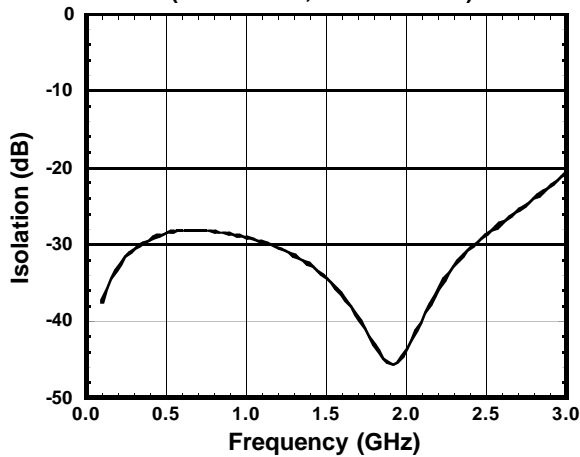
PC1-PA1 Insetion Loss vs. Frequency
(VCTL1=2.7V, VCTL2=0V)



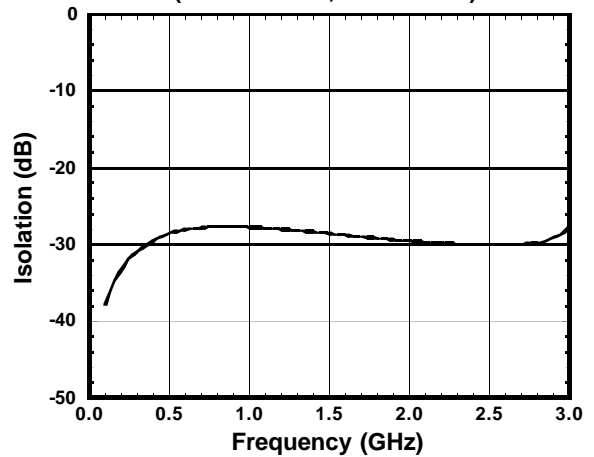
PC1-PA2 Insetion Loss vs. Frequency
(VCTL1=0V, VCTL2=2.7V)



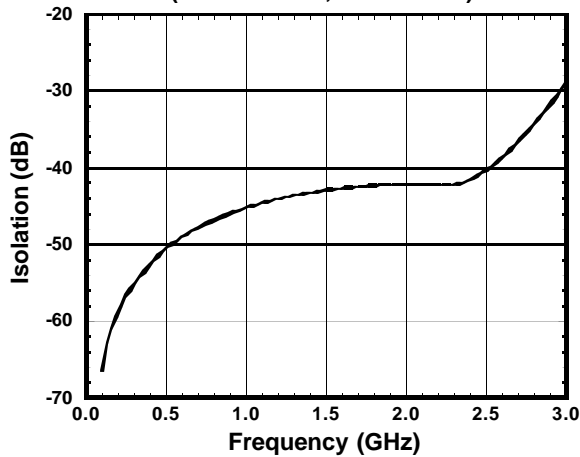
PC1-PA1 Isolation vs. Frequency
(VCTL1=0V, VCTL2=2.7V)



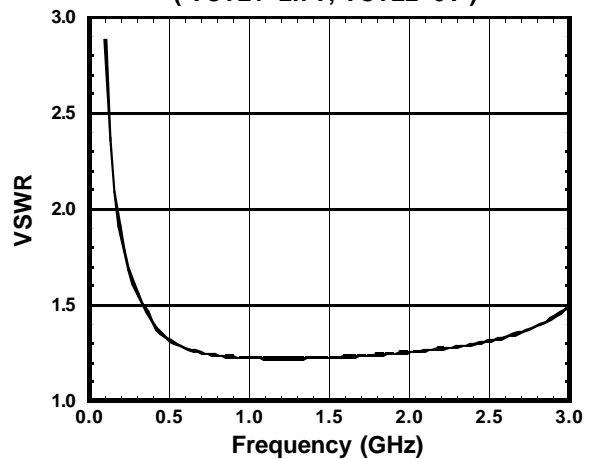
PC1-PA2 Isolation vs. Frequency
(VCTL1=2.7V, VCTL2=0V)



PC1-PC2 Isolation vs. Frequency
(VCTL1=2.7V, VCTL2=0V)



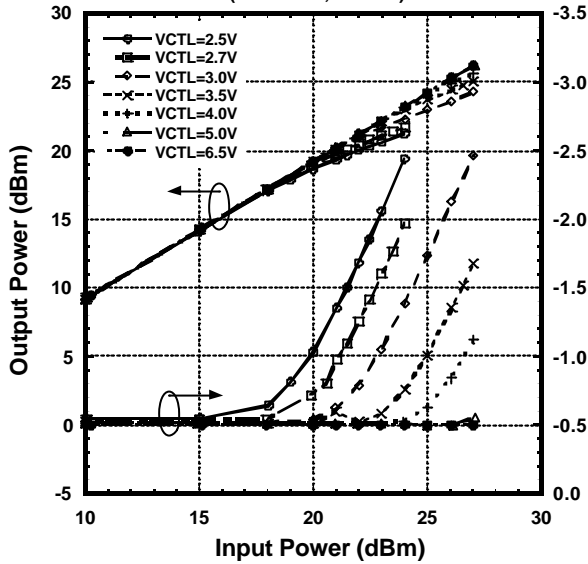
PA1 VSWR vs. Frequency
(VCTL1=2.7V, VCTL2=0V)



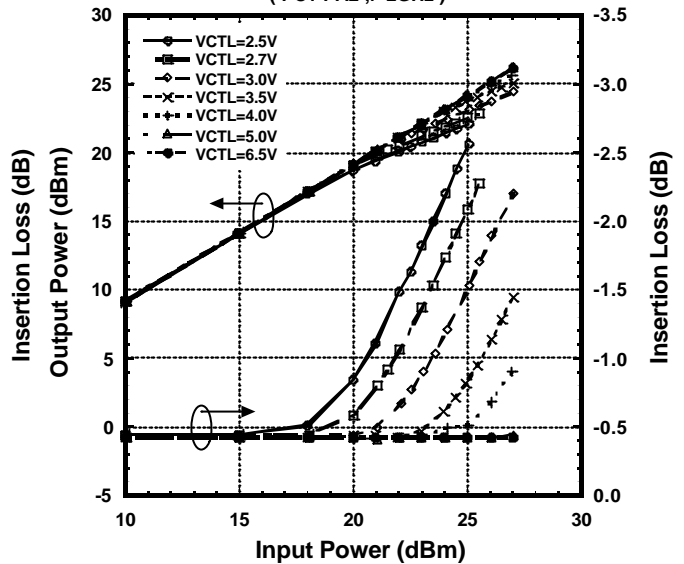
TYPICAL CHARACTERISTICS

(50MHz~3GHz, with application circuit, without DC blocking capacitor, losses of circuit are excluded.)

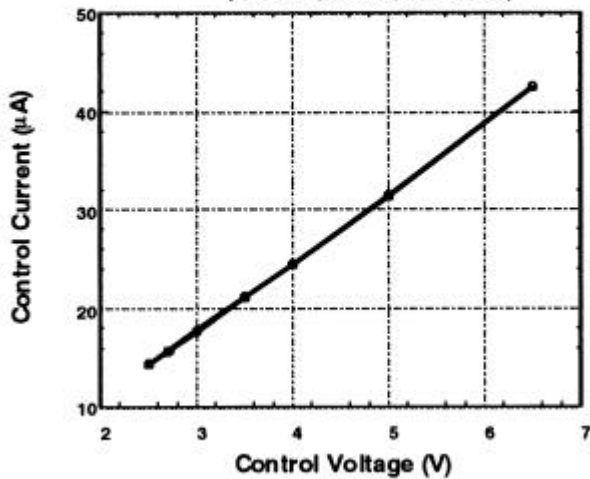
Output Power ,Insertion Loss vs. Input Power
(PC1-PA1 ,f=2GHz)



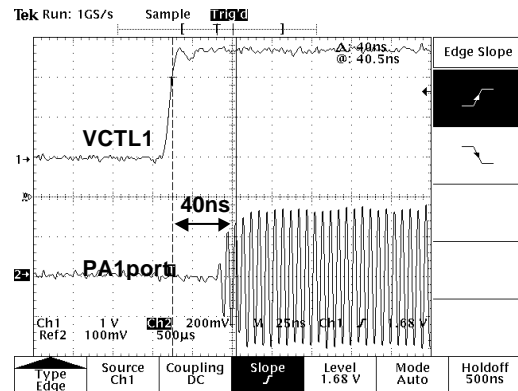
Output Power ,Insertion Loss vs. Input Power
(PC1-PA2 ,f=2GHz)



Control Current vs. Control Voltage
(PC1-PA1 ,f=1GHz ,Pin=10dBm)



Switching Speed
(VCTL=2.7V, Pin=10dBm)

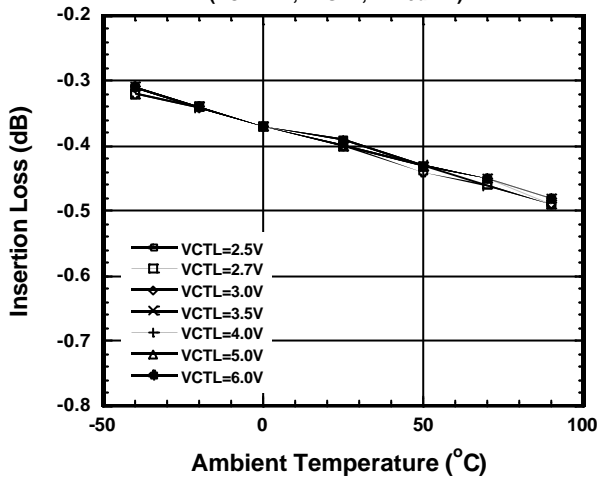


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TYPICAL CHARACTERISTICS

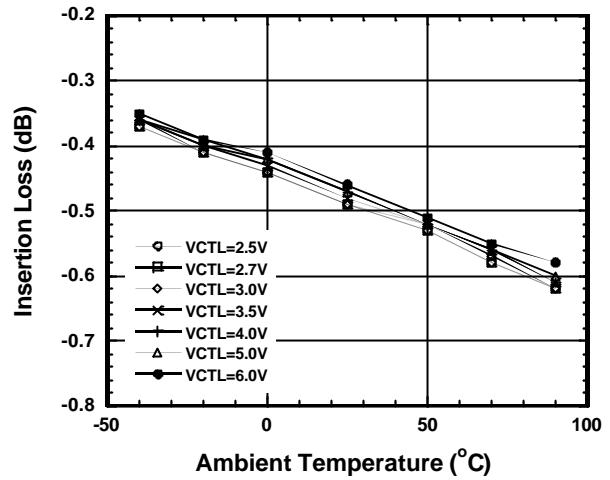
Insertion Loss vs. Ambient Temperature

(PC1-PA2, f=1GHz, Pin=0dBm)



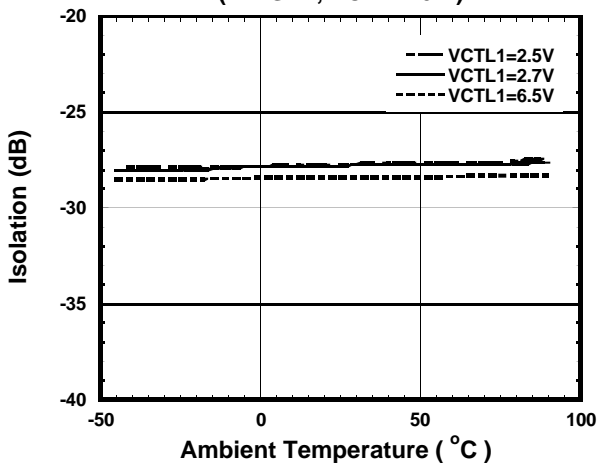
Insertion Loss vs. Ambient Temperature

(PC1-PA2, f=2GHz, Pin=0dBm)



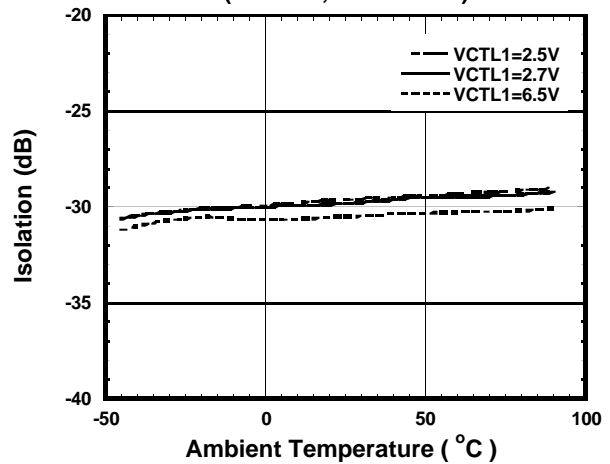
PC1-PA2 Isolation vs. Ambient Temperature

(f=1GHz, VCTL2=0V)



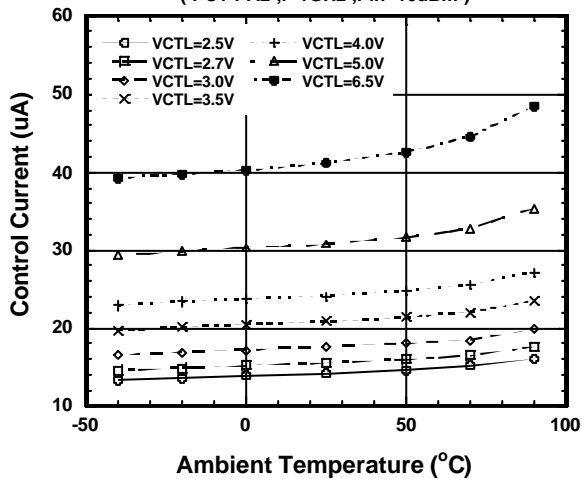
PC1-PA2 Isolation vs. Ambient Temperature

(f=2GHz, VCTL2=0V)



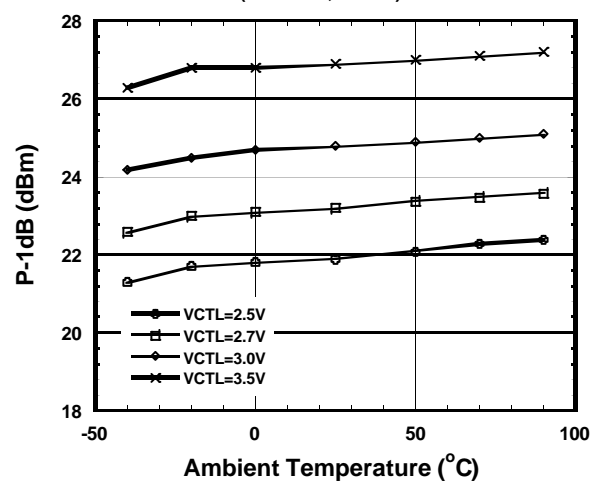
Control Current vs. Ambient Temperature

(PC1-PA2, f=1GHz, Pin=10dBm)

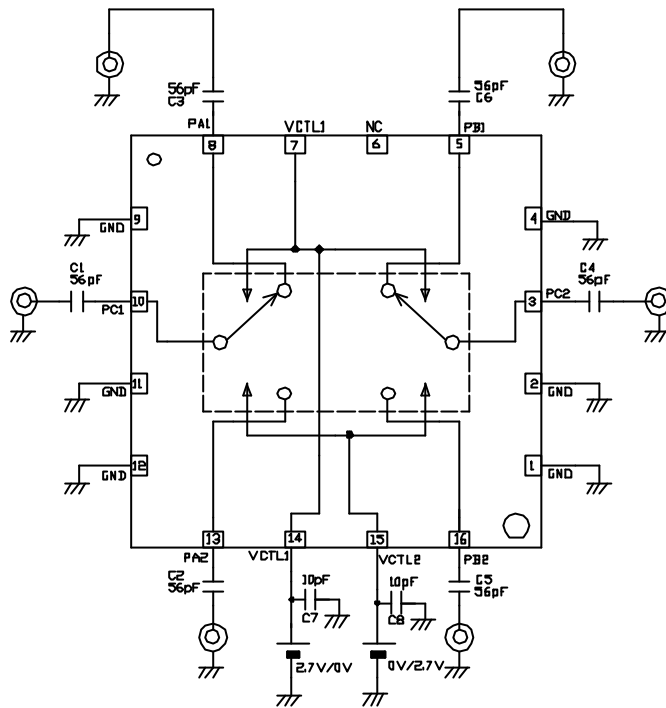


P-1dB vs. Ambient Temperature

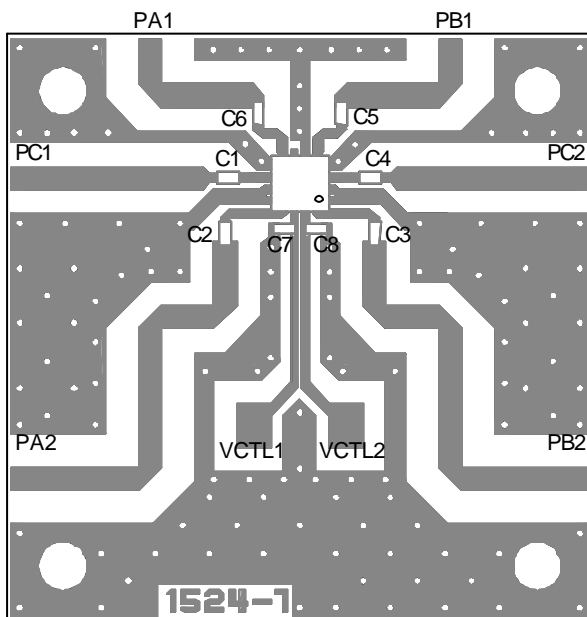
(PC1-PA2, f=2GHz)



APPLICATION CIRCUIT



RECOMMENDED PCB DESIGN



PCB SIZE=26x26mm
 PCB: FR-4, t=0.5mm
 CAPACITOR: size 1005
 Strip line width=1.0mm

Parts table

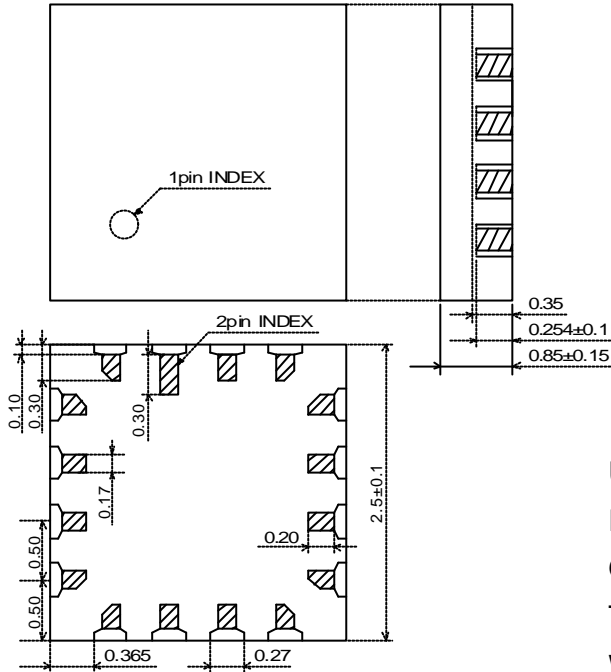
| Parts ID | 1 | 2 | 3 |
|----------|----------------|-----------------|-----------------|
| | fin=50-100 MHz | fin=0.1-0.5 GHz | fin=0.5-2.5 GHz |
| C1-C6 | 0.01uF | 1000pF | 56pF |
| C7,C8 | 10pF | 10pF | 10pF |

PRECAUTION

- [1]The DC blocking capacitor have to be placed at RF terminal of PC1, PC2, PA1, PA2, PB1, PB2. Please choose appropriate capacitance values to the application frequency.
- [2]To reduce stripline influence on RF characteristics, please locate bypass capacitors (C7, C8) close to each terminal.
- [3]For good isolation the GND terminal must be placed possibly close to ground place of substrate, and through holes for GND should be placed near by the pin connection.

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PACKAGE OUTLINE (FFP16-C1)



| | |
|----------------|---------------|
| UNIT | : mm |
| PCB | : Ceramic |
| OVER COAT | : Epoxy resin |
| TERMINAL TREAT | : Au |
| WEIGHT | : 15mg |

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.

- To waste this product, please obey the relative law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.