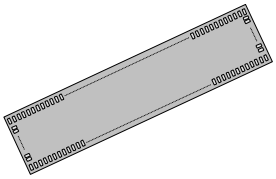
132COMMON x 132RGB LCD DRIVER FOR 65,536-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The **NJU6854** is a 132COMMON x 132RGB LCD driver for 65,536-color STN display. It contains common drivers, RGB drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 278,784-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 64 or 32 grayscales from a built-in grayscale palette, and the LSI achieves 65,536 colors (64x32x32).

In addition, the **NJU6854** operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



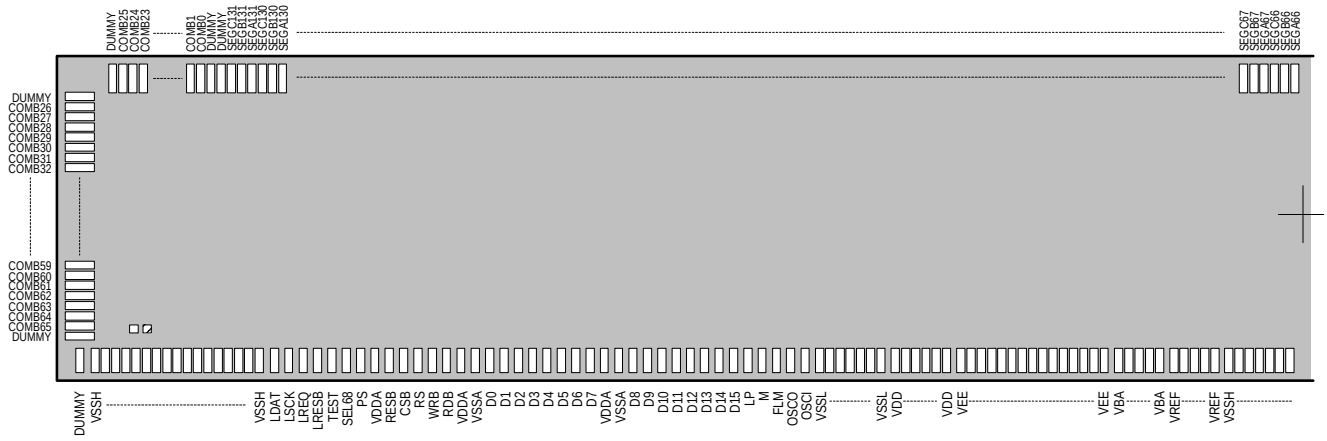
BUMP CHIP

■ FEATURES

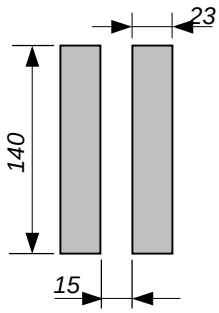
- 65,536-color STN LCD driver
- Built-in LCD Drivers : 132-common x 132RGB (396-segment drivers)
- Built-in Display Data RAM (DDRAM) : 278,784 bits for Graphic Display
- Programmable Display Mode
  - 64 grayscales(Green)
  - 32 grayscales(Red, Blue)
- 3 Areas Partial Display
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 6 times
- Programmable Contrast Control : 128-step Electronic Volume Register (EVR)
- Various Useful Instructions
- Low Operating Current
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip

TABLE OF CONTENTS

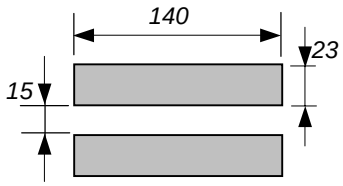
■ PAD LOCATION



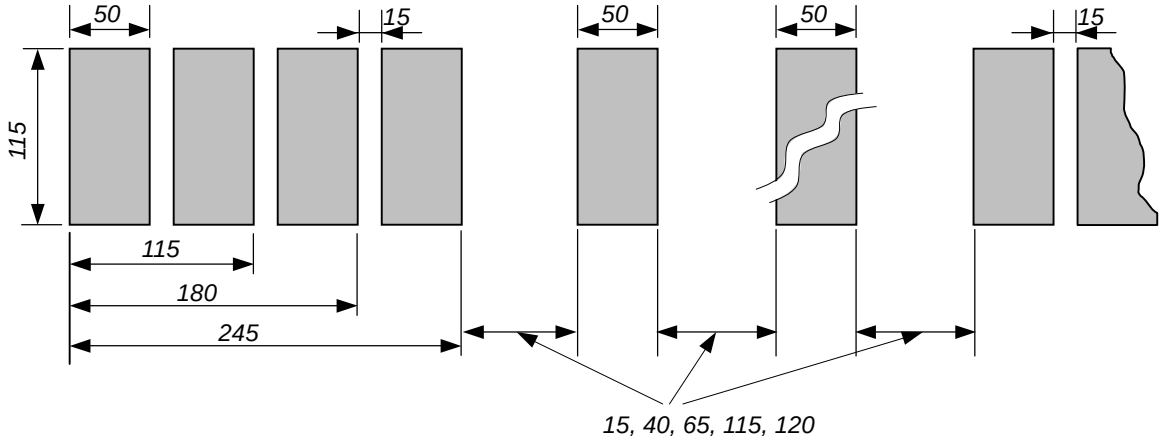
SEGA0~SEGC131, COMA0~COMA25, COMB0~COMB25, DUMMY



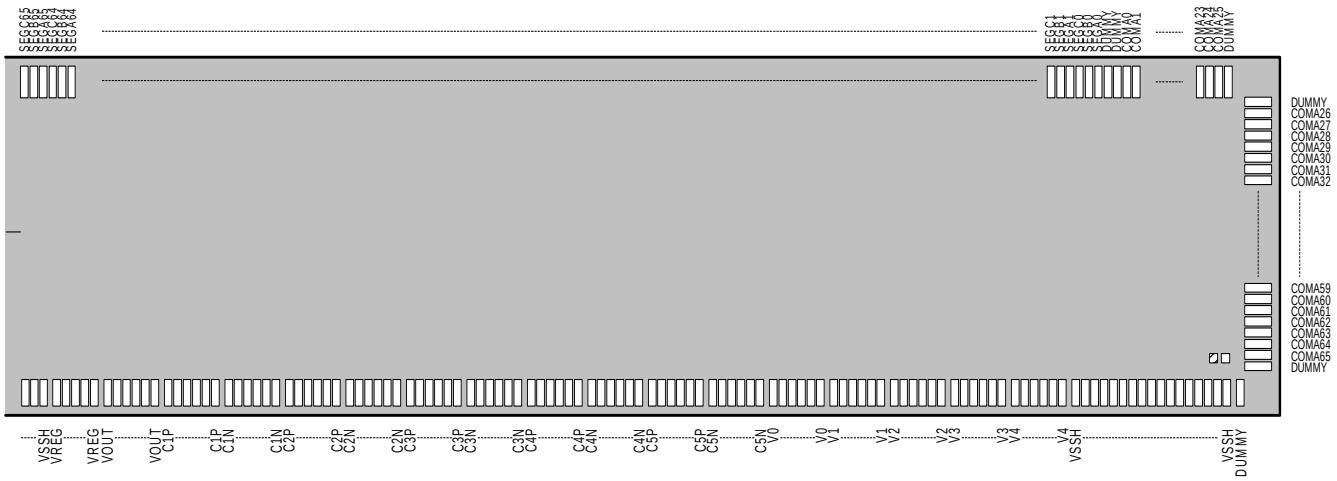
COMA26~COMA65, COMB26~COMB65, DUMMY



CPU interface pads and other pads



Bump Material : Au (gold)

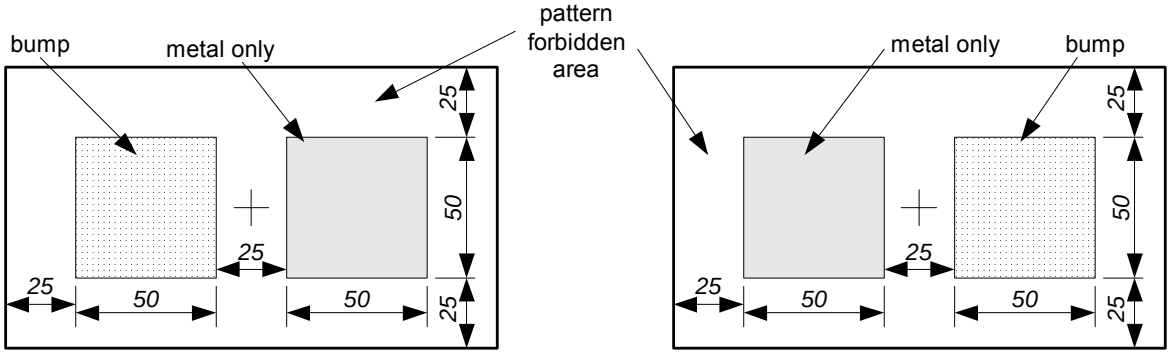


Note 1) The pads with the same name are connected within the chip.
Note 2) Dummy pads are kept open..

UNIT: um

ITEMS	REMARK / PAD NO.	SIZE	
		X	Y
Chip size	With scribe lane (100 um)	17,643	2,180
PAD pitch / space (bump)	Driver pads pitch	38	
	Interface pads	70~170	
PAD open side	Driver sides	9	126
	Interface sides	9	96
PAD size (bump)	Driver sides	23	140
	Interface sides	50	115
BUMP height	All pads	17.5	

ALIGN MARK DESIGN



Coordinates LEFT BOTTOM : X= -8157.92 Y= -515.62
RIGHT BOTTOM : X= 8157.92 Y= -515.62

■ PAD COORDINATES

chip size 17,643 × 2,180 μm² (chip center = 0:0)

PAD No.	Pad name	X(μm)	Y(μm)	PAD No.	Pad name	X (μm)	Y (μm)	PAD No.	Pad name	X (μm)	Y (μm)
1	DUMMY	-8620.0	-935.5	51	D15	-3695.0	-935.5	101	VSSHA	-20.0	-935.5
2	VSSH	-8530.0	-935.5	52	LP	-3580.0	-935.5	102	VSSHA	45.0	-935.5
3	VSSH	-8465.0	-935.5	53	M	-3465.0	-935.5	103	VSSHA	110.0	-935.5
4	VSSH	-8400.0	-935.5	54	FLM	-3350.0	-935.5	104	VSSHA	175.0	-935.5
5	VSSH	-8335.0	-935.5	55	OSCO	-3235.0	-935.5	105	VREG	340.0	-935.5
6	VSSH	-8270.0	-935.5	56	OSCI	-3120.0	-935.5	106	VREG	405.0	-935.5
7	VSSH	-8205.0	-935.5	57	VSS	-3005.0	-935.5	107	VREG	470.0	-935.5
8	VSSH	-8140.0	-935.5	58	VSS	-2940.0	-935.5	108	VREG	535.0	-935.5
9	VSSH	-8075.0	-935.5	59	VSS	-2875.0	-935.5	109	VREG	600.0	-935.5
10	VSSH	-8010.0	-935.5	60	VSS	-2810.0	-935.5	110	VOUT	690.0	-935.5
11	VSSH	-7945.0	-935.5	61	VSS	-2745.0	-935.5	111	VOUT	755.0	-935.5
12	VSSH	-7880.0	-935.5	62	VSS	-2680.0	-935.5	112	VOUT	820.0	-935.5
13	VSSH	-7815.0	-935.5	63	VSS	-2615.0	-935.5	113	VOUT	885.0	-935.5
14	VSSH	-7750.0	-935.5	64	VDD	-2525.0	-935.5	114	VOUT	950.0	-935.5
15	VSSH	-7685.0	-935.5	65	VDD	-2460.0	-935.5	115	VOUT	1015.0	-935.5
16	VSSH	-7620.0	-935.5	66	VDD	-2395.0	-935.5	116	C1+	1105.0	-935.5
17	VSSH	-7555.0	-935.5	67	VDD	-2330.0	-935.5	117	C1+	1170.0	-935.5
18	VSSH	-7490.0	-935.5	68	VDD	-2265.0	-935.5	118	C1+	1235.0	-935.5
19	LDAT	-7375.0	-935.5	69	VDD	-2200.0	-935.5	119	C1+	1300.0	-935.5
20	LSCK	-7260.0	-935.5	70	VEE	-2110.0	-935.5	120	C1+	1365.0	-935.5
21	LREQ	-7145.0	-935.5	71	VEE	-2045.0	-935.5	121	C1+	1430.0	-935.5
22	LRESb	-7030.0	-935.5	72	VEE	-1980.0	-935.5	122	C1-	1520.0	-935.5
23	TEST	-6915.0	-935.5	73	VEE	-1915.0	-935.5	123	C1-	1585.0	-935.5
24	SEL68	-6800.0	-935.5	74	VEE	-1850.0	-935.5	124	C1-	1650.0	-935.5
25	PS	-6685.0	-935.5	75	VEE	-1785.0	-935.5	125	C1-	1715.0	-935.5
26	VDDA	-6570.0	-935.5	76	VEE	-1720.0	-935.5	126	C1-	1780.0	-935.5
27	RESb	-6455.0	-935.5	77	VEE	-1655.0	-935.5	127	C1-	1845.0	-935.5
28	CSb	-6340.0	-935.5	78	VEE	-1590.0	-935.5	128	C2+	1935.0	-935.5
29	RS	-6225.0	-935.5	79	VEE	-1525.0	-935.5	129	C2+	2000.0	-935.5
30	WRb	-6110.0	-935.5	80	VEE	-1460.0	-935.5	130	C2+	2065.0	-935.5
31	RDb	-5995.0	-935.5	81	VEE	-1395.0	-935.5	131	C2+	2130.0	-935.5
32	VDDA	-5880.0	-935.5	82	VEE	-1330.0	-935.5	132	C2+	2195.0	-935.5
33	VSSA	-5765.0	-935.5	83	VEE	-1265.0	-935.5	133	C2+	2260.0	-935.5
34	D0	-5650.0	-935.5	84	VEE	-1200.0	-935.5	134	C2-	2350.0	-935.5
35	D1	-5535.0	-935.5	85	VBA	-1110.0	-935.5	135	C2-	2415.0	-935.5
36	D2	-5420.0	-935.5	86	VBA	-1045.0	-935.5	136	C2-	2480.0	-935.5
37	D3	-5305.0	-935.5	87	VBA	-980.0	-935.5	137	C2-	2545.0	-935.5
38	D4	-5190.0	-935.5	88	VBA	-915.0	-935.5	138	C2-	2610.0	-935.5
39	D5	-5075.0	-935.5	89	VBA	-850.0	-935.5	139	C2-	2675.0	-935.5
40	D6	-4960.0	-935.5	90	VREF	-760.0	-935.5	140	C3+	2765.0	-935.5
41	D7	-4845.0	-935.5	91	VREF	-695.0	-935.5	141	C3+	2830.0	-935.5
42	VDDA	-4730.0	-935.5	92	VREF	-630.0	-935.5	142	C3+	2895.0	-935.5
43	VSSA	-4615.0	-935.5	93	VREF	-565.0	-935.5	143	C3+	2960.0	-935.5
44	D8	-4500.0	-935.5	94	VREF	-500.0	-935.5	144	C3+	3025.0	-935.5
45	D9	-4385.0	-935.5	95	VSSHA	-410.0	-935.5	145	C3+	3090.0	-935.5
46	D10	-4270.0	-935.5	96	VSSHA	-345.0	-935.5	146	C3-	3180.0	-935.5
47	D11	-4155.0	-935.5	97	VSSHA	-280.0	-935.5	147	C3-	3245.0	-935.5
48	D12	-4040.0	-935.5	98	VSSHA	-215.0	-935.5	148	C3-	3310.0	-935.5
49	D13	-3925.0	-935.5	99	VSSHA	-150.0	-935.5	149	C3-	3375.0	-935.5
50	D14	-3810.0	-935.5	100	VSSHA	-85.0	-935.5	150	C3-	3440.0	-935.5

chip size 17,643 ×2,180 μm2 (chip center = 0:0)

PAD No.	Pad name	X(μm)	Y(μm)	PAD No.	Pad name	X (μm)	Y (μm)	PAD No.	Pad name	X (μm)	Y (μm)
151	C3-	3505	-935.5	201	V4	7140	-935.5	251	COMA39	8652	232
152	C4+	3595	-935.5	202	V4	7205	-935.5	252	COMA38	8652	270
153	C4+	3660	-935.5	203	V4	7270	-935.5	253	COMA37	8652	308
154	C4+	3725	-935.5	204	V4	7335	-935.5	254	COMA36	8652	346
155	C4+	3790	-935.5	205	V4	7400	-935.5	255	COMA35	8652	384
156	C4+	3855	-935.5	206	VSSH	7490	-935.5	256	COMA34	8652	422
157	C4+	3920	-935.5	207	VSSH	7555	-935.5	257	COMA33	8652	460
158	C4-	4010	-935.5	208	VSSH	7620	-935.5	258	COMA32	8652	498
159	C4-	4075	-935.5	209	VSSH	7685	-935.5	259	COMA31	8652	536
160	C4-	4140	-935.5	210	VSSH	7750	-935.5	260	COMA30	8652	574
161	C4-	4205	-935.5	211	VSSH	7815	-935.5	261	COMA29	8652	612
162	C4-	4270	-935.5	212	VSSH	7880	-935.5	262	COMA28	8652	650
163	C4-	4335	-935.5	213	VSSH	7945	-935.5	263	COMA27	8652	688
164	C5+	4425	-935.5	214	VSSH	8010	-935.5	264	COMA26	8652	726
165	C5+	4490	-935.5	215	VSSH	8075	-935.5	265	DUMMY	8652	764
166	C5+	4555	-935.5	216	VSSH	8140	-935.5	266	DUMMY	8607	920.5
167	C5+	4620	-935.5	217	VSSH	8205	-935.5	267	COMA25	8569	920.5
168	C5+	4685	-935.5	218	VSSH	8270	-935.5	268	COMA24	8531	920.5
169	C5+	4750	-935.5	219	VSSH	8335	-935.5	269	COMA23	8493	920.5
170	C5-	4840	-935.5	220	VSSH	8400	-935.5	270	COMA22	8455	920.5
171	C5-	4905	-935.5	221	VSSH	8465	-935.5	271	COMA21	8417	920.5
172	C5-	4970	-935.5	222	VSSH	8530	-935.5	272	COMA20	8379	920.5
173	C5-	5035	-935.5	223	DUMMY	8620	-935.5	273	COMA19	8341	920.5
174	C5-	5100	-935.5	224	DUMMY	8652	-794	274	COMA18	8303	920.5
175	C5-	5165	-935.5	225	COMA65	8652	-756	275	COMA17	8265	920.5
176	V0	5335	-935.5	226	COMA64	8652	-718	276	COMA16	8227	920.5
177	V0	5400	-935.5	227	COMA63	8652	-680	277	COMA15	8189	920.5
178	V0	5465	-935.5	228	COMA62	8652	-642	278	COMA14	8151	920.5
179	V0	5530	-935.5	229	COMA61	8652	-604	279	COMA13	8113	920.5
180	V0	5595	-935.5	230	COMA60	8652	-566	280	COMA12	8075	920.5
181	V0	5660	-935.5	231	COMA59	8652	-528	281	COMA11	8037	920.5
182	V1	5750	-935.5	232	COMA58	8652	-490	282	COMA10	7999	920.5
183	V1	5815	-935.5	233	COMA57	8652	-452	283	COMA9	7961	920.5
184	V1	5880	-935.5	234	COMA56	8652	-414	284	COMA8	7923	920.5
185	V1	5945	-935.5	235	COMA55	8652	-376	285	COMA7	7885	920.5
186	V1	6010	-935.5	236	COMA54	8652	-338	286	COMA6	7847	920.5
187	V1	6075	-935.5	237	COMA53	8652	-300	287	COMA5	7809	920.5
188	V2	6165	-935.5	238	COMA52	8652	-262	288	COMA4	7771	920.5
189	V2	6230	-935.5	239	COMA51	8652	-224	289	COMA3	7733	920.5
190	V2	6295	-935.5	240	COMA50	8652	-186	290	COMA2	7695	920.5
191	V2	6360	-935.5	241	COMA49	8652	-148	291	COMA1	7657	920.5
192	V2	6425	-935.5	242	COMA48	8652	-110	292	COMA0	7619	920.5
193	V2	6490	-935.5	243	COMA47	8652	-72	293	DUMMY	7581	920.5
194	V3	6660	-935.5	244	COMA46	8652	-34	294	DUMMY	7543	920.5
195	V3	6725	-935.5	245	COMA45	8652	4	295	SEGA0	7505	920.5
196	V3	6790	-935.5	246	COMA44	8652	42	296	SEGB0	7467	920.5
197	V3	6855	-935.5	247	COMA43	8652	80	297	SEGC0	7429	920.5
198	V3	6920	-935.5	248	COMA42	8652	118	298	SEGA1	7391	920.5
199	V3	6985	-935.5	249	COMA41	8652	156	299	SEGB1	7353	920.5
200	V4	7075	-935.5	250	COMA40	8652	194	300	SEGC1	7315	920.5

chip size 17,643 ×2,180 μm2 (chip center = 0:0)

PAD No.	Pad name	X(μm)	Y(μm)	PAD No.	Pad name	X (μm)	Y (μm)	PAD No.	Pad name	X (μm)	Y (μm)
301	SEGA2	7277	920.5	351	SEGC18	5377	920.5	401	SEGB35	3477	920.5
302	SEGB2	7239	920.5	352	SEGA19	5339	920.5	402	SEGC35	3439	920.5
303	SEGC2	7201	920.5	353	SEGB19	5301	920.5	403	SEGA36	3401	920.5
304	SEGA3	7163	920.5	354	SEGC19	5263	920.5	404	SEGB36	3363	920.5
305	SEGB3	7125	920.5	355	SEGA20	5225	920.5	405	SEGC36	3325	920.5
306	SEGC3	7087	920.5	356	SEGB20	5187	920.5	406	SEGA37	3287	920.5
307	SEGA4	7049	920.5	357	SEGC20	5149	920.5	407	SEGB37	3249	920.5
308	SEGB4	7011	920.5	358	SEGA21	5111	920.5	408	SEGC37	3211	920.5
309	SEGC4	6973	920.5	359	SEGB21	5073	920.5	409	SEGA38	3173	920.5
310	SEGA5	6935	920.5	360	SEGC21	5035	920.5	410	SEGB38	3135	920.5
311	SEGB5	6897	920.5	361	SEGA22	4997	920.5	411	SEGC38	3097	920.5
312	SEGC5	6859	920.5	362	SEGB22	4959	920.5	412	SEGA39	3059	920.5
313	SEGA6	6821	920.5	363	SEGC22	4921	920.5	413	SEGB39	3021	920.5
314	SEGB6	6783	920.5	364	SEGA23	4883	920.5	414	SEGC39	2983	920.5
315	SEGC6	6745	920.5	365	SEGB23	4845	920.5	415	SEGA40	2945	920.5
316	SEGA7	6707	920.5	366	SEGC23	4807	920.5	416	SEGB40	2907	920.5
317	SEGB7	6669	920.5	367	SEGA24	4769	920.5	417	SEGC40	2869	920.5
318	SEGC7	6631	920.5	368	SEGB24	4731	920.5	418	SEGA41	2831	920.5
319	SEGA8	6593	920.5	369	SEGC24	4693	920.5	419	SEGB41	2793	920.5
320	SEGB8	6555	920.5	370	SEGA25	4655	920.5	420	SEGC41	2755	920.5
321	SEGC8	6517	920.5	371	SEGB25	4617	920.5	421	SEGA42	2717	920.5
322	SEGA9	6479	920.5	372	SEGC25	4579	920.5	422	SEGB42	2679	920.5
323	SEGB9	6441	920.5	373	SEGA26	4541	920.5	423	SEGC42	2641	920.5
324	SEGC9	6403	920.5	374	SEGB26	4503	920.5	424	SEGA43	2603	920.5
325	SEGA10	6365	920.5	375	SEGC26	4465	920.5	425	SEGB43	2565	920.5
326	SEGB10	6327	920.5	376	SEGA27	4427	920.5	426	SEGC43	2527	920.5
327	SEGC10	6289	920.5	377	SEGB27	4389	920.5	427	SEGA44	2489	920.5
328	SEGA11	6251	920.5	378	SEGC27	4351	920.5	428	SEGB44	2451	920.5
329	SEGB11	6213	920.5	379	SEGA28	4313	920.5	429	SEGC44	2413	920.5
330	SEGC11	6175	920.5	380	SEGB28	4275	920.5	430	SEGA45	2375	920.5
331	SEGA12	6137	920.5	381	SEGC28	4237	920.5	431	SEGB45	2337	920.5
332	SEGB12	6099	920.5	382	SEGA29	4199	920.5	432	SEGC45	2299	920.5
333	SEGC12	6061	920.5	383	SEGB29	4161	920.5	433	SEGA46	2261	920.5
334	SEGA13	6023	920.5	384	SEGC29	4123	920.5	434	SEGB46	2223	920.5
335	SEGB13	5985	920.5	385	SEGA30	4085	920.5	435	SEGC46	2185	920.5
336	SEGC13	5947	920.5	386	SEGB30	4047	920.5	436	SEGA47	2147	920.5
337	SEGA14	5909	920.5	387	SEGC30	4009	920.5	437	SEGB47	2109	920.5
338	SEGB14	5871	920.5	388	SEGA31	3971	920.5	438	SEGC47	2071	920.5
339	SEGC14	5833	920.5	389	SEGB31	3933	920.5	439	SEGA48	2033	920.5
340	SEGA15	5795	920.5	390	SEGC31	3895	920.5	440	SEGB48	1995	920.5
341	SEGB15	5757	920.5	391	SEGA32	3857	920.5	441	SEGC48	1957	920.5
342	SEGC15	5719	920.5	392	SEGB32	3819	920.5	442	SEGA49	1919	920.5
343	SEGA16	5681	920.5	393	SEGC32	3781	920.5	443	SEGB49	1881	920.5
344	SEGB16	5643	920.5	394	SEGA33	3743	920.5	444	SEGC49	1843	920.5
345	SEGC16	5605	920.5	395	SEGB33	3705	920.5	445	SEGA50	1805	920.5
346	SEGA17	5567	920.5	396	SEGC33	3667	920.5	446	SEGB50	1767	920.5
347	SEGB17	5529	920.5	397	SEGA34	3629	920.5	447	SEGC50	1729	920.5
348	SEGC17	5491	920.5	398	SEGB34	3591	920.5	448	SEGA51	1691	920.5
349	SEGA18	5453	920.5	399	SEGC34	3553	920.5	449	SEGB51	1653	920.5
350	SEGB18	5415	920.5	400	SEGA35	3515	920.5	450	SEGC51	1615	920.5

chip size 17,643 ×2,180 μm2 (chip center = 0:0)

PAD No.	Pad name	X(μm)	Y(μm)	PAD No.	Pad name	X (μm)	Y (μm)	PAD No.	Pad name	X (μm)	Y (μm)
451	SEGA52	1577	920.5	501	SEGC68	-323	920.5	551	SEGB85	-2223	920.5
452	SEGB52	1539	920.5	502	SEGA69	-361	920.5	552	SEGC85	-2261	920.5
453	SEGC52	1501	920.5	503	SEGB69	-399	920.5	553	SEGA86	-2299	920.5
454	SEGA53	1463	920.5	504	SEGC69	-437	920.5	554	SEGB86	-2337	920.5
455	SEGB53	1425	920.5	505	SEGA70	-475	920.5	555	SEGC86	-2375	920.5
456	SEGC53	1387	920.5	506	SEGB70	-513	920.5	556	SEGA87	-2413	920.5
457	SEGA54	1349	920.5	507	SEGC70	-551	920.5	557	SEGB87	-2451	920.5
458	SEGB54	1311	920.5	508	SEGA71	-589	920.5	558	SEGC87	-2489	920.5
459	SEGC54	1273	920.5	509	SEGB71	-627	920.5	559	SEGA88	-2527	920.5
460	SEGA55	1235	920.5	510	SEGC71	-665	920.5	560	SEGB88	-2565	920.5
461	SEGB55	1197	920.5	511	SEGA72	-703	920.5	561	SEGC88	-2603	920.5
462	SEGC55	1159	920.5	512	SEGB72	-741	920.5	562	SEGA89	-2641	920.5
463	SEGA56	1121	920.5	513	SEGC72	-779	920.5	563	SEGB89	-2679	920.5
464	SEGB56	1083	920.5	514	SEGA73	-817	920.5	564	SEGC89	-2717	920.5
465	SEGC56	1045	920.5	515	SEGB73	-855	920.5	565	SEGA90	-2755	920.5
466	SEGA57	1007	920.5	516	SEGC73	-893	920.5	566	SEGB90	-2793	920.5
467	SEGB57	969	920.5	517	SEGA74	-931	920.5	567	SEGC90	-2831	920.5
468	SEGC57	931	920.5	518	SEGB74	-969	920.5	568	SEGA91	-2869	920.5
469	SEGA58	893	920.5	519	SEGC74	-1007	920.5	569	SEGB91	-2907	920.5
470	SEGB58	855	920.5	520	SEGA75	-1045	920.5	570	SEGC91	-2945	920.5
471	SEGC58	817	920.5	521	SEGB75	-1083	920.5	571	SEGA92	-2983	920.5
472	SEGA59	779	920.5	522	SEGC75	-1121	920.5	572	SEGB92	-3021	920.5
473	SEGB59	741	920.5	523	SEGA76	-1159	920.5	573	SEGC92	-3059	920.5
474	SEGC59	703	920.5	524	SEGB76	-1197	920.5	574	SEGA93	-3097	920.5
475	SEGA60	665	920.5	525	SEGC76	-1235	920.5	575	SEGB93	-3135	920.5
476	SEGB60	627	920.5	526	SEGA77	-1273	920.5	576	SEGC93	-3173	920.5
477	SEGC60	589	920.5	527	SEGB77	-1311	920.5	577	SEGA94	-3211	920.5
478	SEGA61	551	920.5	528	SEGC77	-1349	920.5	578	SEGB94	-3249	920.5
479	SEGB61	513	920.5	529	SEGA78	-1387	920.5	579	SEGC94	-3287	920.5
480	SEGC61	475	920.5	530	SEGB78	-1425	920.5	580	SEGA95	-3325	920.5
481	SEGA62	437	920.5	531	SEGC78	-1463	920.5	581	SEGB95	-3363	920.5
482	SEGB62	399	920.5	532	SEGA79	-1501	920.5	582	SEGC95	-3401	920.5
483	SEGC62	361	920.5	533	SEGB79	-1539	920.5	583	SEGA96	-3439	920.5
484	SEGA63	323	920.5	534	SEGC79	-1577	920.5	584	SEGB96	-3477	920.5
485	SEGB63	285	920.5	535	SEGA80	-1615	920.5	585	SEGC96	-3515	920.5
486	SEGC63	247	920.5	536	SEGB80	-1653	920.5	586	SEGA97	-3553	920.5
487	SEGA64	209	920.5	537	SEGC80	-1691	920.5	587	SEGB97	-3591	920.5
488	SEGB64	171	920.5	538	SEGA81	-1729	920.5	588	SEGC97	-3629	920.5
489	SEGC64	133	920.5	539	SEGB81	-1767	920.5	589	SEGA98	-3667	920.5
490	SEGA65	95	920.5	540	SEGC81	-1805	920.5	590	SEGB98	-3705	920.5
491	SEGB65	57	920.5	541	SEGA82	-1843	920.5	591	SEGC98	-3743	920.5
492	SEGC65	19	920.5	542	SEGB82	-1881	920.5	592	SEGA99	-3781	920.5
493	SEGA66	-19	920.5	543	SEGC82	-1919	920.5	593	SEGB99	-3819	920.5
494	SEGB66	-57	920.5	544	SEGA83	-1957	920.5	594	SEGC99	-3857	920.5
495	SEGC66	-95	920.5	545	SEGB83	-1995	920.5	595	SEGA100	-3895	920.5
496	SEGA67	-133	920.5	546	SEGC83	-2033	920.5	596	SEGB100	-3933	920.5
497	SEGB67	-171	920.5	547	SEGA84	-2071	920.5	597	SEGC100	-3971	920.5
498	SEGC67	-209	920.5	548	SEGB84	-2109	920.5	598	SEGA101	-4009	920.5
499	SEGA68	-247	920.5	549	SEGC84	-2147	920.5	599	SEGB101	-4047	920.5
500	SEGB68	-285	920.5	550	SEGA85	-2185	920.5	600	SEGC101	-4085	920.5

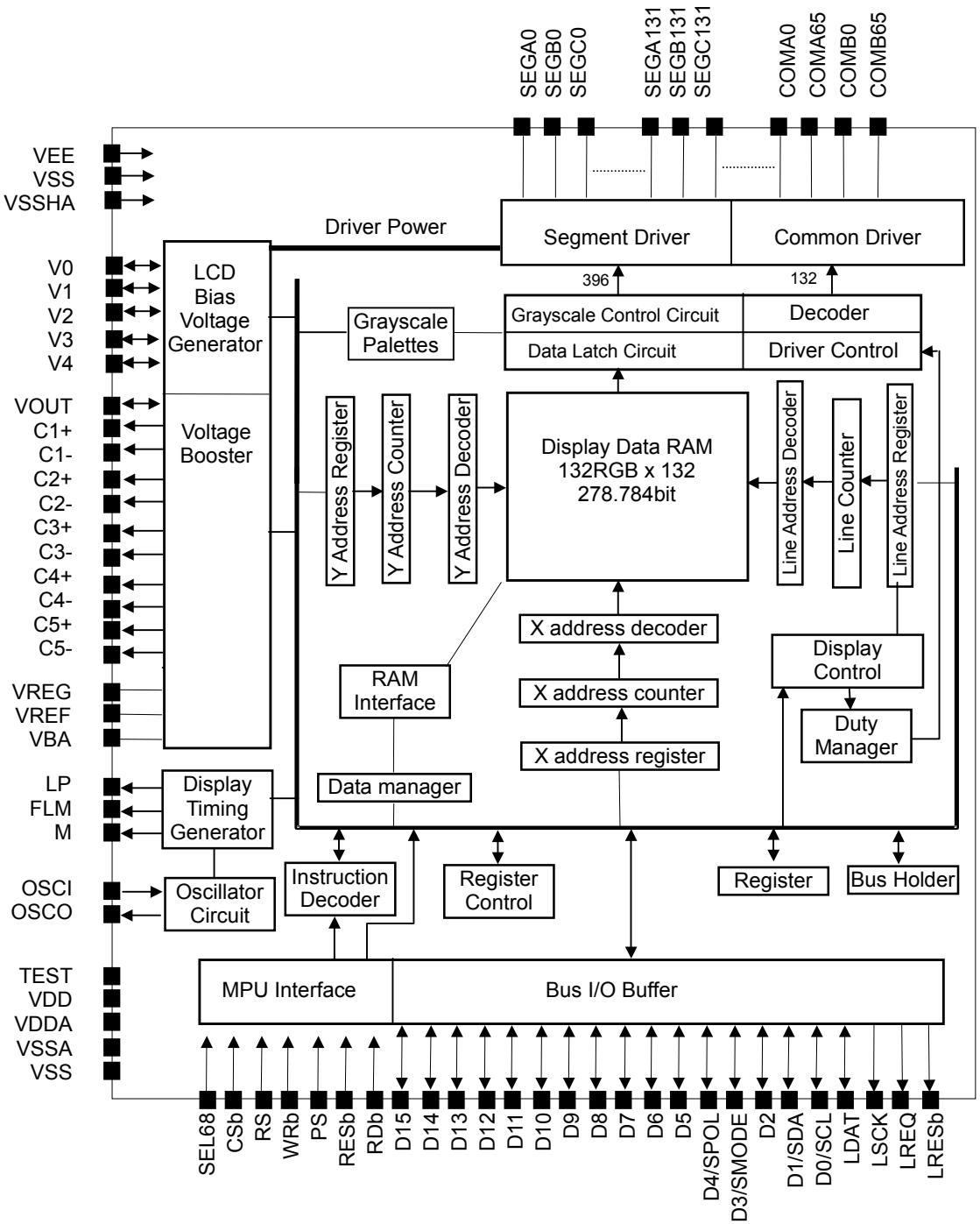
chip size 17,643 ×2,180 μm2 (chip center = 0:0)

PAD No.	Pad name	X(μm)	Y(μm)	PAD No.	Pad name	X (μm)	Y (μm)	PAD No.	Pad name	X (μm)	Y (μm)
601	SEGA102	-4123	920.5	651	SEGC118	-6023	920.5	701	COMB8	-7923	920.5
602	SEGB102	-4161	920.5	652	SEGA119	-6061	920.5	702	COMB9	-7961	920.5
603	SEGC102	-4199	920.5	653	SEGB119	-6099	920.5	703	COMB10	-7999	920.5
604	SEGA103	-4237	920.5	654	SEGC119	-6137	920.5	704	COMB11	-8037	920.5
605	SEGB103	-4275	920.5	655	SEGA120	-6175	920.5	705	COMB12	-8075	920.5
606	SEGC103	-4313	920.5	656	SEGB120	-6213	920.5	706	COMB13	-8113	920.5
607	SEGA104	-4351	920.5	657	SEGC120	-6251	920.5	707	COMB14	-8151	920.5
608	SEGB104	-4389	920.5	658	SEGA121	-6289	920.5	708	COMB15	-8189	920.5
609	SEGC104	-4427	920.5	659	SEGB121	-6327	920.5	709	COMB16	-8227	920.5
610	SEGA105	-4465	920.5	660	SEGC121	-6365	920.5	710	COMB17	-8265	920.5
611	SEGB105	-4503	920.5	661	SEGA122	-6403	920.5	711	COMB18	-8303	920.5
612	SEGC105	-4541	920.5	662	SEGB122	-6441	920.5	712	COMB19	-8341	920.5
613	SEGA106	-4579	920.5	663	SEGC122	-6479	920.5	713	COMB20	-8379	920.5
614	SEGB106	-4617	920.5	664	SEGA123	-6517	920.5	714	COMB21	-8417	920.5
615	SEGC106	-4655	920.5	665	SEGB123	-6555	920.5	715	COMB22	-8455	920.5
616	SEGA107	-4693	920.5	666	SEGC123	-6593	920.5	716	COMB23	-8493	920.5
617	SEGB107	-4731	920.5	667	SEGA124	-6631	920.5	717	COMB24	-8531	920.5
618	SEGC107	-4769	920.5	668	SEGB124	-6669	920.5	718	COMB25	-8569	920.5
619	SEGA108	-4807	920.5	669	SEGC124	-6707	920.5	719	DUMMY	-8607	920.5
620	SEGB108	-4845	920.5	670	SEGA125	-6745	920.5	720	DUMMY	-8652	764
621	SEGC108	-4883	920.5	671	SEGB125	-6783	920.5	721	COMB26	-8652	726
622	SEGA109	-4921	920.5	672	SEGC125	-6821	920.5	722	COMB27	-8652	688
623	SEGB109	-4959	920.5	673	SEGA126	-6859	920.5	723	COMB28	-8652	650
624	SEGC109	-4997	920.5	674	SEGB126	-6897	920.5	724	COMB29	-8652	612
625	SEGA110	-5035	920.5	675	SEGC126	-6935	920.5	725	COMB30	-8652	574
626	SEGB110	-5073	920.5	676	SEGA127	-6973	920.5	726	COMB31	-8652	536
627	SEGC110	-5111	920.5	677	SEGB127	-7011	920.5	727	COMB32	-8652	498
628	SEGA111	-5149	920.5	678	SEGC127	-7049	920.5	728	COMB33	-8652	460
629	SEGB111	-5187	920.5	679	SEGA128	-7087	920.5	729	COMB34	-8652	422
630	SEGC111	-5225	920.5	680	SEGB128	-7125	920.5	730	COMB35	-8652	384
631	SEGA112	-5263	920.5	681	SEGC128	-7163	920.5	731	COMB36	-8652	346
632	SEGB112	-5301	920.5	682	SEGA129	-7201	920.5	732	COMB37	-8652	308
633	SEGC112	-5339	920.5	683	SEGB129	-7239	920.5	733	COMB38	-8652	270
634	SEGA113	-5377	920.5	684	SEGC129	-7277	920.5	734	COMB39	-8652	232
635	SEGB113	-5415	920.5	685	SEGA130	-7315	920.5	735	COMB40	-8652	194
636	SEGC113	-5453	920.5	686	SEGB130	-7353	920.5	736	COMB41	-8652	156
637	SEGA114	-5491	920.5	687	SEGC130	-7391	920.5	737	COMB42	-8652	118
638	SEGB114	-5529	920.5	688	SEGA131	-7429	920.5	738	COMB43	-8652	80
639	SEGC114	-5567	920.5	689	SEGB131	-7467	920.5	739	COMB44	-8652	42
640	SEGA115	-5605	920.5	690	SEGC131	-7505	920.5	740	COMB45	-8652	4
641	SEGB115	-5643	920.5	691	DUMMY	-7543	920.5	741	COMB46	-8652	-34
642	SEGC115	-5681	920.5	692	DUMMY	-7581	920.5	742	COMB47	-8652	-72
643	SEGA116	-5719	920.5	693	COMB0	-7619	920.5	743	COMB48	-8652	-110
644	SEGB116	-5757	920.5	694	COMB1	-7657	920.5	744	COMB49	-8652	-148
645	SEGC116	-5795	920.5	695	COMB2	-7695	920.5	745	COMB50	-8652	-186
646	SEGA117	-5833	920.5	696	COMB3	-7733	920.5	746	COMB51	-8652	-224
647	SEGB117	-5871	920.5	697	COMB4	-7771	920.5	747	COMB52	-8652	-262
648	SEGC117	-5909	920.5	698	COMB5	-7809	920.5	748	COMB53	-8652	-300
649	SEGA118	-5947	920.5	699	COMB6	-7847	920.5	749	COMB54	-8652	-338
650	SEGB118	-5985	920.5	700	COMB7	-7885	920.5	750	COMB55	-8652	-376

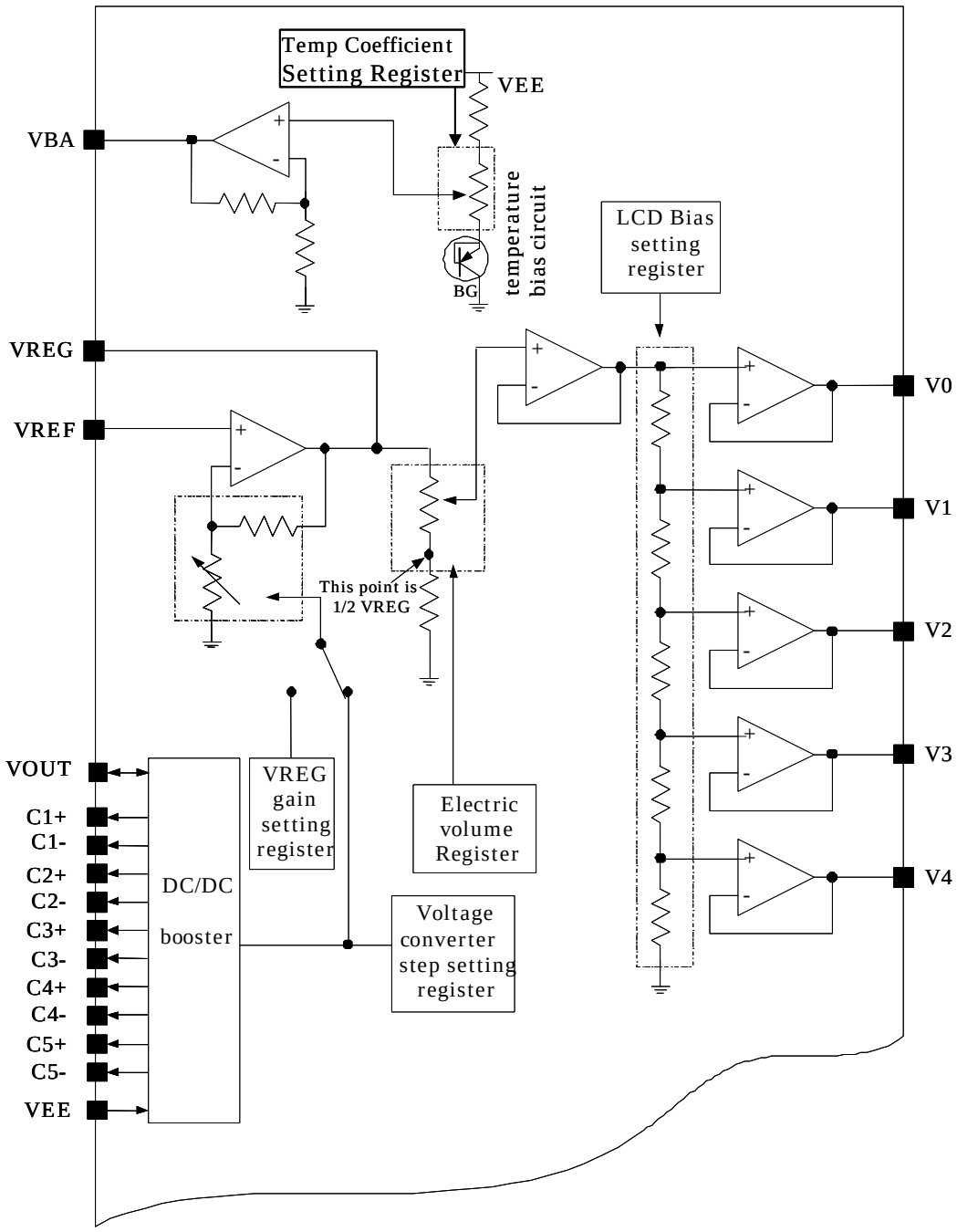
chip size 17,643×2,180 μm2 (chip center = 0:0)

PAD No.	Pad name	X(μm)	Y(μm)	PAD No.	Pad name	X (μm)	Y (μm)	PAD No.	Pad name	X (μm)	Y (μm)
751	COMB56	-8652	-414								
752	COMB57	-8652	-452								
753	COMB58	-8652	-490								
754	COMB59	-8652	-528								
755	COMB60	-8652	-566								
756	COMB61	-8652	-604								
757	COMB62	-8652	-642								
758	COMB63	-8652	-680								
759	COMB64	-8652	-718								
760	COMB65	-8652	-756								
761	DUMMY	-8652	-794								

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



Note) When external V_{REF} is used, keep Reference Voltage Circuit open (VGOFF="0", VBON="0").

■ TERMINAL DESCRIPTION

Power Supply

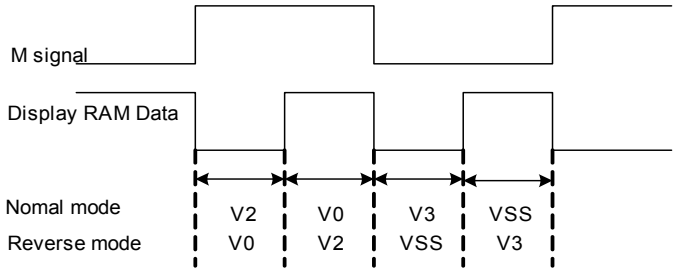
No.	Terminal	I/O	Description
64-69	V_{DD}	Power	Power Supply for Logic Circuits
26,32,42	V_{DDA}	Power	V_{DDA} is internally connected to V_{DD} to fix SEL68 or P/S to "H" if necessary, and cannot be used as main power supply. • V_{DDA} should be open if not used
33,43	V_{SSA}	Power	V_{SSA} is internally connected to V_{SS} to fix SEL68 or P/S to "L" if necessary, and cannot be used as main GND. • V_{SSA} should be open if not used.
57-63	V_{SS}	Power	GND for logic circuits
95-104	V_{SSHA}	Power	GND for voltage converter circuits
206-222	V_{SSH}	Power	GND for voltage booster
176-205	V_0 V_1 V_2 V_3 V_4	Power/O	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V_0-V_4) are activated by the "Power Control" instruction. Stabilizing capacitors are required between each bias voltage and V_{SS}. • When the external LCD power supply is used, LCD bias voltages are externally supplied on V_0, V_1, V_2, V_3 and V_4 individually, with the following relation maintained: $V_{SSH}<V_4<V_3<V_2<V_1<V_0$
116-127	C_{1+} C_{1-}	Power	Capacitor Connection for Voltage Booster
128-139	C_{2+} C_{2-}	Power	Capacitor Connection for Voltage Booster
140-151	C_{3+} C_{3-}	Power	Capacitor Connection for Voltage Booster
152-163	C_{4+} C_{4-}	Power	Capacitor Connection for Voltage Booster
164-175	C_{5+} C_{5-}	Power	Capacitor Connection for Voltage Booster
85-89	V_{BA}	Power	Reference-Voltage Generator Output (typically 1.9V at 25℃, with temperature compensation function)
70-84	V_{EE}	Power	Voltage Booster Input • V_{EE} is normally connected to V_{DD}.
90-94	V_{REF}	Power	Voltage Regulator Input
105-109	V_{REG}	Power	Voltage Regulator Output • Connect this pin to V_{SS} with a stabilizing capacitor
110-115	V_{OUT}	Power	Voltage Booster Output • Connect this pin to V_{SS} with a stabilizing capacitor

MPU Interface

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Description</th></tr>
<tr><td>27</td><td>RESb</td><td>I</td><td>Reset
• Active “L”</td></tr>
<tr><td>34-41</td><td>D0/SCL
D1/SDA
D2
D3/SMODE
D4/SPOL
D5~D7</td><td>I/O</td><td>Parallel Interface
D_7 to D_0: 8-bit Bi-directional Bus(P/S=“H”)

Serial Interface
SDA: Serial Data
SCL: Shift Clock
SMODE: 3-/4-line Serial Mode Select
SPOL: RS Polarity Select (3-line Serial Interface Mode)</td></tr>
<tr><td>44-51</td><td>D8~D15</td><td>I/O</td><td>8-bit Bi-directional Bus
• In the 16-bit bus length mode, D_{15}-D_8 are assigned to upper 8-bit data bus.
• In the serial interface mode or the 8-bit parallel interface mode, D_{15}-D_8 should be fixed to “H” or “L”.</td></tr>
<tr><td>28</td><td>CSb</td><td>I</td><td>Chip Select
• Active “L”</td></tr>
<tr><td>29</td><td>RS</td><td>I</td><td>Register Select
• This signal interprets transferred data as display data or instruction.
<table><tr><th>RS</th><th>H</th><th>L</th></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table></td></tr>
<tr><td>31</td><td>RDb(E)</td><td>I</td><td>80-series MPU Interface (P/S=“H”, SEL68=“L”)
Data Read (RDb) Signal
• Active “L”
68-series MPU Interface (P/S=“H”, SEL68=“H”)
Enable Signal
• Active “H”</td></tr>
<tr><td>30</td><td>WRb
(R/W)</td><td>I</td><td>80-series MPU Interface (P/S=“H”, SEL68=“L”)
Data Write (WRb) Signal
• Active “L”
68-series MPU Interface (P/S=“H”, SEL68=“H”)
Data Read or Write (R/W) Signal
<table><tr><th>R/W</th><th>H</th><th>L</th></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table></td></tr>
<tr><td>24</td><td>SEL68</td><td>I</td><td>MPU Mode Select
<table><tr><th>SEL86</th><th>H</th><th>L</th></tr><tr><td>MPU</td><td>68-series</td><td>80-series</td></tr></table></td></tr>
<tr><td>25</td><td>PS</td><td>I</td><td>Parallel/Serial Interface Mode Select
<table><tr><th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr><tr><td>H</td><td>CSb</td><td>RS</td><td>D_0 ~ D_7</td><td>RDb, WRb</td><td>-</td></tr><tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D_1)</td><td>Write Only</td><td>SCL (D_0)</td></tr></table>In the serial interface mode (P/S=“L”), RDb, WRb, D_2 and D_5-D_{15} should be fixed to “H” or “L”,.</td></tr>
<tr><td>23</td><td>TEST</td><td>I</td><td>Maker test terminal
This terminal must be fixed to “H” in the user’s application.</td></tr>
</table>

LCD Output

<table>
<tr><th>No.</th><th>Terminal</th><th>I/O</th><th>Description</th></tr>
<tr><td>295-690</td><td>$SEGA_0$~
$SEGA_{131}$,
$SEGB_0$~
$SEGB_{131}$,
$SEGC_0$~
$SEGC_{131}$</td><td>O</td><td>Segment Drivers Output
<table>
<tr><th>REV Mode</th><th>Turn-off</th><th>Turn-on</th></tr>
<tr><td>Normal</td><td>0</td><td>1</td></tr>
<tr><td>Reverse</td><td>1</td><td>0</td></tr>
</table>

</td></tr>
<tr><td>54</td><td>FLM</td><td>O</td><td>Normally open.</td></tr>
<tr><td>53</td><td>M</td><td></td><td>Normally open.</td></tr>
<tr><td>52</td><td>LP</td><td>O</td><td>Normally open.</td></tr>
<tr><td>225-292</td><td>$COMA_0$~
$COMA_{65}$
$COMB_0$~
$COMB_{65}$</td><td>O</td><td>Common Divers Output
<table>
<tr><th>Data</th><th>FR</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>V_{SSH}</td></tr>
<tr><td>L</td><td>H</td><td>V_1</td></tr>
<tr><td>H</td><td>L</td><td>V_0</td></tr>
<tr><td>L</td><td>L</td><td>V_4</td></tr>
</table></td></tr>
</table>

Oscillator

56	OSCI	I	When using the internal resistor, connect OSCI to “L” and keep OSCO open
55	OSCO	O	When using an external resistor, connect OSCI and OSCO with the external resistor, and if using external clock, input 50% duty signal into the OSCI.

White LED Driver Ports

19	LDAT	I/O	White LED control port: data input/output
20	LSCK	O	White LED control port: shift clock output
21	LREQ	O	White LED control port: data request output
22	LRESb	O	White LED control port: reset output

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D_7-D_0 (D_{15}-D_0)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) " -" : Fix to "H" or "L".

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D_7-D_0 (D_{15}-D_0)
L	80-series MPU	CSb	RS	RDb	WRb	D_7-D_0 (D_{15}-D_0)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is inactive (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D_7, D_6,…, and D_0, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb="H") temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

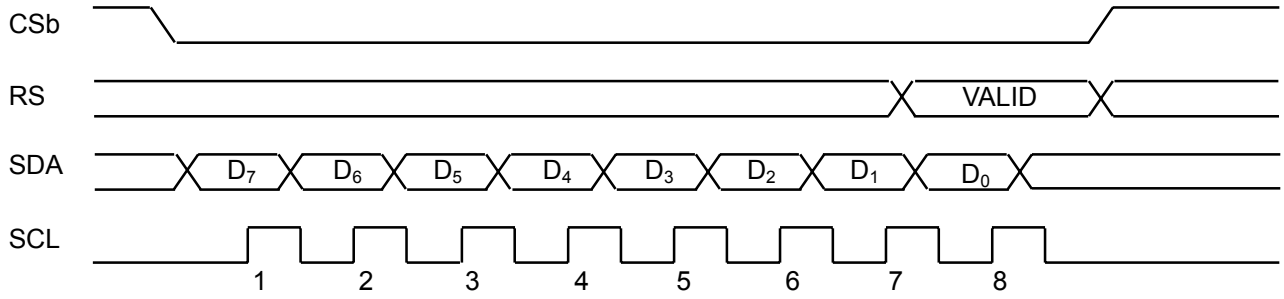


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb="L"), the SDA and SCL are enabled. While the chip select is not active (CSb="H"), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D_7, D_6,…, and D_0, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9^{th} SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to "L" right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb="H") temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

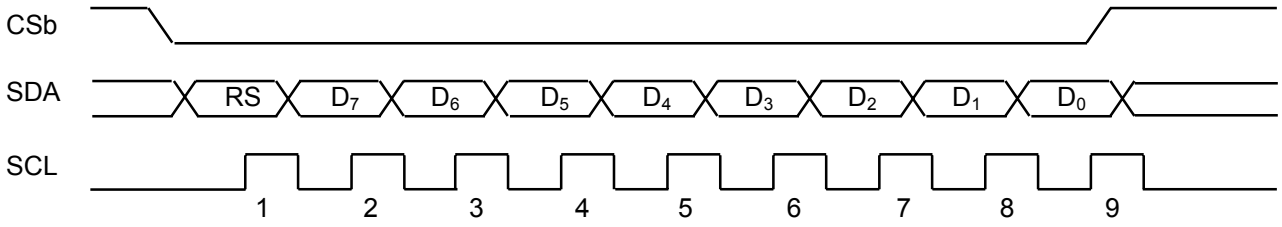


Fig 2 3-line Serial Interface Timing

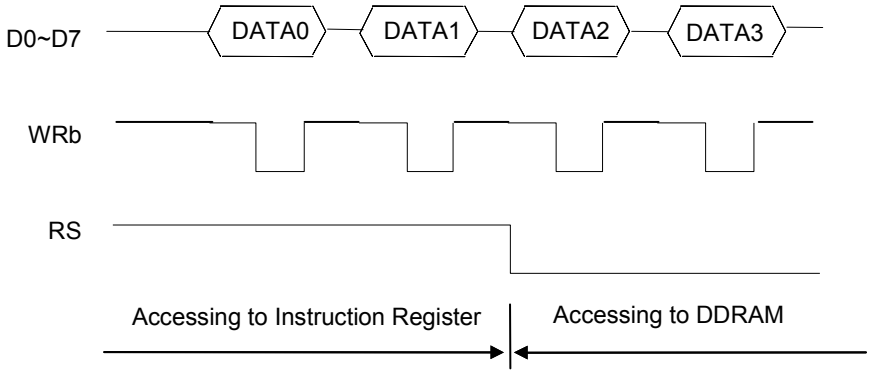
(1-7) Data Write

While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

8-bit access to DDRAM



8-bit access to Instruction Register

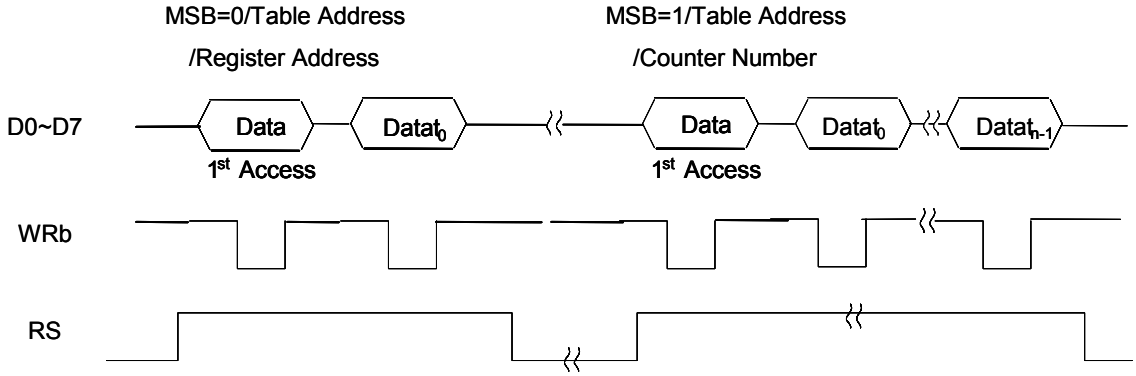
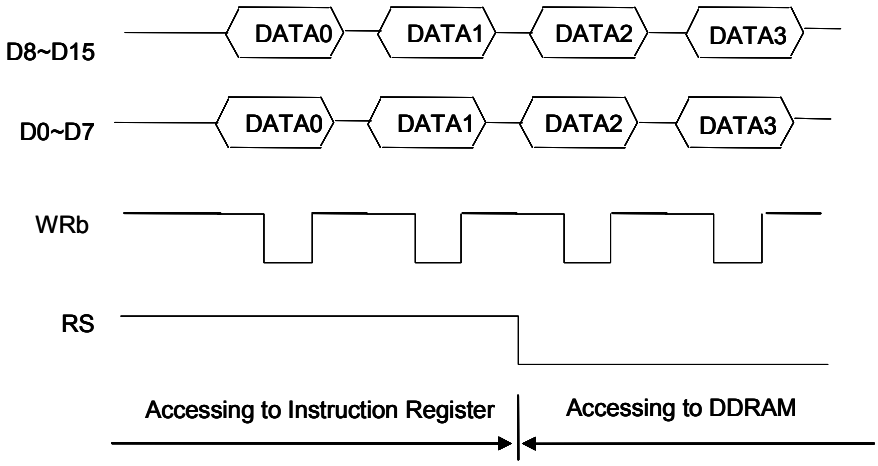


Fig 3 Data Write Operations in 8-bit

16-bit access to DDRAM



16-bit access to Instruction Register

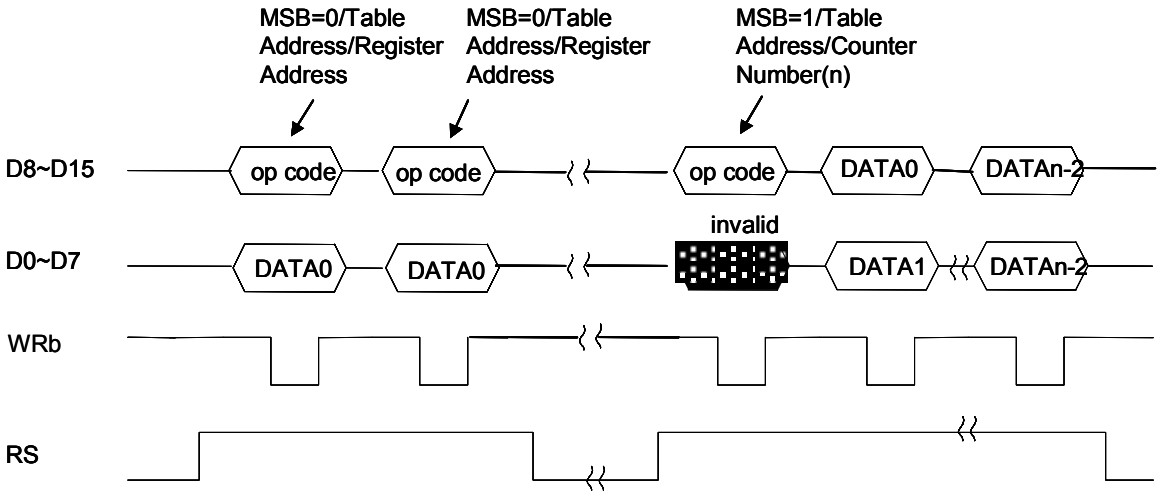
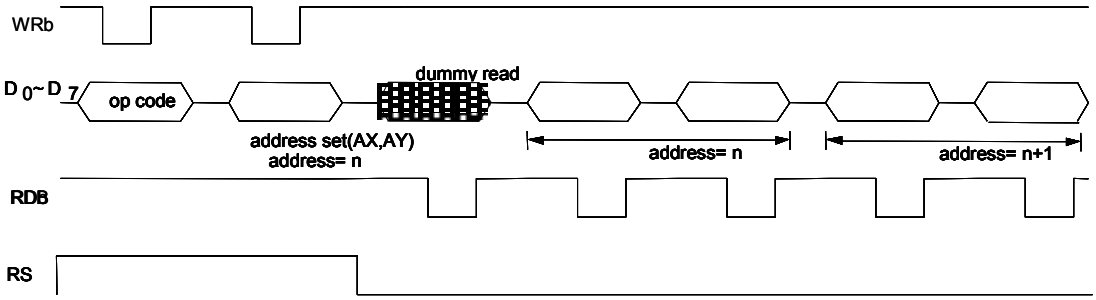


Fig 4 Data Write Operations in 16-bit

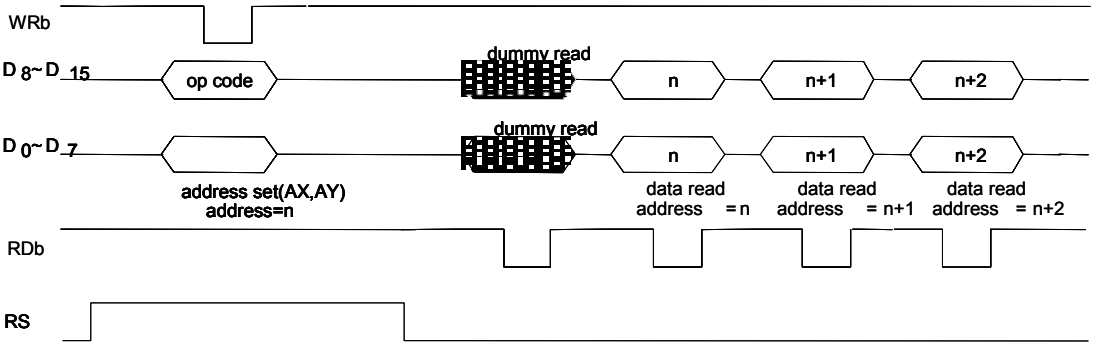
(1-8) Data Read

Just after address setting or data write operation, make sure to conduct dummy read operation once. The reason lies below, data from CPU is temporarily held in the built-in bus holder, and then released to the internal data bus, therefore a dummy data will be read out by the 1st "Display Data Read" instruction, the wanted data will be read out by the 2nd instruction.

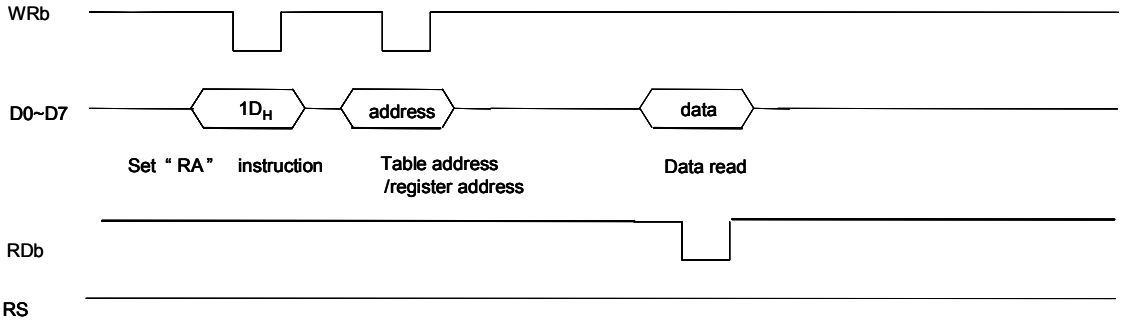
Display Data Read in 8-bit



Display Data Read in 16-bit



Instruction Data Read in 8-bit



Instruction Data Read in 16-bit

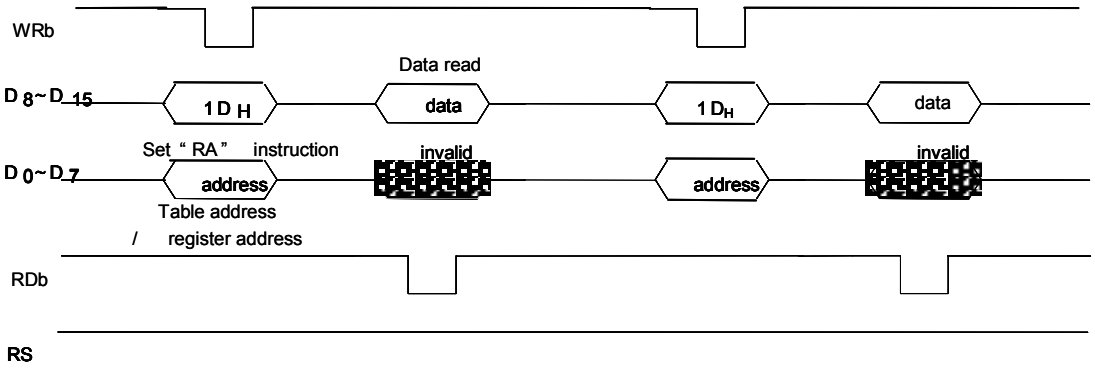


Fig 5 Data Read Operations

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length can be selected by the D_0 (SWIF) bit of the CFG register.

SWIF = "0" : 8-bit bus

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

SWIF = "1" : 16-bit bus

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

Bit assignment is determined by the D_1 (UDS) bit of the CFG register.

16-bit access

UDS = "0"

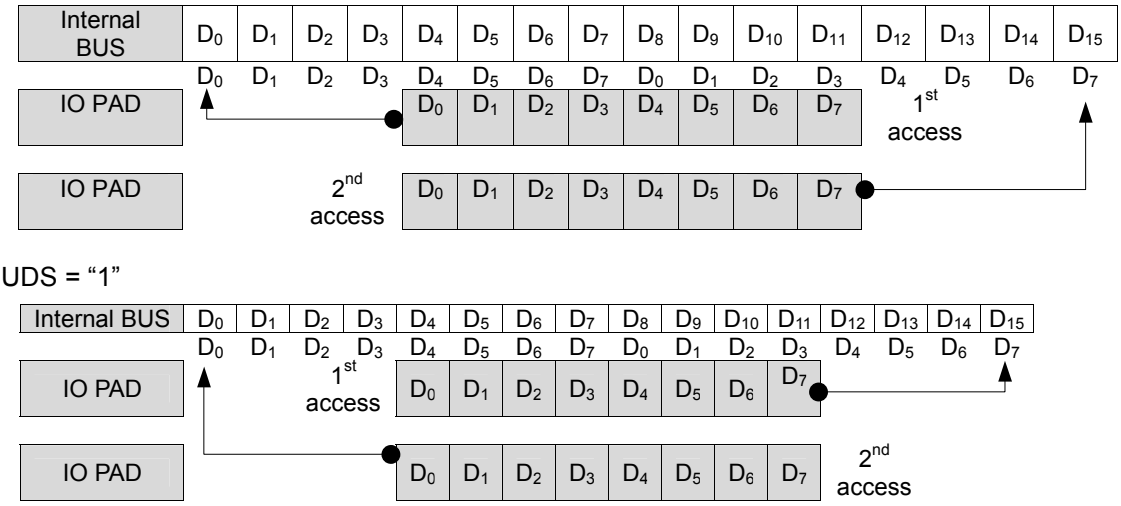
Internal BUS	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
IO PAD	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

UDS = "1"

Internal BUS	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
IO PAD	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}

8-bit access

UDS = "0"



UDS = "1"

During 8-bit access, D15~D8 pins become high impedance, make sure fix them to H" or "L".

(2) INITIAL DISPLAY LINE

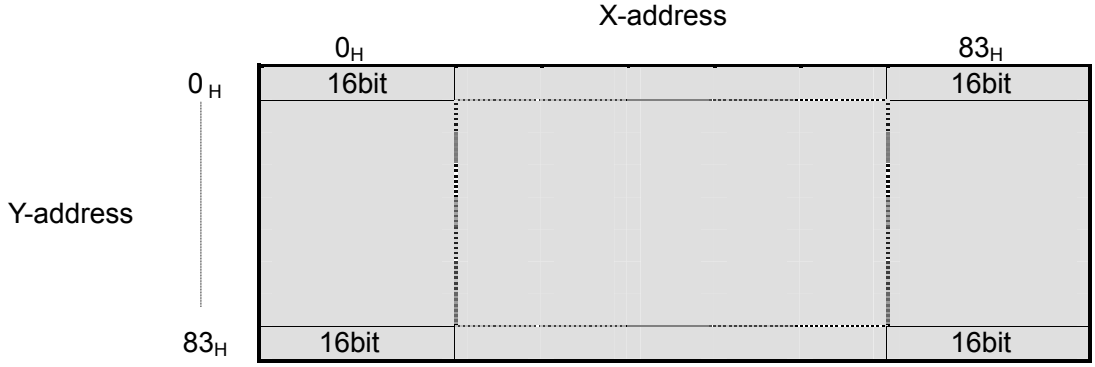
The Initial Display Line register(HST) specifies a DDRAM Y address, and display data corresponding to this address will be displayed by the Scan Start COM 1.

The Y address specified by the Initial Display Line register is preset into the line counter whenever the FLM becomes "H". At the rising edge of the LP signal, the line counter is counted-up, then display data is latched into the data latch circuit. At the falling edge of the LP signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers Ai, Bi and Ci (i=0 to 131) generate LCD waveforms.

(3) DDRAM

(3-1) DDRAM Address Range

The DDRAM is capable of 132 bits for Y address and 2,112 bits (16-bit x 132-segment) for X address. The x and Y address are from 00_H to 83_H. Address setting outside these ranges is not allowed, otherwise it may cause malfunctions. When auto-increment(auto-decrement) function is used during DDRAM access, Y address and/or X address will be automatically increased(decreased). This operation is independent from line counter count-up (count-down).

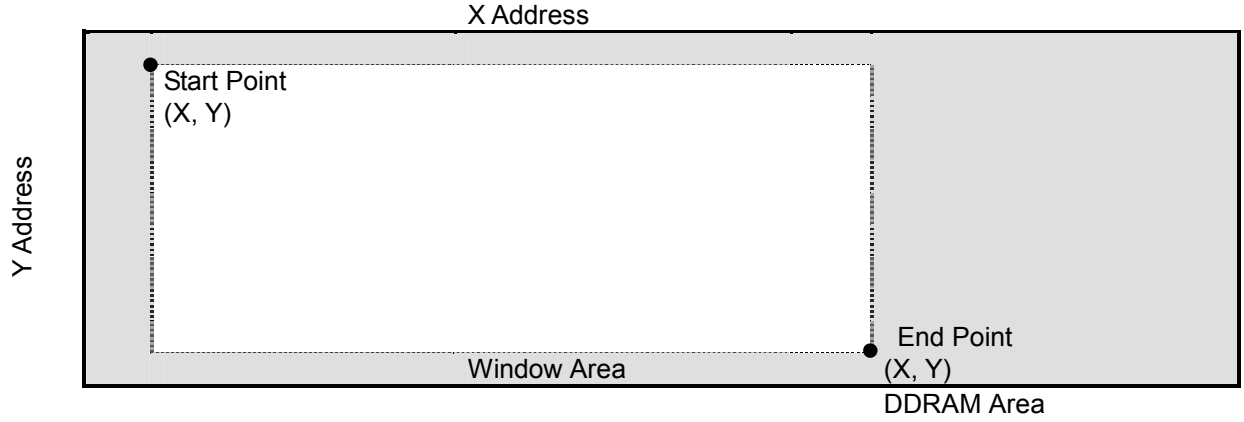


(3-2) Window Area for DDRAM Access

Besides the normal DDRAM access discussed previously, it is possible to access only a specified window area by using CFG, ADRH, ADRL, EADRH and EADRL registers to define a start point and an end point.

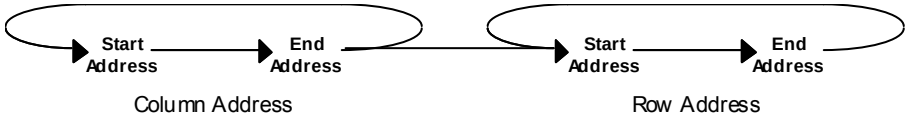
When auto-increment(auto-decrement) function enabled, Y address and/or X address will be automatically increased(decreased) whenever DDRAM is accessed. And, the start point is specified by the X address Register (ADRH) and Y address Register(ADRL), the end point by the Window End X address Register(EADRH) and Window End Y address Register(EADRL). For the details, refer to the Instruction Table. The typical sequence of the window area setting is listed below.

1. Set D_7 (AIM1), D_6 (AIM0), D_5 (VWR), D_4 (IDSY), D_3 (IDSX), and D_2 (WIN) bit of CFG register.
2. Set start point by ADRH and ADRL register.
3. Set end point by EADRH and EADRL register.
4. Window area is set up, and DDRAM can be accessed.



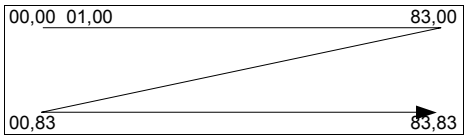
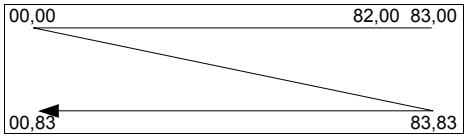
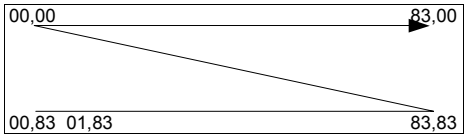
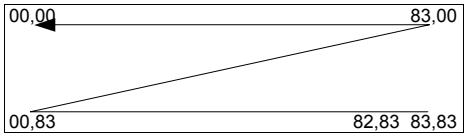
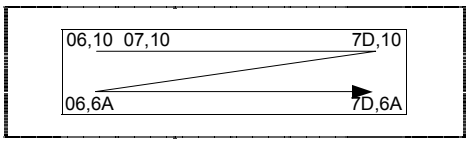
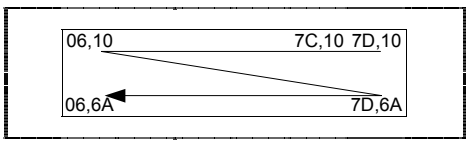
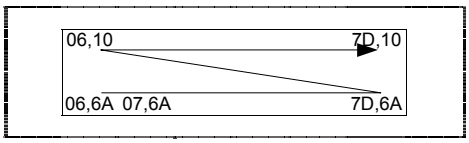
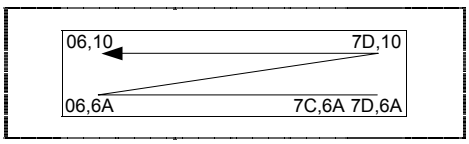
NOTE1) The following relationship should be maintained to avoid malfunctions.
- AX (Window Start X address) < EX (Window End X address) < Maximum X address
- AY (Window Start Y address) < EY (Window End Y address) < Maximum Y address

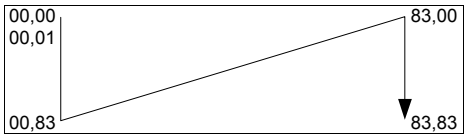
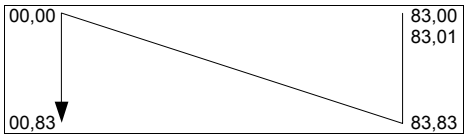
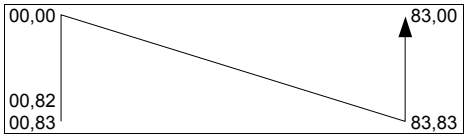
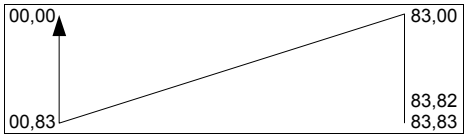
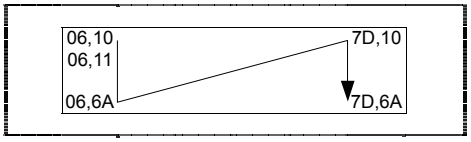
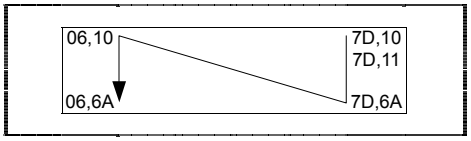
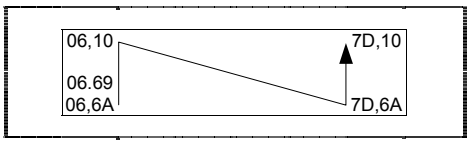
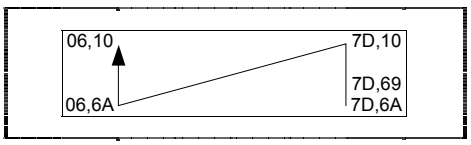
NOTE2) Auto-increment in the window area



NOTE3) When AIM[1:0]=(0,1), read-modify-write operation is valid.

(3-3) DDRAM Access Direction

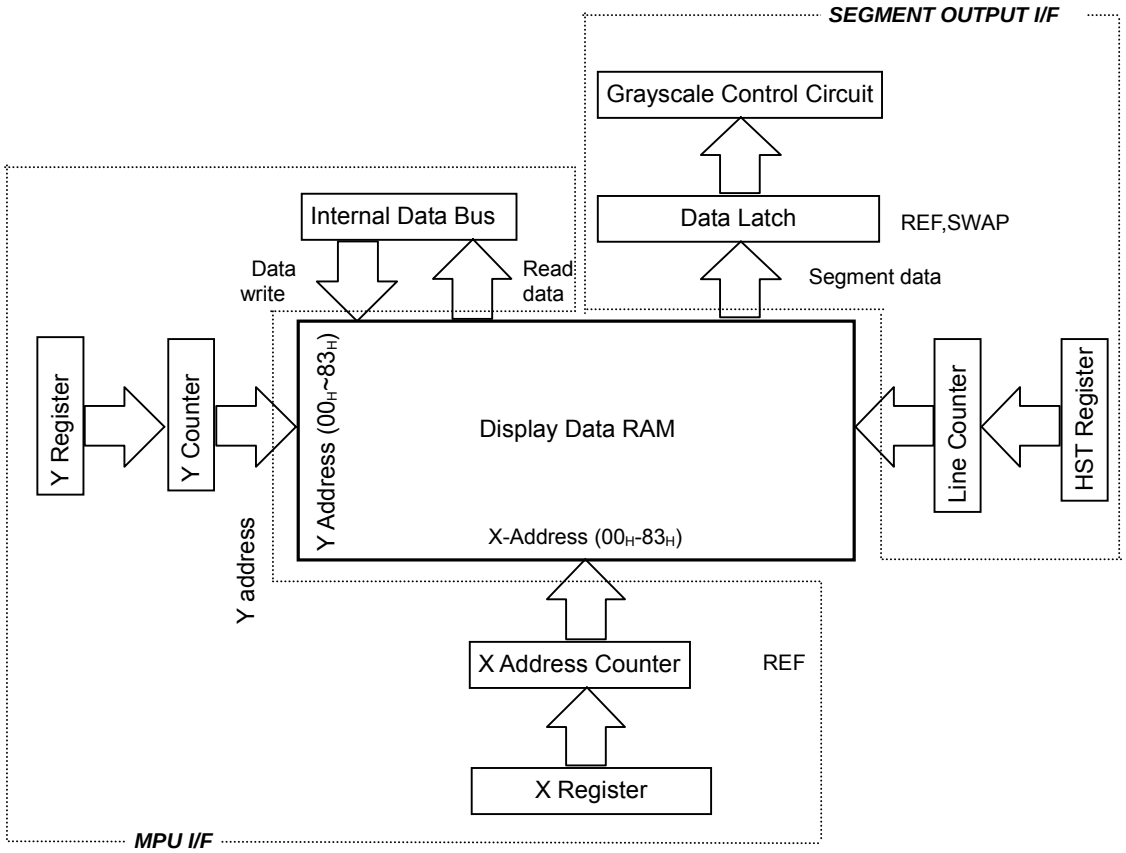
Registers setting									DDDRAM Access Direction	Remark
ADRH	EADRH	ADRL	EADRL	WIN	AIM	IDSX	IDSY	VWR		
00 (H)	X (H)	00 (H)	X (H)	0	00	0	0	0		
83 (H)	X (H)	00 (H)	X (H)	0	00	1	0	0		
00 (H)	X (H)	83 (H)	X (H)	0	00	0	1	0		
83 (H)	X (H)	83 (H)	X (H)	0	00	1	1	0		
06 (H)	7D (H)	10 (H)	6A (H)	1	00	0	0	0		Window Area
7D (H)	06 (H)	10 (H)	6A (H)	1	00	1	0	0		Window Area
06 (H)	7D (H)	6A (H)	10 (H)	1	00	0	1	0		Window Area
7D (H)	06 (H)	6A (H)	10 (H)	1	00	1	1	0		Window Area

Registers setting									DDDRAM Access Direction	Remark
ADRH	EADRH	ADRL	EADRL	WIN	AIM	IDSX	IDSY	VWR		
00 (H)	X (H)	00 (H)	X (H)	0	00	0	0	1		
83 (H)	X (H)	00 (H)	X (H)	0	00	1	0	1		
00 (H)	X (H)	83 (H)	X (H)	0	00	0	1	1		
83 (H)	X (H)	83 (H)	X (H)	0	00	1	1	1		
06 (H)	7D (H)	10 (H)	6A (H)	1	00	0	0	1		Window Area
7D (H)	06 (H)	10 (H)	6A (H)	1	00	1	0	1		Window Area
06 (H)	7D (H)	6A (H)	10 (H)	1	00	0	1	1		Window Area
7D (H)	06 (H)	6A (H)	10 (H)	1	00	1	1	1		Window Area

(3-4) Segment Shift Direction

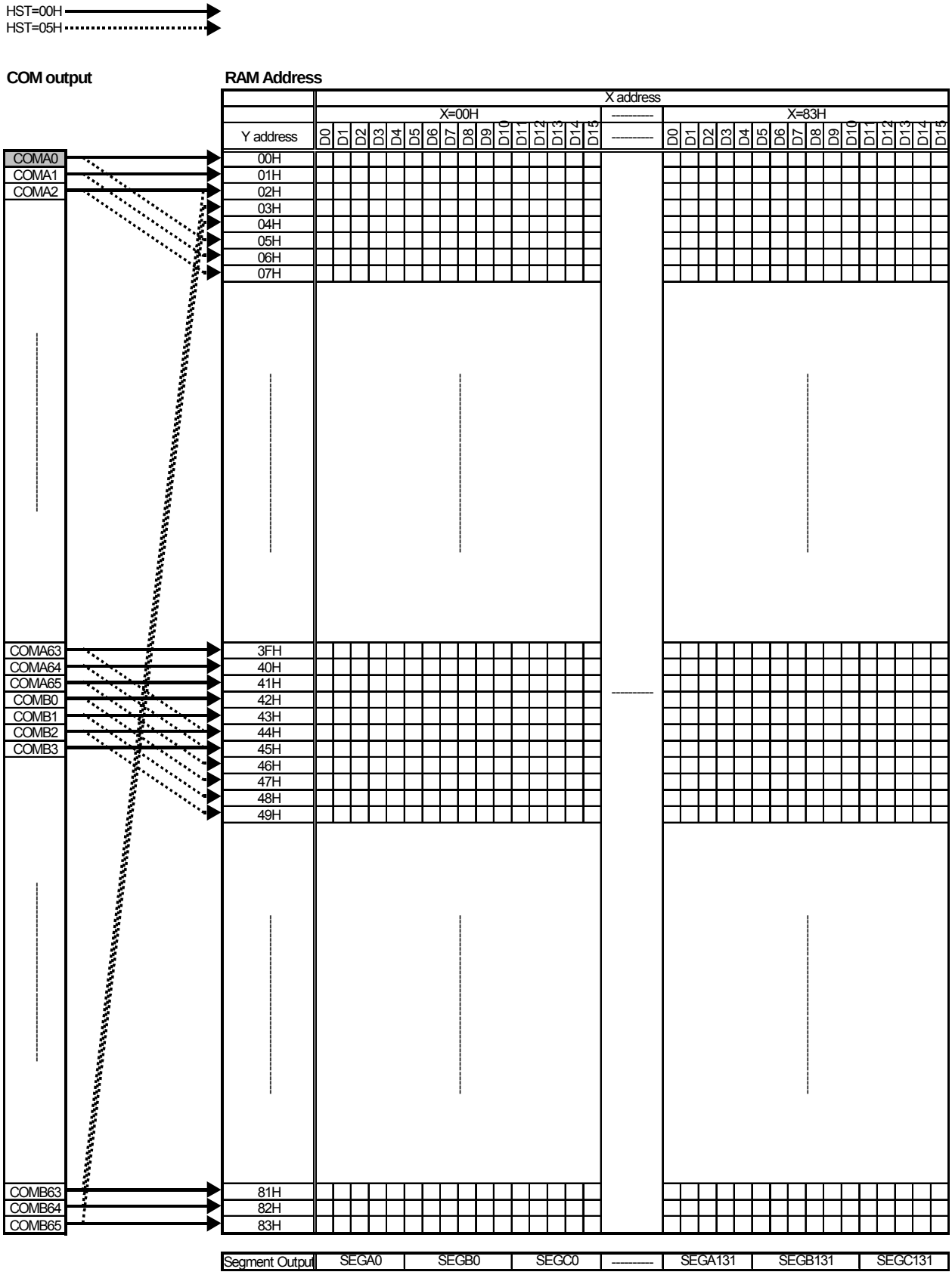
The DDRAM access direction can be selected through setting the D_7(REF) bit of the Display Control register (DISPLAY), This function enables to reverse segment shift direction to reduce the restriction on the IC location on an LCD module.

(3-5) Block Diagram of DDRAM and Peripheral Circuit

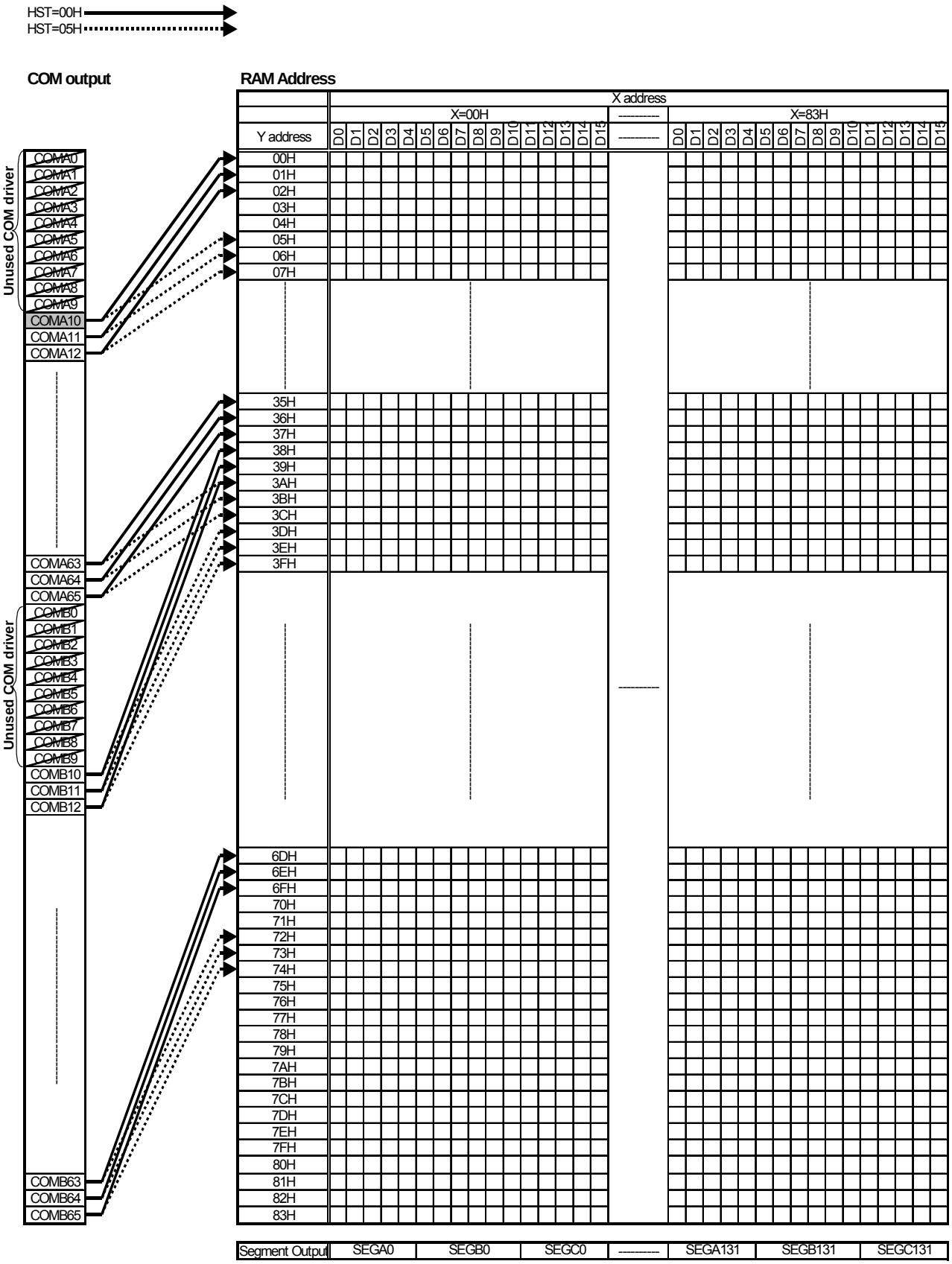


(3-6) DDRAM Mapping

(3-6-1) (REW, SWAP) = (0,0), SHIFT1 = “0”, SHIFT0 = “0”, VPC = "84H“ (1/132 Duty), FVC = "00H", HCT = “00H”, SSC1 and SSC2 = “0”, EN3PTL = “0”



(3-6-2) (REW, SWAP) = (0,0), SHIFT1 = “0”, SHIFT0 = “0”, VPC = "70H“ (1/112 Duty), FVC = "00H", HCT = “0AH”, SSC1 and SSC2 = “0”, EN3PTL = “0”



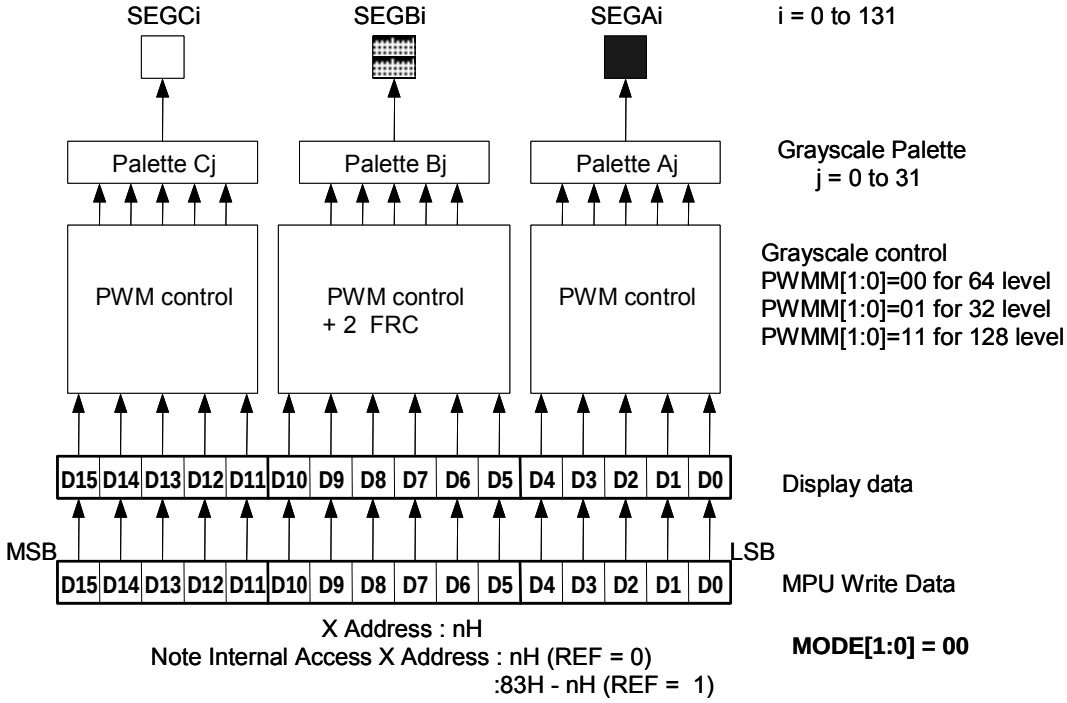
(3-7) The Relationship among Bit Assignment, X address and Segment Driver

Three sub pixels(R, G, B) individually driven by 3 segment drivers (SEGAi, SEGBi, SEGCi) consist one pixel of the color STN panel. In the 65k display mode, 5-bit display data for SEGAi and SEGCi can output 32-level grayscale respectively, and 6-bit display data for SEGBi can output 64-level grayscale, so the total quantity of possible colors is 65,536(32x32x64). In 4k-color mode, 4-bit display data for every SEGAi, SEGBi and SEGCi, so the total quantity of possible colors is 4,096(16x16x16).

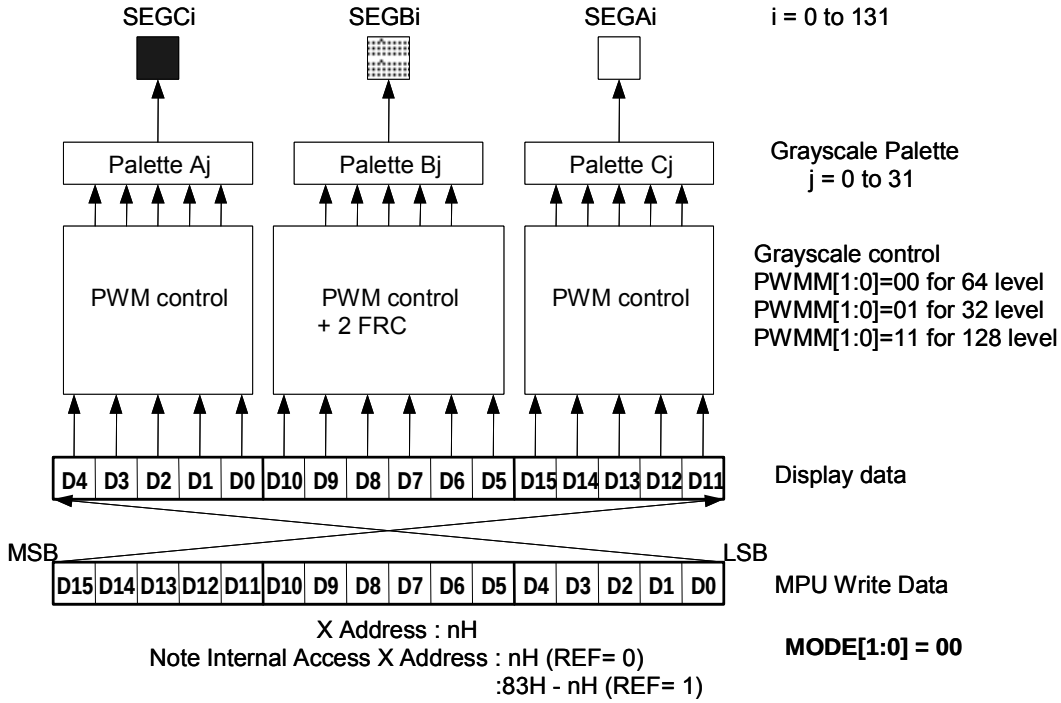
Weighting value of display data is dependent on the status of the SWAP bit and the REF bit of DISPLAY register.

16-bit Bus Access (65k-color Mode)

(REF,SWAP)=(0,0) or (1,1)
MODED = 0 (65,536 color display)

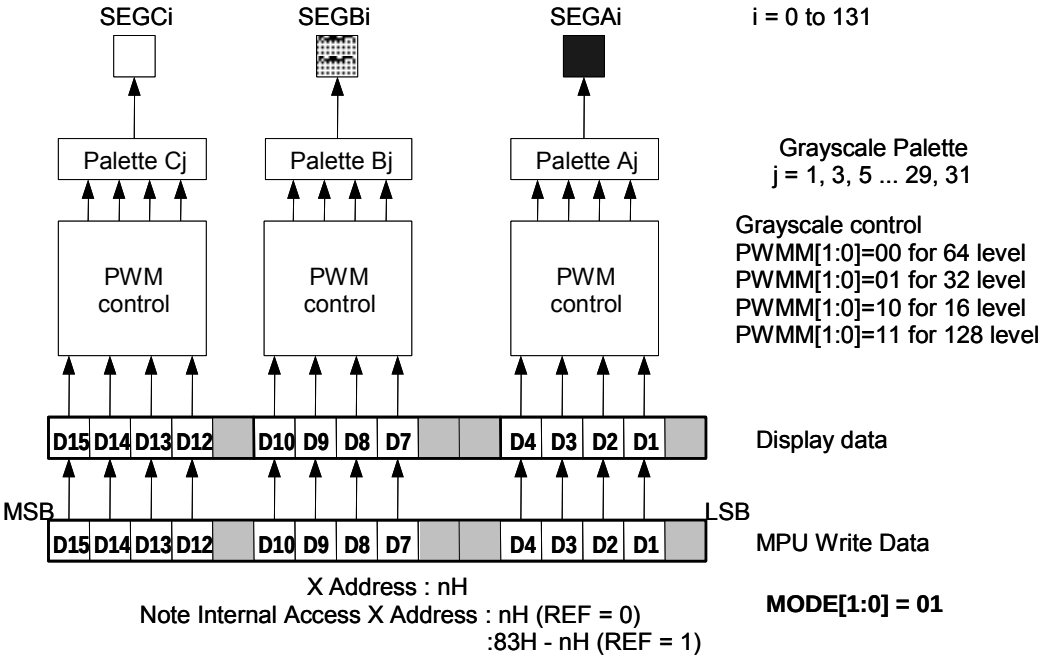


(REF,SWAP)=(0,1) or (1,0)
MODED = 0 (65,536 color display)

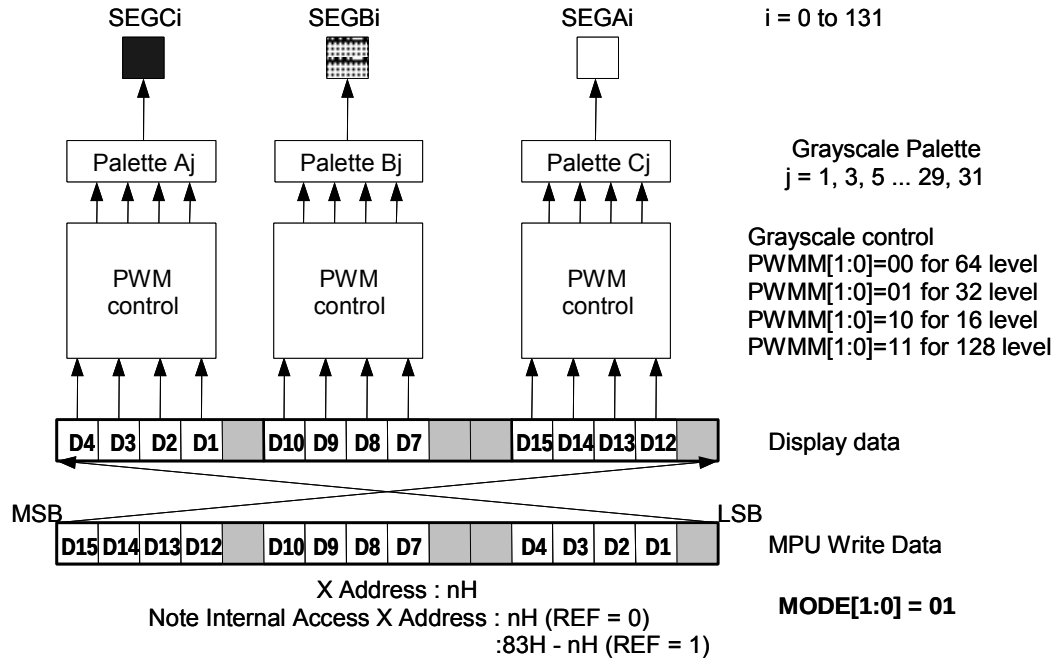


16-bit Bus Access (4k-color Mode 1)

(REF,SWAP)=(0,0) or (1,1)
MODED = 1 (4,096 color display)

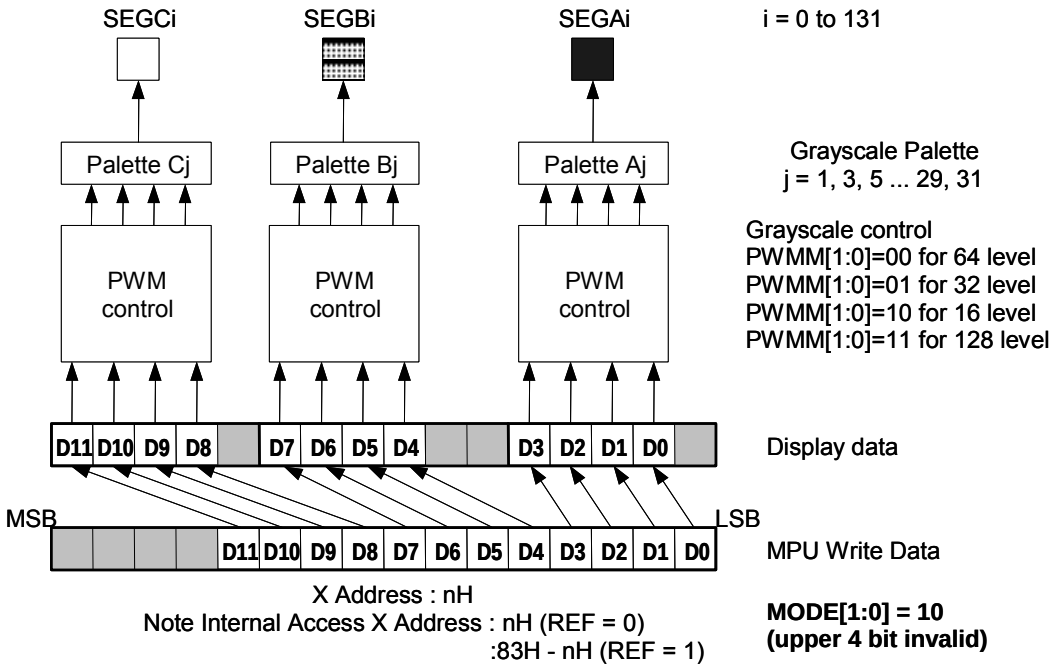


(REF,SWAP)=(0,1) or (1,0)
MODED = 1 (4,096 color display)

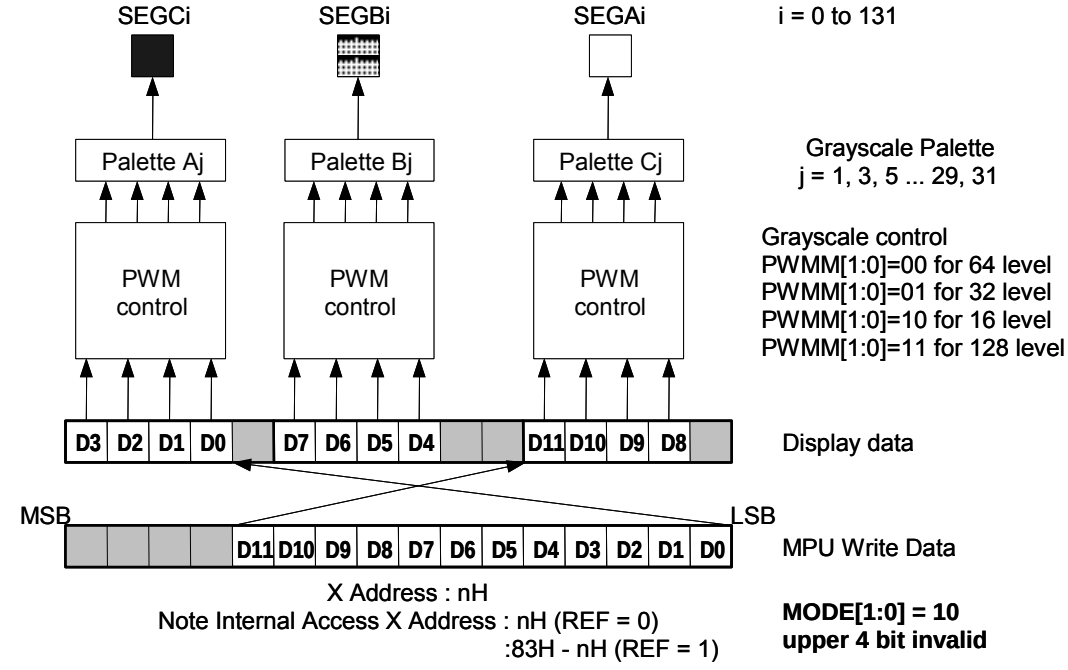


16-bit Bus Access (4k-color Mode 2)

(REF,SWAP)=(0,0) or (1,1)
MODED = 1 (4,096 color display)



(REF,SWAP)=(0,1) or (1,0)
MODED = 1 (4,096 color display)



Relationship among Display Data, X address and Segment Drivers(16-bit Access Mode)

65k-color mode, MODE[1:0]=0_H

REF	SWAP	IDSX 0	IDSX 1	X Address / Display Data / Grayscale Palette / Segment Driver		
0	0	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	$X = 00_H$	··	$X = 83_H$
1	1	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	$X = 83_H$	··	$X = 00_H$
UDS 0		D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15			··	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
UDS 1		D8 D9 D10 D11 D12 D13 D14 D15 D0 D1 D2 D3 D4 D5 D6 D7			··	D8 D9 D10 D11 D12 D13 D14 D15 D0 D1 D2 D3 D4 D5 D6 D7
		Palette A	Palette B	Palette C	··	Palette A	Palette B	Palette C
		SEGA0	SEGB0	SEGC0	··	SEGA131	SEGB131	SEGC131

REF	SWAP	IDSX 0	IDSX 1	X Address / Display Data / Grayscale Palette / Segment Driver		
0	1	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	$X = 00_H$	··	$X = 83_H$
1	0	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	$X = 83_H$	··	$X = 00_H$
UDS 0		D11 D12 D13 D14 D15 D5 D6 D7 D8 D9 D10 D0 D1 D2 D3 D4			··	D11 D12 D13 D14 D15 D5 D6 D7 D8 D9 D10 D0 D1 D2 D3 D4
UDS 1		D3 D4 D5 D6 D7 D13 D14 D15 D0 D1 D2 D8 D9 D10 D11 D12			··	D3 D4 D5 D6 D7 D13 D14 D15 D0 D1 D2 D8 D9 D10 D11 D12
		Palette C	Palette B	Palette A	··	Palette C	Palette B	Palette A
		SEGA0	SEGB0	SEGC0	··	SEGA131	SEGB131	SEGC131

4k-color mode 1, MODE[1:0]=1_H

REF	SWAP	IDSX 0	IDSX 1	X Address / Display Data / Grayscale Palette / Segment Driver		
0	0	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	$X = 00_H$	··	$X = 83_H$
1	1	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	$X = 83_H$	··	$X = 00_H$
UDS 0		D1 D2 D3 D4 D7 D8 D9 D10 D12 D13 D14 D15			··	D1 D2 D3 D4 D7 D8 D9 D10 D12 D13 D14 D15
UDS 1		D9 D10 D11 D12 D15 D0 D1 D2 D4 D5 D6 D7			··	D9 D10 D11 D12 D15 D0 D1 D2 D4 D5 D6 D7
		Palette A	Palette B	Palette C	··	Palette A	Palette B	Palette C
		SEGA0	SEGB0	SEGC0	··	SEGA131	SEGB131	SEGC131

REF	SWAP	IDSX 0	IDSX 1	X Address / Display Data / Grayscale Palette / Segment Driver		
0	1	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	$X = 00_H$	··	$X = 83_H$
1	0	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	$X = 83_H$	··	$X = 00_H$
UDS 0		D12 D13 D14 D15 D7 D8 D9 D10 D1 D2 D3 D4			··	D12 D13 D14 D15 D7 D8 D9 D10 D1 D2 D3 D4
UDS 1		D4 D5 D6 D7 D15 D0 D1 D2 D9 D10 D11 D12			··	D4 D5 D6 D7 D15 D0 D1 D2 D9 D10 D11 D12
		Palette C	Palette B	Palette A	··	Palette C	Palette B	Palette A
		SEGA0	SEGB0	SEGC0	··	SEGA131	SEGB131	SEGC131

4k-color mode, MODE[1:0]=2_H

	REF	SWAP	IDSX 0	IDSX 1	X Address / Display Data / Grayscale Palette / Segment Driver																											
	0	0	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H												··	X = 83_H															
	1	1	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H												··	X = 00_H															
UDS	0				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	··	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11				
	1				D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	··	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3				
					Palette A				Palette B				Palette C				··	Palette A				Palette B				Palette C							
					SEGA0				SEGB0				SEGC0				··	SEGA131				SEGB131				SEGC131							

	REF	SWAP	IDSX 0	IDSX 1	X Address / Display Data / Grayscale Palette / Segment Driver																											
	0	1	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H												··	X = 83_H															
	1	0	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H												··	X = 00_H															
UDS	0				D8	D9	D10	D11	D4	D5	D6	D7	D0	D1	D2	D3	··	D8	D9	D10	D11	D4	D5	D6	D7	D0	D1	D2	D3				
	1				D0	D1	D2	D3	D12	D13	D14	D15	D8	D9	D10	D11	··	D0	D1	D2	D3	D12	D13	D14	D15	D8	D9	D10	D11				
					Palette C				Palette B				Palette A				··	Palette C				Palette B				Palette A							
					SEGA0				SEGB0				SEGC0				··	SEGA131				SEGB131				SEGC131							

Relationship among Display Data, X address and Segment Drivers(8-bit Access Mode)

1st write in data	D01	D11	D21	D31	D41	D51	D61	D71
2nd write in data	D02	D12	D22	D32	D42	D52	D62	D72

65k-color mode, MODE[1:0]=0_H

REF	SWAF	IDSX		X Address / Display Data / Grayscale Palette / Segment Driver																																
		0	1																																	
0	0	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H																..	X = 83_H															
1	1	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H																..	X = 00_H															
UDS		0		D01	D11	D21	D31	D41	D51	D61	D71	D02	D12	D22	D32	D42	D52	D62	D72	..	D01	D11	D21	D31	D41	D51	D61	D71	D02	D12	D22	D32	D42	D52	D62	D72
UDS		1		D02	D12	D22	D32	D42	D52	D62	D72	D01	D11	D21	D31	D41	D51	D61	D71	..	D02	D12	D22	D32	D42	D52	D62	D72	D01	D11	D21	D31	D41	D51	D61	D71
				Palette A					Palette B						Palette C					..	Palette A					Palette B						Palette C				
				SEGA0					SEGB0						SEGC0					..	SEGA131					SEGB131						SEGC131				

REF	SWAF	IDSX		X Address / Display Data / Grayscale Palette / Segment Driver																																
		0	1																																	
0	1	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H																..	X = 83_H															
1	0	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H																..	X = 00_H															
UDS		0		D32	D42	D52	D62	D72	D51	D61	D71	D02	D12	D22	D01	D11	D21	D31	D41	..	D32	D42	D52	D62	D72	D51	D61	D71	D02	D12	D22	D01	D11	D21	D31	D41
UDS		1		D31	D41	D51	D61	D71	D52	D62	D72	D01	D11	D21	D02	D12	D22	D32	D42	..	D31	D41	D51	D61	D71	D52	D62	D72	D01	D11	D21	D02	D12	D22	D32	D42
				Palette C					Palette B						Palette A					..	Palette C					Palette B						Palette A				
				SEGA0					SEGB0						SEGC0					..	SEGA131					SEGB131						SEGC131				

4k-color mode, MODE[1:0]=1_H

REF	SWAF	IDSX		X Address / Display Data / Grayscale Palette / Segment Driver																								
		0	1																									
0	0	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H												..	X = 83_H											
1	1	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H												..	X = 00_H											
UDS		0		D11	D21	D31	D41	D71	D02	D12	D22	D42	D52	D62	D72	..	D11	D21	D31	D41	D71	D02	D12	D22	D42	D52	D62	D72
UDS		1		D12	D22	D32	D42	D72	D01	D11	D21	D41	D51	D61	D71	..	D12	D22	D32	D42	D72	D01	D11	D21	D41	D51	D61	D71
				Palette A				Palette B				Palette C				..	Palette A				Palette B				Palette C			
				SEGA0				SEGB0				SEGC0				..	SEGA131				SEGB131				SEGC131			

REF	SWAF	IDSX		X Address / Display Data / Grayscale Palette / Segment Driver																								
		0	1																									
0	1	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H												..	X = 83_H											
1	0	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H												..	X = 00_H											
UDS		0		D42	D52	D62	D72	D71	D02	D12	D22	D11	D21	D31	D41	..	D42	D52	D62	D72	D71	D02	D12	D22	D11	D21	D31	D41
UDS		1		D41	D51	D61	D71	D72	D01	D11	D21	D12	D22	D32	D42	..	D41	D51	D61	D71	D72	D01	D11	D21	D12	D22	D32	D42
				Palette C				Palette B				Palette A				..	Palette C				Palette B				Palette A			
				SEGA0				SEGB0				SEGC0				..	SEGA131				SEGB131				SEGC131			

4k-color mode, MODE[1:0]=2_H

REF	SWAP	IDSX		X Address / Display Data / Grayscale Palette / Segment Driver																								
		0	1																									
0	0	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H												··	X = 83_H											
1	1	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H												··	X = 00_H											
UDS	0			D01	D11	D21	D31	D41	D51	D61	D71	D02	D12	D22	D32	··	D01	D11	D21	D31	D41	D51	D61	D71	D02	D12	D22	D32
UDS	1			D02	D12	D22	D32	D42	D52	D62	D72	D01	D11	D21	D31	··	D02	D12	D22	D32	D42	D52	D62	D72	D01	D11	D21	D31
				Palette A				Palette B				Palette C				··	Palette A				Palette B				Palette C			
				SEGA0				SEGB0				SEGC0				··	SEGA131				SEGB131				SEGC131			

REF	SWAP	IDSX		X Address / Display Data / Grayscale Palette / Segment Driver																								
		0	1																									
0	1	$00_H \rightarrow 83_H$	$00_H \leftarrow 83_H$	X = 00_H												··	X = 83_H											
1	0	$83_H \leftarrow 00_H$	$83_H \rightarrow 00_H$	X = 83_H												··	X = 00_H											
UDS	0			D02	D12	D22	D32	D41	D51	D61	D71	D01	D11	D21	D31	··	D02	D12	D22	D32	D41	D51	D61	D71	D01	D11	D21	D31
UDS	1			D01	D11	D21	D31	D42	D52	D62	D72	D02	D12	D22	D32	··	D01	D11	D21	D31	D42	D52	D62	D72	D02	D12	D22	D32
				Palette C				Palette B				Palette A				··	Palette C				Palette B				Palette A			
				SEGA0				SEGB0				SEGC0				··	SEGA131				SEGB131				SEGC131			

(4) PWM CONTROL

There are three variable grayscale modes and one fixed grayscale mode for NJU6854.

In the 65k variable grayscale mode ((PWMM1,PWMM0)=(1,1)), every Aj, Bj and Cj(j=0-31) grayscale palette can select one of 32 PWM values from 128 levels(0/127~127/127).

In the 4k mode, every Aj, Bj and Cj(j=0-31) grayscale palette can select one of 16 PWM values from 128 levels (0/127~127/127).

Table 8 PWM and Grayscale mode

PWMM1	PWMM0	Grayscale Mode	Grayscale Display Mode
0	0	Variable	32 options from 64 levels（65k-color mode）, or 16 options（4k-color mode）
0	1	Variable	32 options from 32 levels（65k-color mode）, or 16 options（4k-color mode）
1	0	Fixed	16 options from 16 levels（4k-color mode）
1	1	Variable	32 options from 128 levels（65k-color mode）, or 16 options（4k-color mode）

(5) FRAME RATE CONTROL(FRC)

FRC (Frame Rate control) is the method which averages PWM value (grayscale level) by changing this value by the frame. The FRC is used for the SEGBi (palette Bj) in combination with PWM control in the 65K mode, so that the SEGBi can generate 64 grayscales (32 grayscales x 2) by total 6 bits data (5-bit PWM data and 1-bit FRC data).

(6) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the LP (Latch Pulse), M (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency.

The LP is used for the line counter and the data latch circuit. At the rising edge of the LP signal, the line counter is counted up, then display data is latched into the data latch circuit. At the falling edge of the LP signal, the latch data is released to the grayscale control circuit, then segment drivers Ai, Bi and Ci (i=0~131) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent of external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The M toggles once every frame in the default status, and can be programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes "H".

(7) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the LP. The "Display ON/OFF" and "Reverse Display ON/OFF" instructions control the data in this circuit, but does not change the data in the DDRAM.

(8) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 132-common drivers and 396-segment drivers. The common drivers generate LCD driving waveforms formed on the V_0, V_1, V_4 and V_{SSH} levels. The segment drivers generate waveforms formed on the V_0, V_2, V_3 and V_{SSH} levels.

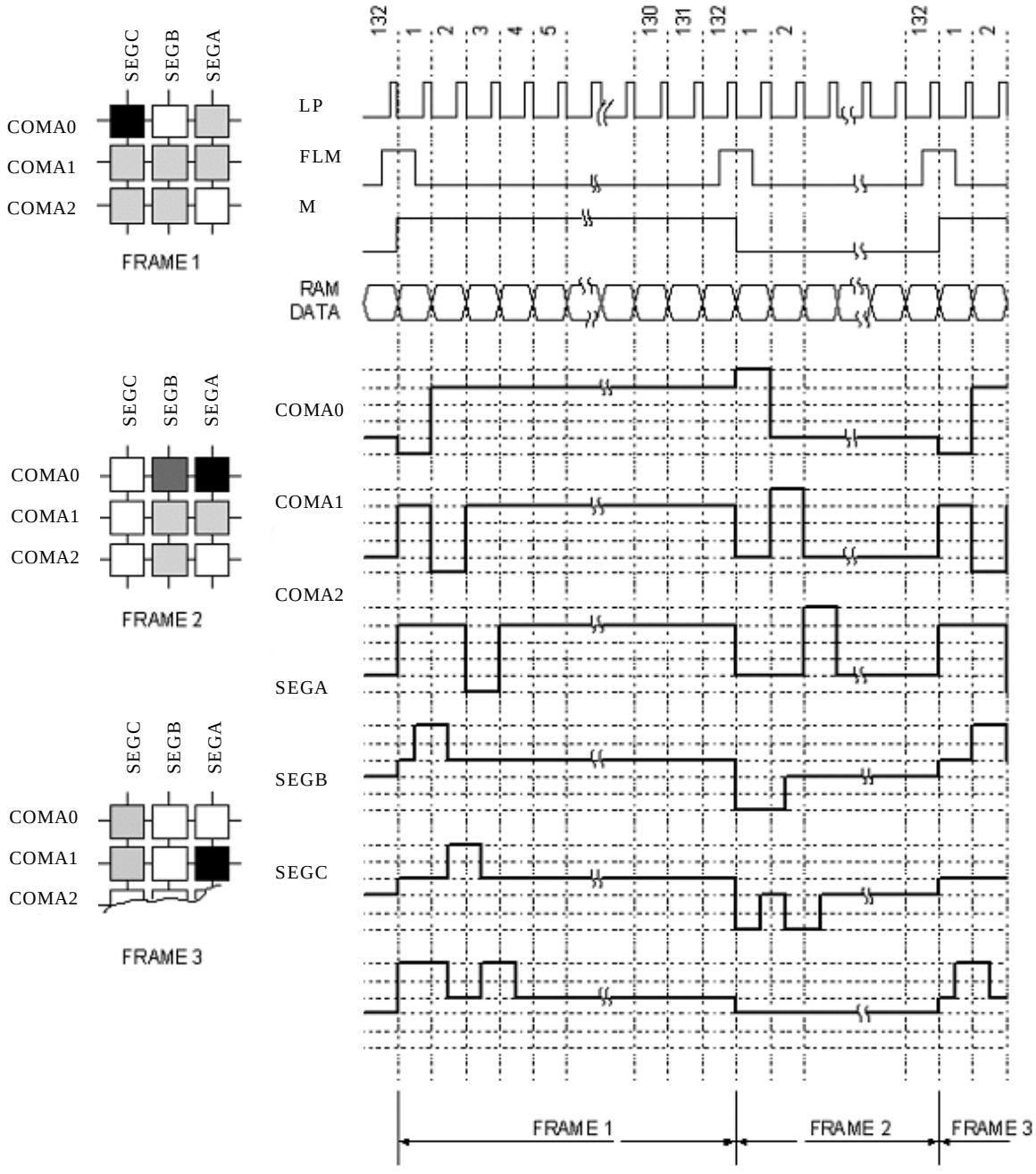


Fig 6 LCD Driving Waveforms (1/132Duty)

(9) OSCILLATOR

The oscillator consists of a resistor and a capacitor, and generates internal clocks for the display timing generator and the voltage booster. Through Oscillation Control register(CR), oscillating signal can be generated by using the internal resistor or an external resistor. Besides, external clock can be used too.

If using the internal resistor, ground OSCI pin and keep OSCO pin open. Frequency can be adjusted or divided by using Frequency Control register(MDIV). If using the external resistor, connect OSCI and OSCO with an resistor. If using external clock, input 50% duty signal to the OSCI pin.

(10) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator with temperature compensation circuit, the voltage regulator with EVR control and the LCD bias voltage generator. Furthermore the configuration of the LCD power supply can be arranged by setting Power Control 1 register(TCBI) and Power Control 2 register (POW2). It is possible to use part of the internal LCD power supply with an external supply, as shown in Table 17.

Table 9 Configuration of LCD Power Supply

DCON	AMPON	VGOFF	VBON	Voltage Booster	Voltage Converter			External Power Supply	Note
					Voltage Regulator (V_{REG} output)	Reference Voltage Generator (V_{BA} output)	LCD Bias Generator		
0	0	X	X	DISABLE	DISABLE	DISABLE	DISABLE	V_{OUT}, V_0, V_1, V_2, V_3 and V_4 are supplied	1
0	1	0	0	DISABLE	ENABLE	DISABLE	ENABLE	V_{OUT}, V_{REF} are supplied	2
		1	X		DISABLE	DISABLE		V_{OUT}, V_{REG} are supplied	3
		0	1		ENABLE	ENABLE		V_{OUT} is supplied	4
1	1	0	0	ENALBLE	ENABLE	DISABLE	ENABLE	V_{REF} is supplied	5
		1	X		DISABLE	DISABLE		V_{REG} is supplied	6
		0	1		ENABLE	ENABLE			

NOTE1) The LCD bias voltages are externally supplied, and C1±, C2±, C3±, C4±, C5±, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) The V_{OUT} and V_{REF} are externally supplied, and the C1±, C2±, C3±, C4±, C5± and V_{EE} are open.

NOTE3) The V_{OUT} and V_{REG} are externally supplied, and the C1±, C2±, C3±, C4±, C5± and V_{EE} are open.

NOTE4) The V_{OUT} is externally supplied, and the C1±, C2±, C3±, C4± and C5± are open.

NOTE5) The V_{REF} is externally supplied.

NOTE6) The V_{REG} is externally supplied

(10-1) Voltage Booster

The internal voltage booster generates up to 6xV_{EE} voltage. The boost level is selected from 2x~6x by setting the Boost Level register(GVU). The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

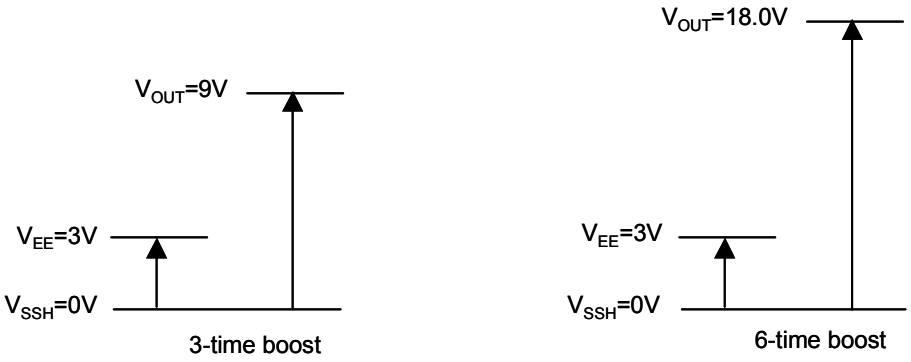


Fig 7 Boost Voltage

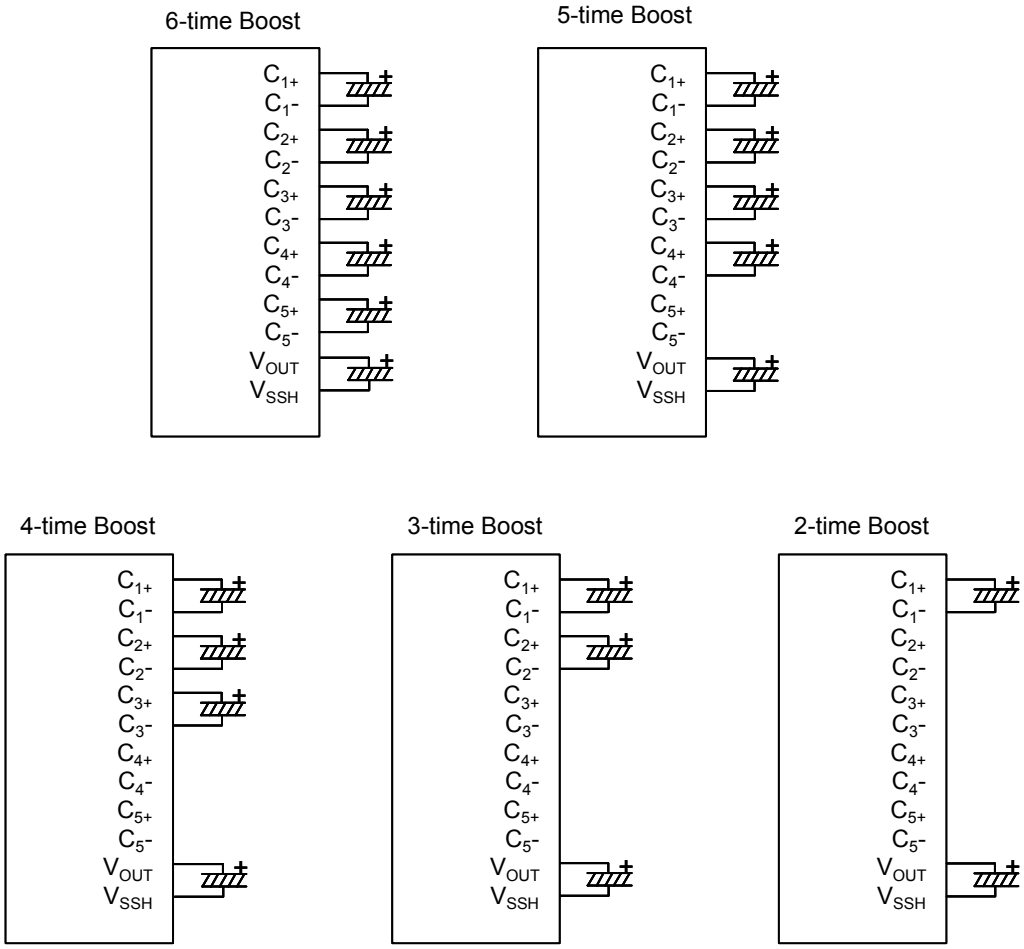


Fig 8 External Capacitor Connection of Voltage Booster

(10-2) Electrical Volume Register (EVR)

The EVR is used to fine-tune the V_0 voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the Electrical Volume register(EVOL).

(10-3) Voltage Converter

(10-3-1) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and gain control is set by the GSEL bit of the Boost Level register (GVU). When GSEL=0, boost level is determined by VU_2~VU_0 bits value. When GSEL=1, booster level is determined by RG_2~RG_0 bit value.

The relationship of V_{REG} and LCD driving voltage(V_0) is shown as below:

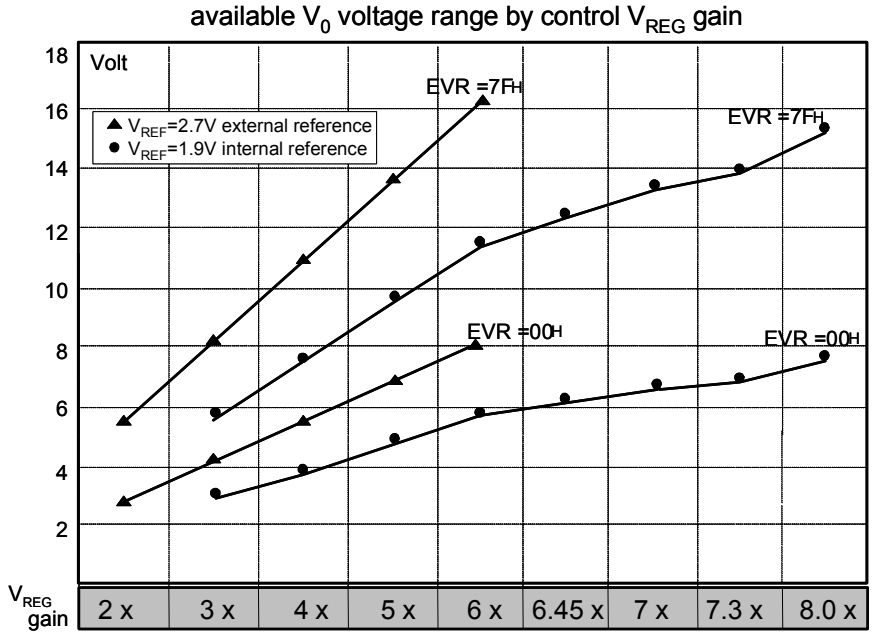


Fig 9 Relationship of V_0 and V_{REG}

Table 10 V_{REG} gain

GSEL = '0'			GSEL = '1'			V_{REG} Gain	Remark
VU2	VU1	VU0	RG2	RG1	RG0		
0	0	0				-	default VU[2:0]
0	0	1				2	
0	1	0	0	0	0	3	default RG[2:0]
0	1	1	0	0	1	4	
1	0	0	0	1	0	5	
1	0	1	0	1	1	6	
			1	0	0	6.45	
			1	0	1	7	
			1	1	0	7.3	
			1	1	1	8.0	
1	1	0				-	
1	1	1				-	

V_{REG} can be calculated by the following equation:

$$V_{REG} = V_{REF} \times N \qquad \text{(N: Boost Level)}$$

Note) To stabilize the V_{REG}, connect a capacitor to the V_{REG} pin.

(10-3-2) Reference Voltage Generator

The reference voltage generator outputs about 1.9V reference voltage. When using the internal LCD power supply, connect the V_{BA} and the V_{REF}. When using an external LCD power supply, input external power into V_{REF} pin and keep V_{BA} open.

The temperature compensating circuit is built in, compensation coefficient can be selected from the following shown 4 levels by setting TCV1~TVC0 bits of Power Control 1 register(TCBI).

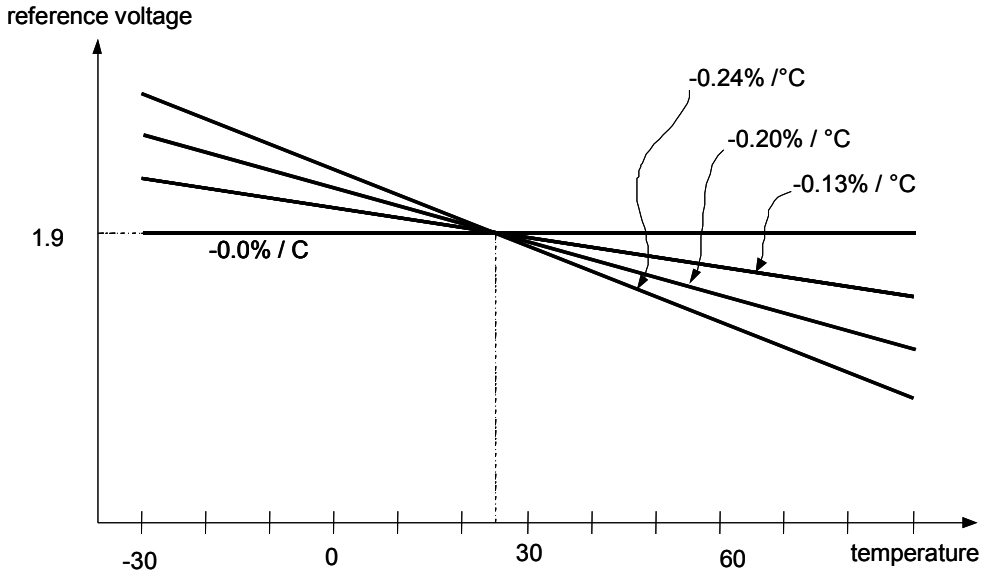


Fig 10 Temperature Compensation

Table 11 Temperature Coefficient Selection

TCV[1]	TCV[0]	V_{BA} Output	Remark
0	0	0.0 % /°C	Default setting
0	1	- 0.13 % /°C	
1	0	- 0.20 % /°C	
1	1	- 0.24 % /°C	

(10-3-3) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors, and the bias ratio can be selected from1/5~1/12 through setting B2~B0 bits of Power Control 1 register(TCBI).

(10-4) External Components for LCD Power Supply

Using External Power Supply

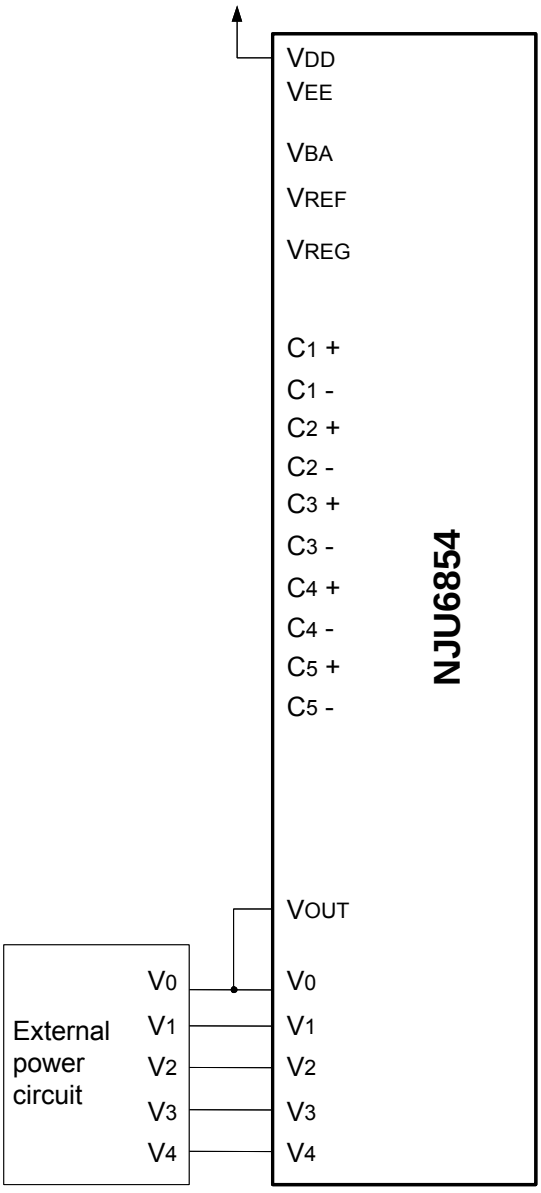


Fig 11

Only Using Internal Power Supply

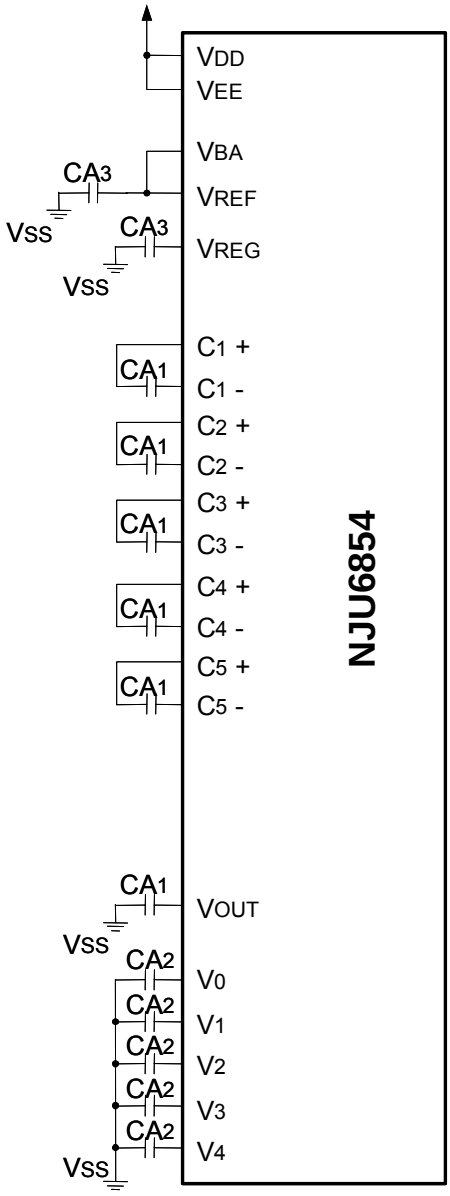


Fig 12

Reference guide values of capacitor

CA_1	0.47 ~ 4.7 uF
CA_2	0.47 ~ 2.2 uF
CA_3	0~0.1uF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_0, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal Power Supply without Reference Voltage Generator(1)

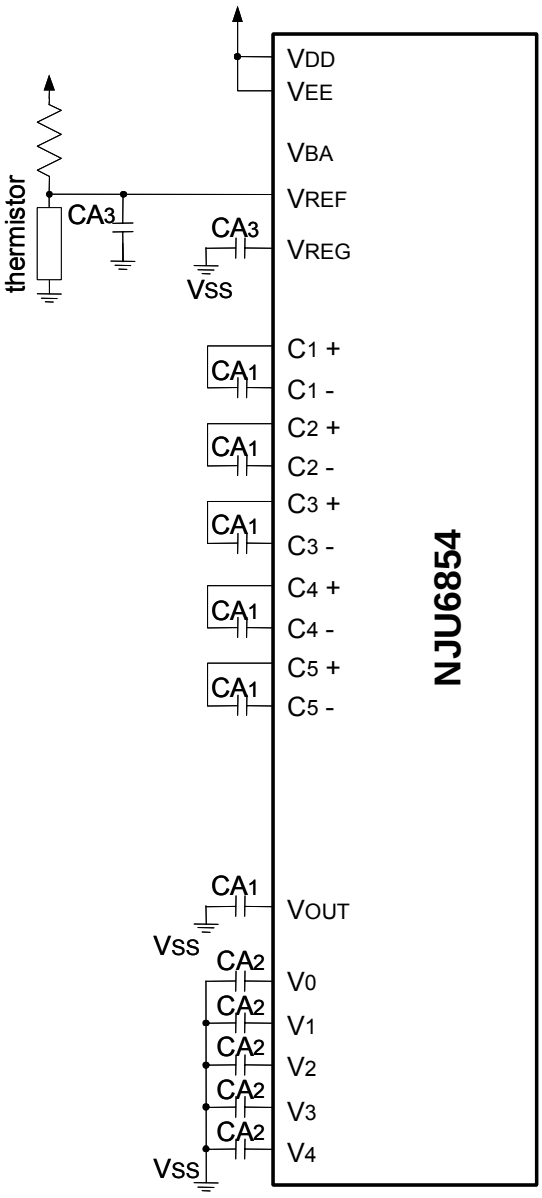


Fig 11

Using Internal Power Supply without Reference Voltage Generator(2)

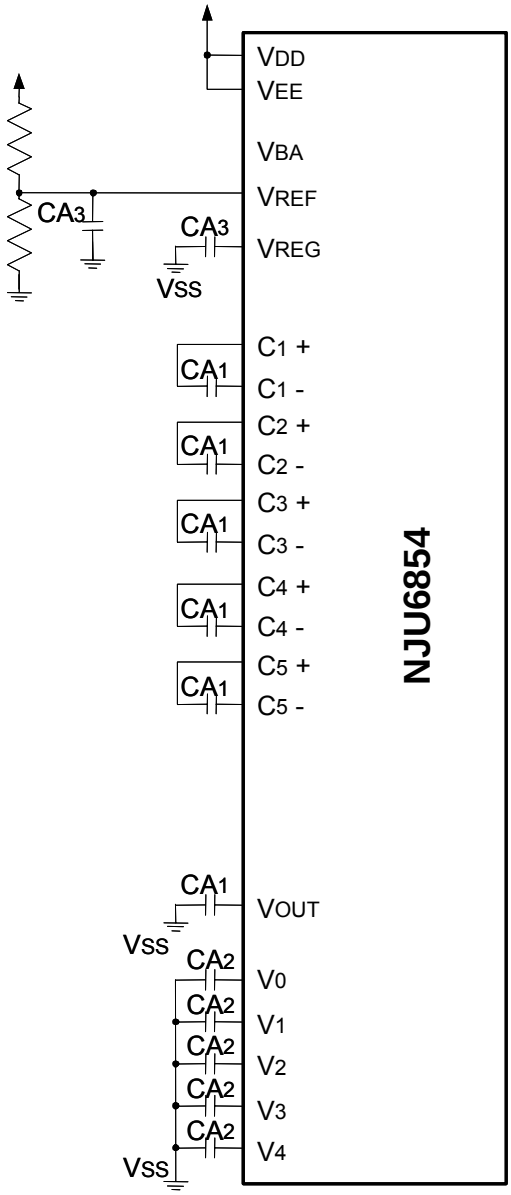


Fig 12

Reference guide values of capacitor

CA_1	0.47 ~ 4.7 uF
CA_2	0.47 ~ 2.2 uF
CA_3	0~0.1uF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_0, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

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Using Internal Power Supply
Without Voltage Booster

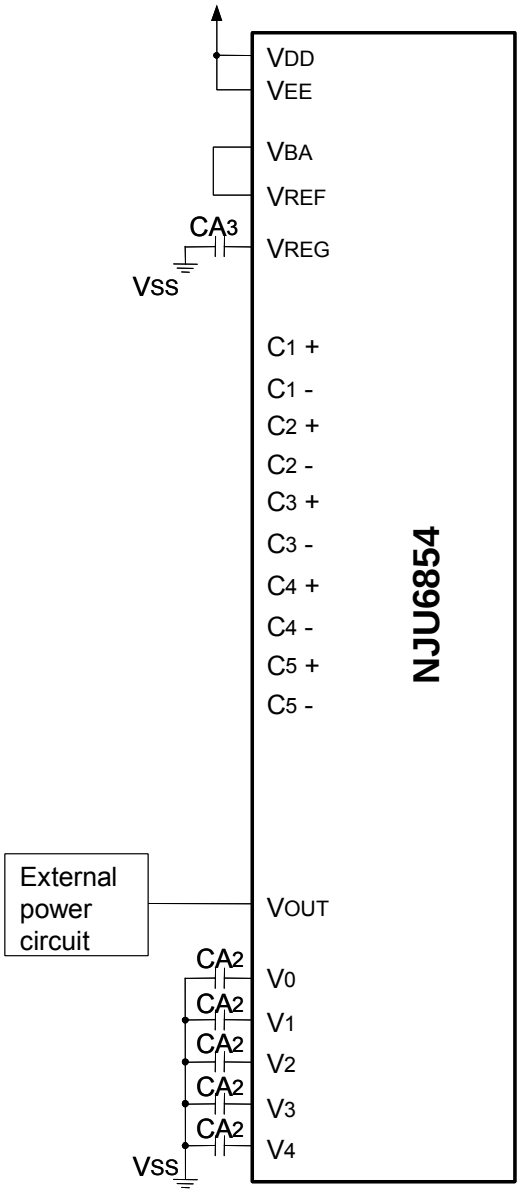


Fig 15

Reference guide values of capacitor

CA_1	0.47 ~ 4.7 uF
CA_2	0.47 ~ 2.2 uF
CA_3	0~0.1uF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD}, V_{SS}, V_{EE}, V_{SSH}, V_{OUT}, V_0, V_1, V_2, V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(10-5) Power ON/OFF

To protect the LSI from over current, the following sequences must be maintained to turn on and off the power supply.

Using Internal LCD Power Supply

Power ON

First "V_{DD} and V_{EE} ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First "Reset by RESb or "HALT" instruction", next "V_{DD} and V_{EE} OFF". If using different power sources for the V_{DD} and the V_{EE}, the V_{EE} must be turned off after the reset or the "HALT". After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_0~V_4) drop below the threshold level of LCD pixels.

Using External LCD Power Supply

Power ON

First "V_{DD} and V_{EE} ON", next "Reset by RESb", then "External LCD power supply ON". When using only external V_{OUT}, first "V_{DD} ON", next "Reset by RESb", then "External V_{OUT} ON", as well.

Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next "V_{DD} OFF". For more safety, placing a resistor in series on the V_0 line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50Ω and 100Ω.

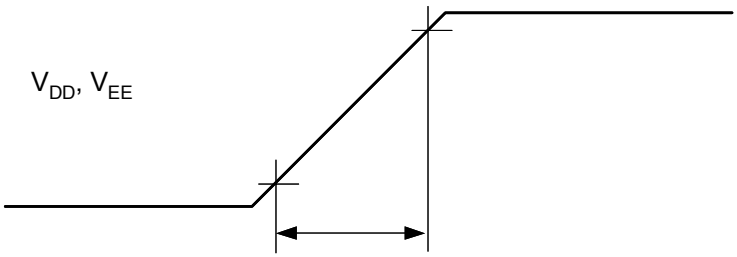


Fig 16 Rising Time of the Power Supply

Item	Recommended Rising Time	Applicable Power
tr	30 μs ~ 100 ms	V_{DD}, V_{EE}

Note : The rising time is the time from 10% V_{DD} to 90%V_{EE}

(10-6) Discharge Circuit

The LSI incorporates two independently discharge circuits for the capacitors connected to V_{OUT} and V_1-V_4. When setting DSI1 bit of Discharge ON/OFF register (DISC) to "1", or executing reset instruction, the capacitors on V_1-V_4 are discharged, by the same way, setting DSI2 to "1" or resetting, the capacitor on V_{OUT} is discharged.

Be sure to turn off the internal or external LCD power supply during discharging, otherwise discharge circuit will function as a current load and increase operating current.

(10-7) Reset Function

The reset function initializes the LSI to the following default status by setting the RESb to "L". Usually connect the RESb to MPU's reset pin, so that the LSI and MPU are initialized simultaneously.

Table 12 Default Status

ITEM	Initial value
DDRAM	Undefined
Y address	00_H
X address	00_H
DDRAM access increment mode	X/Y address increment ON
Bus length	8bit
Initial display line	0_H (1^{st} line)
Display ON/OFF	OFF
Reverse display ON/OFF	OFF(Normal)
Display clock monitor	OFF
Duty cycle ratio	1/132
Vertical Blanking Area	0
n-line Inversion ON/OFF	OFF
Common scan direction	COMA0 → COMA65 → COMB0 → COMB65
REF	REF=0(Normal)
Swap	OFF(Normal)
Electronic Volume Register(EVR)	(0, 0, 0, 0, 0, 0)
Internal LCD Power Supply	OFF
Display mode	Variable grayscale mode(64 grayscales)
Bias ratio	1/9 bias
Colors Select	65,536 colors
Grayscale palette Aj[6:0]	Default value
Grayscale palette Bj[6:0]	Default value
Grayscale palette Cj[6:0]	Default value
Extra palette PCX[6:0]	Default value
PWM output mode	Forward PWM
Discharge ON/OFF	OFF(0)

(11) INSTRUCTION TABLES

Table 0 [2:0] = 000_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	CR	*	*	*	*	*	CRF	CRS1	CRS0	OSC control
1	0001	CFG	AIM1	AIM0	VWR	IDSY	IDSX	WIN	UDS	SWIF	Display data Configuration /Window Area ON/OFF /Increment Control
2	0010	VPC	VPC7	VPC6	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	Display Line Number
3	0011	FVC	*	*	*	*	FVC3	FVC2	FVC1	FVC0	Blank Line Number
4	0100	ADRH	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	DDRAM X address
5	0101	ADRL	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0	DDRAM Y address
6	0110	EADRH	XEA7	XEA6	XEA5	XEA4	XEA3	XEA2	XEA1	XEA0	Window End X address
7	0111	EADRL	YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0	Window End Y address
8	1000	COLOR	PWMM1	PWMM0	*	MODE1	MODE0	*	*	MODED	Display Mode/Grayscale Mode
9	1001	MDIV	*	MDIV2	MDIV1	MDIV0	*	CRB2	CRB1	CRB0	OSC Frequency control
10	1010	HCT	*	HCT6	HCT5	HCT4	HCT3	HCT2	HCT1	HCT0	Header COM
11	1011	HST	HST7	HST6	HST5	HST4	HST3	HST2	HST1	HST0	Initial Display Line
12	1100	SSC1	SSC17	SSC16	SSC15	SSC14	SSC13	SSC12	SSC11	SSC10	Scan Start COM 1
13	1101	SSC2	SSC27	SSC26	SSC25	SSC24	SSC23	SSC22	SSC21	SSC20	Scan Start COM 2
14	1110	PCC1	PCC17	PCC16	PCC15	PCC14	PCC13	PCC12	PCC11	PCC10	Partial Display Line Number1
15	1111	PCC2	PCC27	PCC26	PCC25	PCC24	PCC23	PCC22	PCC21	PCC20	Partial Display Line Number 2

Table1 [2:0] = 001_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	MC	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0	N-line Inversion
1	0001	TCBI	VGOFF	VBON	TCV1	TCV0	*	B2	B1	B0	Power Control 1
2	0010	EVOL	*	EVOL6	EVOL5	EVOL4	EVOL3	EVOL2	EVOL1	EVOL0	Electronic Volume
3	0011	PBX	MON	*	*	GS	PBX3	PBX2	PBX1	PBX0	Display Timing Signal Monitor/Grayscale palette BX
4	0100	*	*	*	*	*	*	*	*	*	N/A
5	0101	POW2	*	*	*	CKCONT	AMPON	HALT	DCON	RES	Power control 2
6	0110	GVU	GSEL	RG2	RG1	RG0	*	VU2	VU1	VU0	Amplifier gain/ Booster Level
7	0111	BCK	BCKS	BCKG	*	*	BCK3	BCK2	BCK1	BCK0	Booster clock
8	1000	DISPLAY	REF	SWAP	*	SHIFT1	SHIFT0	TBC	TEN	ON/OFF	Display control
9	1001	PWM	*	*	PWMC1	PWMC0	PWMB1	PWMB0	PWMA1	PWMA0	PWM Mode control
10	1010	ECONT	TST0	EN3PTL	ENLED	REV	LED13	LED12	LED11	LED10	3 Partial Display / LED control / Rev
11	1011	DISC	*	*	*	*	*	*	DIS2	DIS1	Discharge control
12	1100	EDATA	LED27	LED26	LED25	LED24	LED23	LED22	LED21	LED20	LED control signal
13	1101	RA	RSS	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Setting Instruction Table
14	1110	SSC3	SSC37	SSC36	SSC35	SSC34	SSC33	SSC32	SSC31	SSC30	Scan Start COM 3
15	1111	PCC3	PCC37	PCC36	PCC35	PCC34	PCC33	PCC32	PCC31	PCC30	Partial Display Line Number3

Table2 [2:0] = 010_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	PA0	*	PA06	PA05	PA04	PA03	PA02	PA01	PA00	Grayscale palette A0 (0/31)
1	0001	PA1	*	PA16	PA15	PA14	PA13	PA12	PA11	PA10	Grayscale palette A1 (1/31)
2	0010	PA2	*	PA26	PA25	PA24	PA23	PA22	PA21	PA20	Grayscale palette A2 (2/31)
3	0011	PA3	*	PA36	PA35	PA34	PA33	PA32	PA31	PA30	Grayscale palette A3 (3/31)
4	0100	PA4	*	PA46	PA45	PA44	PA43	PA42	PA41	PA40	Grayscale palette A4 (4/31)
5	0101	PA5	*	PA56	PA55	PA54	PA53	PA52	PA51	PA50	Grayscale palette A5 (5/31)
6	0110	PA6	*	PA66	PA65	PA64	PA63	PA62	PA61	PA60	Grayscale palette A6 (6/31)
7	0111	PA7	*	PA76	PA75	PA74	PA73	PA72	PA71	PA70	Grayscale palette A7 (7/31)
8	1000	PA8	*	PA86	PA85	PA84	PA83	PA82	PA81	PA80	Grayscale palette A8 (8/31)
9	1001	PA9	*	PA96	PA95	PA94	PA93	PA92	PA91	PA90	Grayscale palette A9 (9/31)
10	1010	PA10	*	PA106	PA105	PA104	PA103	PA102	PA101	PA100	Grayscale palette A10 (10/31)
11	1011	PA11	*	PA116	PA115	PA114	PA113	PA112	PA111	PA110	Grayscale palette A11 (11/31)
12	1100	PA12	*	PA126	PA125	PA124	PA123	PA122	PA121	PA120	Grayscale palette A12 (12/31)
13	1101	PA13	*	PA136	PA135	PA134	PA133	PA132	PA131	PA130	Grayscale palette A13 (13/31)
14	1110	PA14	*	PA146	PA145	PA144	PA143	PA142	PA141	PA140	Grayscale palette A14 (14/31)
15	1111	PA15	*	PA156	PA155	PA154	PA153	PA152	PA151	PA150	Grayscale palette A15 (15/31)

Table3 [2:0] = 011_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	PA16	*	PA166	PA165	PA164	PA163	PA162	PA161	PA160	Grayscale palette A16 (16/31)
1	0001	PA17	*	PA176	PA175	PA174	PA173	PA172	PA171	PA170	Grayscale palette A17 (17/31)
2	0010	PA18	*	PA186	PA185	PA184	PA183	PA182	PA181	PA180	Grayscale palette A18 (18/31)
3	0011	PA19	*	PA196	PA195	PA194	PA193	PA192	PA191	PA190	Grayscale palette A19 (19/31)
4	0100	PA20	*	PA206	PA205	PA204	PA203	PA202	PA201	PA200	Grayscale palette A20 (20/31)
5	0101	PA21	*	PA216	PA215	PA214	PA213	PA212	PA211	PA210	Grayscale palette A21 (21/31)
6	0110	PA22	*	PA226	PA225	PA224	PA223	PA222	PA221	PA220	Grayscale palette A22 (22/31)
7	0111	PA23	*	PA236	PA235	PA234	PA233	PA232	PA231	PA230	Grayscale palette A23 (23/31)
8	1000	PA24	*	PA246	PA245	PA244	PA243	PA242	PA241	PA240	Grayscale palette A24 (24/31)
9	1001	PA25	*	PA256	PA255	PA254	PA253	PA252	PA251	PA250	Grayscale palette A25 (25/31)
10	1010	PA26	*	PA266	PA265	PA264	PA263	PA262	PA261	PA260	Grayscale palette A26 (26/31)
11	1011	PA27	*	PA276	PA275	PA274	PA273	PA272	PA271	PA270	Grayscale palette A27 (27/31)
12	1100	PA28	*	PA286	PA285	PA284	PA283	PA282	PA281	PA280	Grayscale palette A28 (28/31)
13	1101	PA29	*	PA296	PA295	PA294	PA293	PA292	PA291	PA290	Grayscale palette A29 (29/31)
14	1110	PA30	*	PA306	PA305	PA304	PA303	PA302	PA301	PA300	Grayscale palette A30 (30/31)
15	1111	PA31	*	PA316	PA315	PA314	PA313	PA312	PA311	PA310	Grayscale palette A31 (31/31)

Table4 [2:0] = 100_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	PB0	*	PB06	PB05	PB04	PB03	PB02	PB01	PB00	Grayscale palette B0 (0/31)
1	0001	PB1	*	PB16	PB15	PB14	PB13	PB12	PB11	PB10	Grayscale palette B1 (1/31)
2	0010	PB2	*	PB26	PB25	PB24	PB23	PB22	PB21	PB20	Grayscale palette B2 (2/31)
3	0011	PB3	*	PB36	PB35	PB34	PB33	PB32	PB31	PB30	Grayscale palette B3 (3/31)
4	0100	PB4	*	PB46	PB45	PB44	PB43	PB42	PB41	PB40	Grayscale palette B4 (4/31)
5	0101	PB5	*	PB56	PB55	PB54	PB53	PB52	PB51	PB50	Grayscale palette B5 (5/31)
6	0110	PB6	*	PB66	PB65	PB64	PB63	PB62	PB61	PB60	Grayscale palette B6 (6/31)
7	0111	PB7	*	PB76	PB75	PB74	PB73	PB72	PB71	PB70	Grayscale palette B7 (7/31)
8	1000	PB8	*	PB86	PB85	PB84	PB83	PB82	PB81	PB80	Grayscale palette B8 (8/31)
9	1001	PB9	*	PB96	PB95	PB94	PB93	PB92	PB91	PB90	Grayscale palette B9 (9/31)
10	1010	PB10	*	PB106	PB105	PB104	PB103	PB102	PB101	PB100	Grayscale palette B10 (10/31)
11	1011	PB11	*	PB116	PB115	PB114	PB113	PB112	PB111	PB110	Grayscale palette B11 (11/31)
12	1100	PB12	*	PB126	PB125	PB124	PB123	PB122	PB121	PB120	Grayscale palette B12 (12/31)
13	1101	PB13	*	PB136	PB135	PB134	PB133	PB132	PB131	PB130	Grayscale palette B13 (13/31)
14	1110	PB14	*	PB146	PB145	PB144	PB143	PB142	PB141	PB140	Grayscale palette B14 (14/31)
15	1111	PB15	*	PB156	PB155	PB154	PB153	PB152	PB151	PB150	Grayscale palette B15 (15/31)

Table5 [2:0] = 101_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	PB16	*	PB166	PB165	PB164	PB163	PB162	PB161	PB160	Grayscale palette B16 (16/31)
1	0001	PB17	*	PB176	PB175	PB174	PB173	PB172	PB171	PB170	Grayscale palette B17 (17/31)
2	0010	PB18	*	PB186	PB185	PB184	PB183	PB182	PB181	PB180	Grayscale palette B18 (18/31)
3	0011	PB19	*	PB196	PB195	PB194	PB193	PB192	PB191	PB190	Grayscale palette B19 (19/31)
4	0100	PB20	*	PB206	PB205	PB204	PB203	PB202	PB201	PB200	Grayscale palette B20 (20/31)
5	0101	PB21	*	PB216	PB215	PB214	PB213	PB212	PB211	PB210	Grayscale palette B21 (21/31)
6	0110	PB22	*	PB226	PB225	PB224	PB223	PB222	PB221	PB220	Grayscale palette B22 (22/31)
7	0111	PB23	*	PB236	PB235	PB234	PB233	PB232	PB231	PB230	Grayscale palette B23 (23/31)
8	1000	PB24	*	PB246	PB245	PB244	PB243	PB242	PB241	PB240	Grayscale palette B24 (24/31)
9	1001	PB25	*	PB256	PB255	PB254	PB253	PB252	PB251	PB250	Grayscale palette B25 (25/31)
10	1010	PB26	*	PB266	PB265	PB264	PB263	PB262	PB261	PB260	Grayscale palette B26 (26/31)
11	1011	PB27	*	PB276	PB275	PB274	PB273	PB272	PB271	PB270	Grayscale palette B27 (27/31)
12	1100	PB28	*	PB286	PB285	PB284	PB283	PB282	PB281	PB280	Grayscale palette B28 (28/31)
13	1101	PB29	*	PB296	PB295	PB294	PB293	PB292	PB291	PB290	Grayscale palette B29 (29/31)
14	1110	PB30	*	PB306	PB305	PB304	PB303	PB302	PB301	PB300	Grayscale palette B30 (30/31)
15	1111	PB31	*	PB316	PB315	PB314	PB313	PB312	PB311	PB310	Grayscale palette B31 (31/31)

Table6 [2:0] = 110_B

RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	PC0	*	PC06	PC05	PC04	PC03	PC02	PC01	PC00	Grayscale palette C0 (0/31)
1	0001	PC1	*	PC16	PC15	PC14	PC13	PC12	PC11	PC10	Grayscale palette C1 (1/31)
2	0010	PC2	*	PC26	PC25	PC24	PC23	PC22	PC21	PC20	Grayscale palette C2 (2/31)
3	0011	PC3	*	PC36	PC35	PC34	PC33	PC32	PC31	PC30	Grayscale palette C3 (3/31)
4	0100	PC4	*	PC46	PC45	PC44	PC43	PC42	PC41	PC40	Grayscale palette C4 (4/31)
5	0101	PC5	*	PC56	PC55	PC54	PC53	PC52	PC51	PC50	Grayscale palette C5 (5/31)
6	0110	PC6	*	PC66	PC65	PC64	PC63	PC62	PC61	PC60	Grayscale palette C6 (6/31)
7	0111	PC7	*	PC76	PC75	PC74	PC73	PC72	PC71	PC70	Grayscale palette C7 (7/31)
8	1000	PC8	*	PC86	PC85	PC84	PC83	PC82	PC81	PC80	Grayscale palette C8 (8/31)
9	1001	PC9	*	PC96	PC95	PC94	PC93	PC92	PC91	PC90	Grayscale palette C9 (9/31)
10	1010	PC10	*	PC106	PC105	PC104	PC103	PC102	PC101	PC100	Grayscale palette C10 (10/31)
11	1011	PC11	*	PC116	PC115	PC114	PC113	PC112	PC111	PC110	Grayscale palette C11 (11/31)
12	1100	PC12	*	PC126	PC125	PC124	PC123	PC122	PC121	PC120	Grayscale palette C12 (12/31)
13	1101	PC13	*	PC136	PC135	PC134	PC133	PC132	PC131	PC130	Grayscale palette C13 (13/31)
14	1110	PC14	*	PC146	PC145	PC144	PC143	PC142	PC141	PC140	Grayscale palette C14 (14/31)
15	1111	PC15	*	PC156	PC155	PC154	PC153	PC152	PC151	PC150	Grayscale palette C15 (15/31)

Table7 [2:0] = 111_B

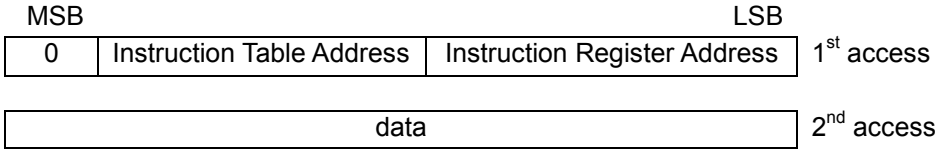
RA[3:0]		Name	D7	D6	D5	D4	D3	D2	D1	D0	REMARK
0	0000	PC16	*	PC166	PC165	PC164	PC163	PC162	PC161	PC160	Grayscale palette C16 (16/31)
1	0001	PC17	*	PC176	PC175	PC174	PC173	PC172	PC171	PC170	Grayscale palette C17 (17/31)
2	0010	PC18	*	PC186	PC185	PC184	PC183	PC182	PC181	PC180	Grayscale palette C18 (18/31)
3	0011	PC19	*	PC196	PC195	PC194	PC193	PC192	PC191	PC190	Grayscale palette C19 (19/31)
4	0100	PC20	*	PC206	PC205	PC204	PC203	PC202	PC201	PC200	Grayscale palette C20 (20/31)
5	0101	PC21	*	PC216	PC215	PC214	PC213	PC212	PC211	PC210	Grayscale palette C21 (21/31)
6	0110	PC22	*	PC226	PC225	PC224	PC223	PC222	PC221	PC220	Grayscale palette C22 (22/31)
7	0111	PC23	*	PC236	PC235	PC234	PC233	PC232	PC231	PC230	Grayscale palette C23 (23/31)
8	1000	PC24	*	PC246	PC245	PC244	PC243	PC242	PC241	PC240	Grayscale palette C24 (24/31)
9	1001	PC25	*	PC256	PC255	PC254	PC253	PC252	PC251	PC250	Grayscale palette C25 (25/31)
10	1010	PC26	*	PC266	PC265	PC264	PC263	PC262	PC261	PC260	Grayscale palette C26 (26/31)
11	1011	PC27	*	PC276	PC275	PC274	PC273	PC272	PC271	PC270	Grayscale palette C27 (27/31)
12	1100	PC28	*	PC286	PC285	PC284	PC283	PC282	PC281	PC280	Grayscale palette C28 (28/31)
13	1101	PC29	*	PC296	PC295	PC294	PC293	PC292	PC291	PC290	Grayscale palette C29 (29/31)
14	1110	PC30	*	PC306	PC305	PC304	PC303	PC302	PC301	PC300	Grayscale palette C30 (30/31)
15	1111	PC31	*	PC316	PC315	PC314	PC313	PC312	PC311	PC310	Grayscale palette C31 (31/31)

(12) INSTRUCTION DESCRIPTIONS

(12-1) 8-bit Access Mode

(12-1-1) Instruction Register

Set MSB bit of the 1st byte to "0". Data to instruction register is transferred in 2 bytes, For the 1st byte, D6~D4 is used to set the instruction table address, and D3~D0 to set instruction register address. The 2nd byte is instruction data.



(Example) X, Y address of DDRAM

Step 1: 1st byte(X address)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0

CSb	RS	RDb	WRb
0	1	1	0

0 Table address Register address — Pins setting

Step 2: 2nd byte(X address)

D7	D6	D5	D4	D3	D2	D1	D0
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0

CSb	RS	RDb	WRb
0	1	1	0

Step 3: 1st byte(Y address)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1

CSb	RS	RDb	WRb
0	1	1	0

0 Table address Register address — Pins setting

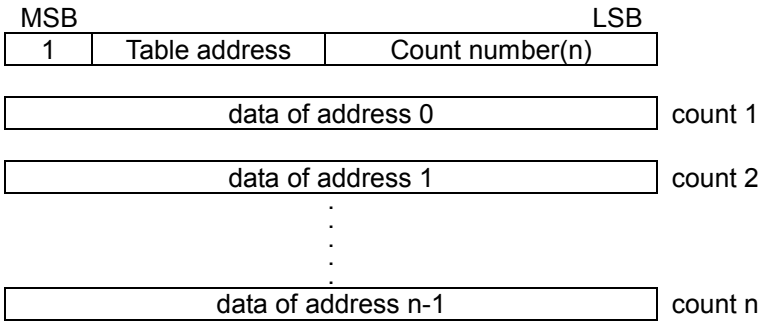
Step 4: 2nd byte(Y address).

D7	D6	D5	D4	D3	D2	D1	D0
YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0

CSb	RS	RDb	WRb
0	1	1	0

(12-1-2) Auto-increment of Instruction Register Address

By setting MSB bit of the 1st byte to "1", instruction data can be written to the registers successively. For the 1st byte, D6~D4 is used to set the instruction table address(Table[2:0]) and D3~D0 to set the count number for the registers, from the 2nd byte, data will be automatically written to the successive registers.



If the counter number is set as 0, data is written to the registers from the address 0 to 15.

(Example) Oscillator and others.

Step 1: 8bit auto increment / table address set / count number

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	1
1	Table address			count number = 5			

CSb	RS	RDb	WRb
0	1	1	0
Pins setting			

Step 2: 8bit auto increment / count = 1

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	CRF	CRS1	CRS0

CSb	RS	RDb	WRb
0	1	1	0

Step 3: 8 bit auto increment / count = 2

D7	D6	D5	D4	D3	D2	D1	D0
AIM1	AIM0	VWR	IDSY	IDSX	WIN	UDS	SWIF

CSb	RS	RDb	WRb
0	1	1	0

Step 4: 8 bit auto increment / count = 3

D7	D6	D5	D4	D3	D2	D1	D0
VPC7	VPC6	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0

CSb	RS	RDb	WRb
0	1	1	0

Step 5: 8 bit auto increment / count = 4

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	FVC3	FVC2	FVC1	FVC0

CSb	RS	RDb	WRb
0	1	1	0

Step 6: 8 bit auto increment / count = 5

D7	D6	D5	D4	D3	D2	D1	D0
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0

CSb	RS	RDb	WRb
0	1	1	0

(12-2) 16-bit Access Mode

(12-2-1) Instruction Register

Set MSB bit to"0". Instruction table number, instruction register address and instruction data will be transferred in one 16-bit data. Instruction table number is determined by D14~D12, instruction register is determined by D11~D8, and D7~D0 is instruction data.

MSB			LSB
0	Table address	Register address	Instruction data

(Example) X, Y address of DDRAM

Step 1: X address setting.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	0	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0
0	Table address			Register address				data							

Step 1: Y address setting

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	0	1	YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0
0	Table address			Register address				data							

(12-2-2) Auto Increment of Instruction Register Address

By setting MSB bit of the 1st byte to "1", instruction data can be written to the registers successively. For the 1st byte, only upper 8-bit data is valid, D14~D12 is used to set the instruction table number(Table[2:0]) and D11~D8 to set the count number of the registers. From the 2nd byte, data will be automatically written to the successive registers.

MSB		LSB
1	Table address	Count number(n)

data of address 0	data of address 1
data of address 2	data of address 3
..	..
.	.
.	.
data of address n-2	data of address n-1

If count number is 0, data is written to the registers from the address 0 to 15.

(Example) Oscillator and Configuration control

Step 1:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	1	0	1	*	*	*	*	*	*	*	*
1	Table address			count number = 5				data (don't care)							

Step 2:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	CRF	CRS1	CRS0	AIM1	AIM0	VWR	IDSY	IDSX	WIN	UDS	SWIF

Step 3:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VPC7	VPC6	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	*	*	*	*	FVC3	FVC2	FVC1	FVC0

Step 4:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	*	*	*	*	*	*	*	*

(*: not applicable)

(12-3) Oscillation Control

Register : CR Table0 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	CRF	CRS1	CRS0

CSb	RS	RDb	WRb
0	1	1	0

(default: {CRF, CRS1, CRS0} = 0_H, address: 0_H)

Setting Frequency

CRF	CRS1	CRS0	Function
0	0	0	OSCI (730 kHz)
0	0	1	OSC2 (170 kHz)
0	1	0	OSC5 (external R, external source)
0	1	1	Invalid
1	0	0	OSC3 (1,200 kHz)
1	0	1	OSC4 (285 kHz)
1	1	0	Invalid
1	1	1	Invalid

In OSC5 mode, connect the OSCI pin and the OSCO pin with a resistor, and input external clock signal to OSCI.

(12-4) Display Data Assignment/ Window Area ONOFF/Increment Control

Register: CFG / Table 0 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
AIM1	AIM0	VWR	IDSY	IDSX	WIN	UDS	SWIF

CSb	RS	RDb	WRb
0	1	1	0

(default: {AIM1, AIM0, VWR, IDSY, ISDX, WIN, UDS, SWIF} = 0_H, address: 1_H)

(i) SWIF

SWIF	Bus length
0	8bit I/F (Initial Value)
1	16bit I/F

(ii) UDS

Assignment of MPU data on the DDRAM

16 Bit I/F Access

UDS = "0": the lower 8-bit MPU data corresponding to the lower 8-bit display data
the upper 8-bit MPU data corresponding to the upper 8-bit display data

UDS = "1": the lower 8-bit MPU data corresponding to the upper 8-bit display data
the upper 8-bit MPU data corresponding to the lower 8-bit display data

8 Bit I/F Access

UDS = "0": 1st MPU data corresponding to the lower 8-bit display data
2nd MPU data corresponding to the upper 8-bit display data

UDS = "1": 1st MPU data corresponding to the upper 8-bit display data
2nd MPU data corresponding to the lower 8-bit display data

(iii) WIN

WIN = "1" : Window area ON
WIN = "0" : Window area OFF(default)

(iv) IDSX

X address auto increment/auto decrement

IDSX = "0" : auto increment
IDSX = "1" : auto decrement

(v) IDSY

Y address auto increment/auto decrement

IDSY = "0" : auto increment
IDSY = "1" : auto decrement

(vi) VWR

Setting the direction of data write /read to DDRAM

VWR = "0" : start from X direction

VWR = "1" : start from Y direction

(vii) AIM[1:0]

AIM1	AIM0	
0	0	Auto increment/decrement during data writing and reading
0	1	Auto increment/decrement during data writing
1	0	Auto increment/decrement OFF
1	1	Prohibited

(12-5) Display Line Number

Register: VPC TABLE0 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
VPC7	VPC6	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0

CSb	RS	RDb	WRb
0	1	1	0

(default: VPC[7:0] = 84_H, address: 2_H)

VPC[7:0]: display line number (displayed pixel number in Y direction).

Setting within the range of 2~132（02H~84H）

VPC7	VPC6	VPC5	VPC4	VPC3	VPC2	VPC1	VPC0	Vertical Pixel Number
0	0	0	0	0	0	0	0	Forbidden
0	0	0	0	0	0	0	1	Forbidden
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
0	0	0	0	0	1	0	1	5
				:				
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131
1	0	0	0	0	1	0	0	132
1	0	0	0	0	1	0	1	Forbidden
				:				
1	1	1	1	1	1	1	1	Forbidden

(12-6) Blank Line Number

Register : FVC TABLE0 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	FVC3	FVC2	FVC1	FVC0

CSb	RS	RDb	WRb
0	1	1	0

(default: FVC[3:0]=0_H, address: 3_H)

FVC[3:0]: Blank line number(not displayed pixel number in Y direction)

FVC3	FVC2	FVC1	FVC0	Vertical blanking Lines
0	0	0	0	0
0	0	0	1	1
		:		
1	1	1	0	14
1	1	1	1	15

(12-7) X Address

Register : ADRH TABLE0 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0

CSb	RS	RDb	WRb
0	1	1	0

(default: XA[7:0] = 0H, address: 4H)
X address range is from 00H to 83H.

(12-8) Y Address

Register : ADRL TABLE0 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0

CSb	RS	RDb	WRb
0	1	1	0

(default: YA[7:0] = 0_H, address: 5_H)
Y address range is from 00H to 83H.

(12-9) Window End X Address

Register : EADRH TABLE0 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
XEA7	XEA6	XEA5	XEA4	XEA3	XEA2	XEA1	XEA0

CSb	RS	RDb	WRb
0	1	1	0

(default: XEA[7:0] = 0_H, address: 6_H)
Setting X address of window area when window area access is valid(WIN="1").

(12-10) Window End Y Address

Register : EADRL TABLE0 [7H]

D7	D6	D5	D4	D3	D2	D1	D0
YEA7	YEA6	YEA5	YEA4	YEA3	YEA2	YEA1	YEA0

CSb	RS	RDb	WRb
0	1	1	0

(default: YEA[7:0] = 0_H, address: 7_H)
Setting Y address of window area when window area access is valid(WIN="1").

(12-11) Display Mode/Grayscale Mode

Register : COLOR TABLE0 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
PWMM1	PWMM0	*	MODE1	MODE0	*	*	MODED

CSb	RS	RDb	WRb
0	1	1	0

(default: PWMM[1:0], MODE[1:0], MODED = 0_H, address: 8_H)

(i) MODED

Setting 65k-color or 4k-color display mode

MODED	Display Color Mode
0	65,536 Colors Mode (PWM 5bit + 2 FRC)
1	4,096 Colors(4bit PWM only)

(ii) MODE[1:0]

Bit assignment of display data

MODE[1:0]		Input data																Remar
MODE1	MODE0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	C4	C3	C2	C1	C0	B5	B4	B3	B2	B1	B0	A4	A3	A2	A1	A0	Note (1)
0	1	C3	C2	C1	C0		B3	B2	B1	B0			A3	A2	A1	A0		Note (2)
1	0					C3	C2	C1	C0	B3	B2	B1	B0	A3	A2	A1	A0	Note (3)
1	1																	Invalid

Note (1) 65,536 colors 5-6-5 data
(2) 4,096 colors 4-4-4 data
(3) 4,096 colors4-4-4 data, upper 4 bits invalid

(iii) PWMM[1:0]

Setting grayscale mode through PWM control.

PWMM1	PWMM0	Grayscale Mode
0	0	Select 32 grayscales（65k mode）or 16 grayscales（4k mode）from 64 levels.
0	1	Select 32 grayscales（65k mode）or 16 grayscales（4k mode）from 32 levels.
1	0	Select 16 grayscales（4k mode）from 16 levels.
1	1	Select 32 grayscales（65k mode）or 16 grayscales（4k mode）from 128 levels.

Using PWM control (PWMM[1:0]) and Frame rate control(FRC), the following display mode can be selected.

MODED	Display Mode	FRC control	PWM control			
			64 grayscales base	32 grayscales base	16 grayscales base	128 grayscales base
0	65,536 color mode	2 scan	32 grayscales selectable	32grayscales selectable	Forbidden	32 grayscales selectable
1	4,096 color mode	unavailable	16 grayscales selectable	16 grayscales selectable	16 grayscales selectable	16 grayscales selectable

The relationship among the oscillating circuit, built-in clock and frame frequency

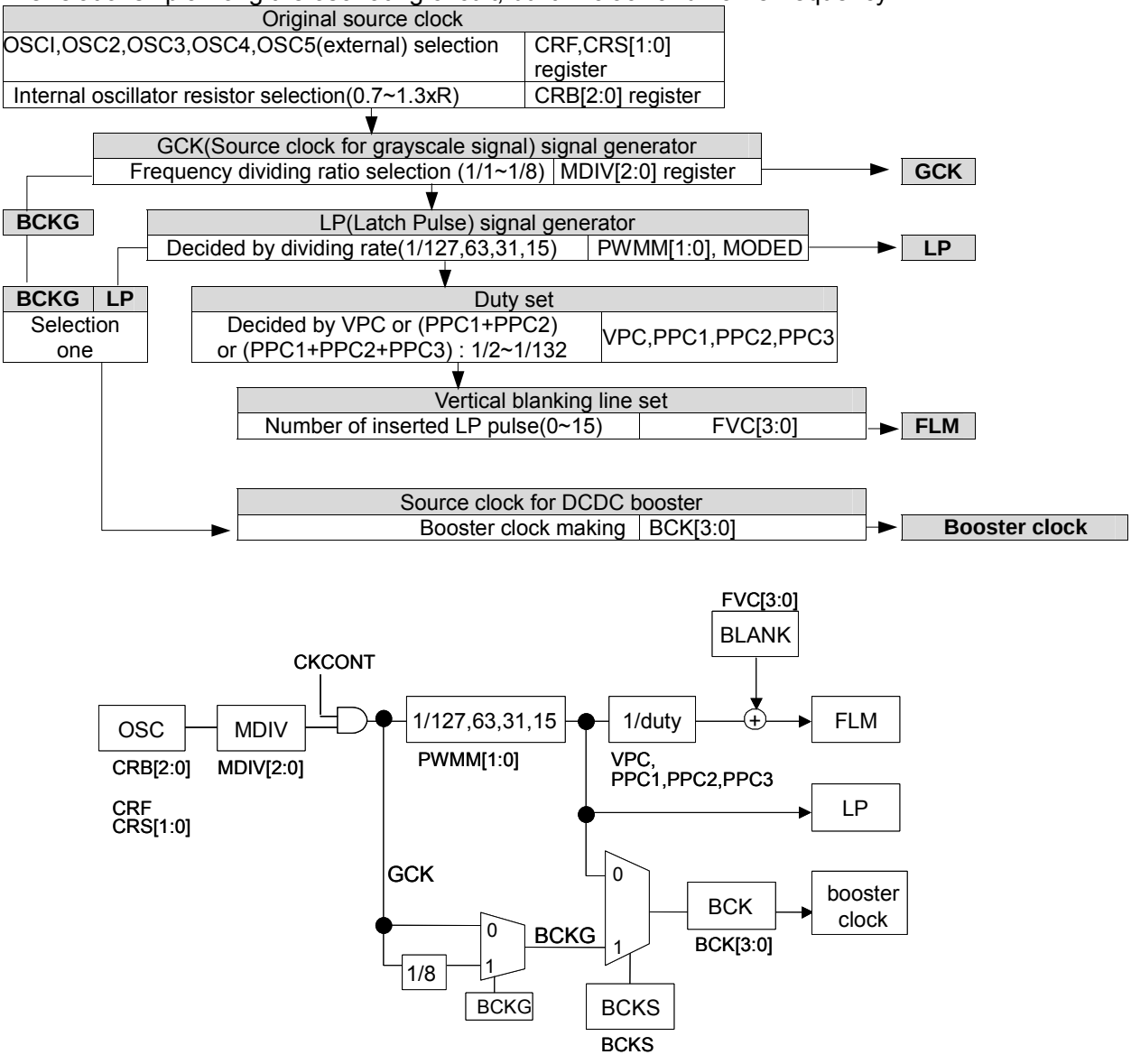


Fig 17 Block Diagram of Oscillator

Frame Duty = 1 / (duty + blank)

PWM duty vs. display mode

Display mode	MODED	PWM control			
		PWMM=00	PWMM=01	PWMM=10	PWMM=11
		variable	variable	fixed	variable
65,536 color mode	0	1/63	1/31	Forbidden	1/127
4,096 color mode	1	1/63	1/31	1/15	1/127

Frame frequency vs. display mode

Usag	Oscillator	GCK	Display mode	Grayscale mode (PWMM[1:0])		Duty	Blank	Equation*1)
1	1200 kHz	1/1 undivided	65,536 color	Variable	Among 128	1/132	0	FLM=1200kHz/(1x127x(132+ 0))=72Hz
							5	FLM=1200kHz/(1x127x(132+ 5))=69Hz
2	285 kHz	1/1 undivided	4,096 color	Variable	Among 32	1/132	0	FLM=285kHz/(1x31x(132+ 0))=70Hz
							10	FLM=285kHz/(1x31x(132+10))=65Hz
3	170 kHz	1/1 undivided	4,096 color	Fixed	Among 32	1/132	0	FLM=170kHz/(1x15x(132+ 0))=86Hz
							15	FLM=170kHz/(1x15x(132+15))=77Hz
4	730 kHz	1/1 undivided	65,536 color	Variable	Among 64	1/132	0	FLM=730kHz/(1x63x(132+ 0))=88Hz
							8	FLM=730kHz/(1x63x(132+ 8))=83Hz

NOTE): FLM: frame frequency = f_{OSC} / (MDIV(1,2,3,4,5,6,7,8) x PWMM(15,31,63,127) x (Duty + Blank))

65k Colors Display Mode
Display data and grayscale palette.

Display RAM data						Grayscale by PWM + FRC			
A4	A3	A2	A1	A0	-	A/C	B		C/A
B5	B4	B3	B2	B1	B0	32 gray	64 gray (1)		32 gray
C4	C3	C2	C1	C0	-	GS=X	GS=1	GS=0	GS=X
0	0	0	0	0	0	PA0	PB0	PB0	PC0
0	0	0	0	0	1		PB0	PBX	
0	0	0	0	1	0	PA1	(PB0 + PB1) / 2	(PB0 + PB1) / 2	PC1
0	0	0	0	1	1		PB1	PB1	
0	0	0	1	0	0	PA2	(PB1 + PB2) / 2	(PB1 + PB2) / 2	PC2
0	0	0	1	0	1		PB2	PB2	
0	0	0	1	1	0	PA3	(PB2 + PB3) / 2	(PB2 + PB3) / 2	PC3
0	0	0	1	1	1		PB3	PB3	
0	0	1	0	0	0	PA4	(PB3 + PB4) / 2	(PB3 + PB4) / 2	PC4
0	0	1	0	0	1		PB4	PB4	
0	0	1	0	1	0	PA5	(PB4 + PB5) / 2	(PB4 + PB5) / 2	PC5
0	0	1	0	1	1		PB5	PB5	
0	0	1	1	0	0	PA6	(PB5 + PB6) / 2	(PB5 + PB6) / 2	PC6
0	0	1	1	0	1		PB6	PB6	
0	0	1	1	1	0	PA7	(PB6 + PB7) / 2	(PB6 + PB7) / 2	PC7
0	0	1	1	1	1		PB7	PB7	
0	1	0	0	0	0	PA8	(PB7 + PB8) / 2	(PB7 + PB8) / 2	PC8
0	1	0	0	0	1		PB8	PB8	
0	1	0	0	1	0	PA9	(PB8 + PB9) / 2	(PB8 + PB9) / 2	PC9
0	1	0	0	1	1		PB9	PB9	
0	1	0	1	0	0	PA10	(PB9 + PB10) / 2	(PB9 + PB10) / 2	PC10
0	1	0	1	0	1		PB10	PB10	
0	1	0	1	1	0	PA11	(PB10 + PB11) / 2	(PB10 + PB11) / 2	PC11
0	1	0	1	1	1		PB11	PB11	
0	1	1	0	0	0	PA12	(PB11 + PB12) / 2	(PB11 + PB12) / 2	PC12
0	1	1	0	0	1		PB12	PB12	
0	1	1	0	1	0	PA13	(PB12 + PB13) / 2	(PB12 + PB13) / 2	PC13
0	1	1	0	1	1		PB13	PB13	
0	1	1	1	0	0	PA14	(PB13 + PB14) / 2	(PB13 + PB14) / 2	PC14
0	1	1	1	0	1		PB14	PB14	
0	1	1	1	1	0	PA15	(PB14 + PB15) / 2	(PB14 + PB15) / 2	PC15
0	1	1	1	1	1		PB15	PB15	
1	0	0	0	0	0	PA16	(PB15 + PB16) / 2	(PB15 + PB16) / 2	PC16
1	0	0	0	0	1		PB16	PB16	
1	0	0	0	1	0	PA17	(PB16 + PB17) / 2	(PB16 + PB17) / 2	PC17
1	0	0	0	1	1		PB17	PB17	
1	0	0	1	0	0	PA18	(PB17 + PB18) / 2	(PB17 + PB18) / 2	PC18
1	0	0	1	0	1		PB18	PB18	
1	0	0	1	1	0	PA19	(PB18 + PB19) / 2	(PB18 + PB19) / 2	PC19
1	0	0	1	1	1		PB19	PB19	
1	0	1	0	0	0	PA20	(PB19 + PB20) / 2	(PB19 + PB20) / 2	PC20
1	0	1	0	0	1		PB20	PB20	
1	0	1	0	1	0	PA21	(PB20 + PB21) / 2	(PB20 + PB21) / 2	PC21
1	0	1	0	1	1		PB21	PB21	
1	0	1	1	0	0	PA22	(PB21 + PB22) / 2	(PB21 + PB22) / 2	PC22
1	0	1	1	0	1		PB22	PB22	
1	0	1	1	1	0	PA23	(PB22 + PB23) / 2	(PB22 + PB23) / 2	PC23
1	0	1	1	1	1		PB23	PB23	
1	1	0	0	0	0	PA24	(PB23 + PB24) / 2	(PB23 + PB24) / 2	PC24
1	1	0	0	0	1		PB24	PB24	
1	1	0	0	1	0	PA25	(PB24 + PB25) / 2	(PB24 + PB25) / 2	PC25
1	1	0	0	1	1		PB25	PB25	
1	1	0	1	0	0	PA26	(PB25 + PB26) / 2	(PB25 + PB26) / 2	PC26
1	1	0	1	0	1		PB26	PB26	
1	1	0	1	1	0	PA27	(PB26 + PB27) / 2	(PB26 + PB27) / 2	PC27
1	1	0	1	1	1		PB27	PB27	
1	1	1	0	0	0	PA28	(PB27 + PB28) / 2	(PB27 + PB28) / 2	PC28
1	1	1	0	0	1		PB28	PB28	
1	1	1	0	1	0	PA29	(PB28 + PB29) / 2	(PB28 + PB29) / 2	PC29
1	1	1	0	1	1		PB29	PB29	
1	1	1	1	0	0	PA30	(PB29 + PB30) / 2	(PB29 + PB30) / 2	PC30
1	1	1	1	0	1		PB30	PB30	
1	1	1	1	1	0	PA31	(PB30 + PB31) / 2	(PB30 + PB31) / 2	PC31
1	1	1	1	1	1		PB31	PB31	

Note1) 5 bits for PWM control and 1 bit for Frame rate control(total 6 bits display data), SEGBi can realize 64-grayscale (32-grayscalex2) display.
Note2) Real 64-grayscael can be realized by setting PBX bit(GS="0").

4k Colors Display Mode
Display data and grayscale palette.

Display RAM data				Grayscale by PWM		
A3	A2	A1	A0	A / C	B	C / A
B3	B2	B1	B0	16 gray	16 gray	16 gray
C3	C2	C1	C0	GS=X	GS=X	GS=X
0	0	0	0	PA1	PB1	PC1
0	0	0	1	PA3	PB3	PC3
0	0	1	0	PA5	PB5	PC5
0	0	1	1	PA7	PB7	PC7
0	1	0	0	PA9	PB9	PC9
0	1	0	1	PA11	PB11	PC11
0	1	1	0	PA13	PB13	PC13
0	1	1	1	PA15	PB15	PC15
1	0	0	0	PA17	PB17	PC17
1	0	0	1	PA19	PB19	PC19
1	0	1	0	PA21	PB21	PC21
1	0	1	1	PA23	PB23	PC23
1	1	0	0	PA25	PB25	PC25
1	1	0	1	PA27	PB27	PC27
1	1	1	0	PA29	PB29	PC29
1	1	1	1	PA31	PB31	PC31

Note) Under 4k colors display mode, GS bit is invalid.

(12-12) Oscillating Frequency Adjustment/Frequency Dividing

Register : MDIV TABLE0 [9H]

D7	D6	D5	D4	D3	D2	D1	D0
*	MDIV2	MDIV1	MDIV0	*	CRB2	CRB1	CRB0

CSb	RS	RDb	WRb
0	1	1	0

(default: MDIV[2:0], CRB[2:0] = 0H, address : 9H)

(i) CRB[2:0]
Frame frequency can be modified by adjusting the resistor of oscillating circuit.

Relationship between RF and Resistance ratio

CRB2	CRB1	CRB0	Status
0	0	0	Initial Resistance Ratio
0	0	1	1.1 times of Initial Resistance Ratio
0	1	0	1.2 times of Initial Resistance Ratio
0	1	1	1.3 times of Initial Resistance Ratio
1	0	0	0.9 times of Initial Resistance Ratio
1	0	1	0.8 times of Initial Resistance Ratio
1	1	0	0.7 times of Initial Resistance Ratio
1	1	1	Forbidden

(ii) MDIV[2:0]

Oscillating Frequency or external clock frequency can be divided.

MDIV2	MDIV1	MDIV0	Divide Ratio
0	0	0	1/1 dividing
0	0	1	1/2 dividing
0	1	0	1/3 dividing
0	1	1	1/4 dividing
1	0	0	1/5 dividing
1	0	1	1/6 dividing
1	1	0	1/7 dividing
1	1	1	1/8 dividing

(12-13) Header COM

Register : HCT TABLE0 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	HCT6	HCT5	HCT4	HCT3	HCT2	HCT1	HCT0

CSb	RS	RDb	WRb
0	1	1	0

(default: HCT [6:0] = 0_H, address: A_H)

For small panel size(row number is less than 132), this instruction is used to decide Header COM position to specify available COM drivers. The setting range is from COMA0/COMB0 ~ COMA65/COMB65. Refer to "(13) Relationship Between Logic COM Number and Physical COM Driver" for details. Note that this instruction is not used to specify a scan start position, The scan start position is decided by the "Scan Start COM 1~3".

0 ≤ HCT ≤ (132-VPC)/2

HCT6	HCT5	HCT4	HCT3	HCT2	HCT1	HCT0	Header COM
0	0	0	0	0	0	0	COMA0/COMB0
0	0	0	0	0	0	1	COMA1/COMB1
0	0	0	0	0	1	0	COMA2/COMB2
0	0	0	0	0	1	1	COMA3/COMB3
0	0	0	0	1	0	0	COMA4/COMB4
0	0	0	0	1	0	1	COMA5/COMB5
			...				...
0	1	1	1	1	1	0	COMA62/COMB62
0	1	1	1	1	1	1	COMA63/COMB63
1	0	0	0	0	0	0	COMA64/COMB64
1	0	0	0	0	0	1	COMA65/COMB65
1	0	0	0	0	1	0	Forbidden
			...				...
1	1	1	1	1	1	1	Forbidden

(12-14) Initial Display Line

Register : HST TABLE0 [BH]

D7	D6	D5	D4	D3	D2	D1	D0
HST7	HST6	HST5	HST4	HST3	HST2	HST1	HST0

CSb	RS	RDb	WRb
0	1	1	0

(default : HST[7:0] = 0_H, address: B_H)

This instruction sets the DDRAM Y address, and the addressed RAM data will be displayed by the scan start COM 1 driver. The available Y address range is from 0~131.

HST7	HST6	HST5	HST4	HST3	HST2	HST1	HST0	Y address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
0	0	0	0	0	1	0	0	4
0	0	0	0	0	1	0	1	5
				...				:
0	1	1	1	1	1	1	0	128
0	1	1	1	1	1	1	1	129
1	0	0	0	0	0	0	0	130
1	0	0	0	0	0	1	1	131
1	0	0	0	0	1	0	0	Forbidden
				...				...
1	1	1	1	1	1	1	1	Forbidden

(12-15) Scan Start COM 1

Register : SSC1 TABLE0 [CH]

D7	D6	D5	D4	D3	D2	D1	D0
SSC17	SSC16	SSC15	SSC14	SSC13	SSC12	SSC11	SSC10

CSb	RS	RDb	WRb
0	1	1	0

(default : SSC1[7:0] = 0_H, address: C_H)

Totally three partial area can be display on the screen once time. This instruction sets the logical number of the scan start COM driver for the full screen display or for the first partial display. Refer to (13) Relationship between logical COM number and physical COM driver for details. The available setting range is: $0 \leq SSC1 \leq (VPC - 1)$

(12-16) Scan Start COM 2

Register : SSC2 TABLE0 [DH]

D7	D6	D5	D4	D3	D2	D1	D0
SSC27	SSC26	SSC25	SSC24	SSC23	SSC22	SSC21	SSC20

CSb	RS	RDb	WRb
0	1	1	0

(default : SSC2[7:0] = 0_H, address: D_H)

This instruction sets the logical number of the scan start COM driver for the second partial display. Refer to (13) Relationship between logical COM number and physical COM driver for details. The available setting range is: $SSC1+PCC1 \leq SSC2 \leq (VPC - 1)$

(12-17) Line Number of Partial Display 1

Register : PCC1 TABLE0 [EH]

D7	D6	D5	D4	D3	D2	D1	D0
PCC17	PCC16	PCC15	PCC14	PCC13	PCC12	PCC11	PCC10

CSb	RS	RDb	WRb
0	1	1	0

(default : PCC1[7:0] = 0_H, address: E_H)

This instruction sets line number(DDRAM Y address range) for the first partial display. In the partial display mode, this instruction has priority over the Display Line Number(VPC) setting. PCC1+PCC2+PCC3 will be the display duty. The available setting range is: $0 \leq PCC1 \leq (VPC - SSC1)$

(12-18) Line Number of Partial Display 2

Register : PCC2 TABLE0 [FH]

D7	D6	D5	D4	D3	D2	D1	D0
PCC27	PCC26	PCC25	PCC24	PCC23	PCC22	PCC21	PCC20

CSb	RS	RDb	WRb
0	1	1	0

(default : PCC2[7:0] = 0_H, address: F_H)

This instruction sets line number(DDRAM Y address range) for the second partial display. In the partial display mode, this instruction has priority over the Display Line Number(VPC) setting. PCC1+PCC2+PCC3 will be the display duty. The available setting range is: $0 \leq PCC2 \leq (VPC - SSC2)$.

(12-19) N-Line Inversion

Register : MC TABLE1 [0H]

D7	D6	D5	D4	D3	D2	D1	D0
MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0

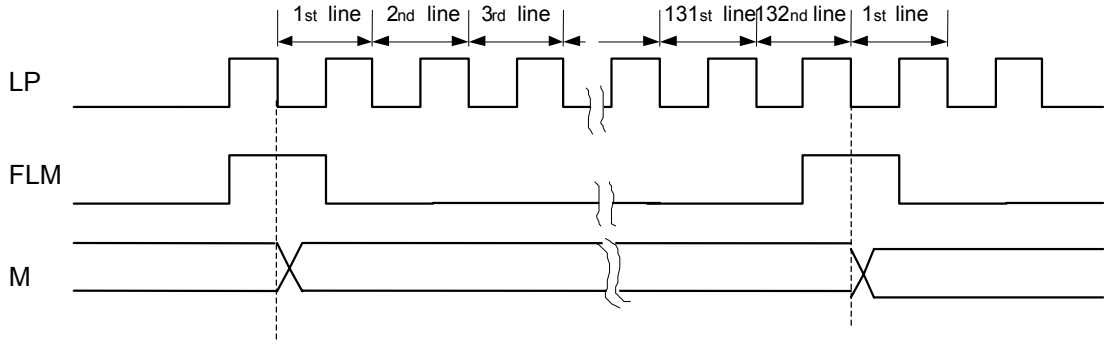
CSb	RS	RDb	WRb
0	1	1	0

(default : MC[7:0] = 0_H, address: 0_H)

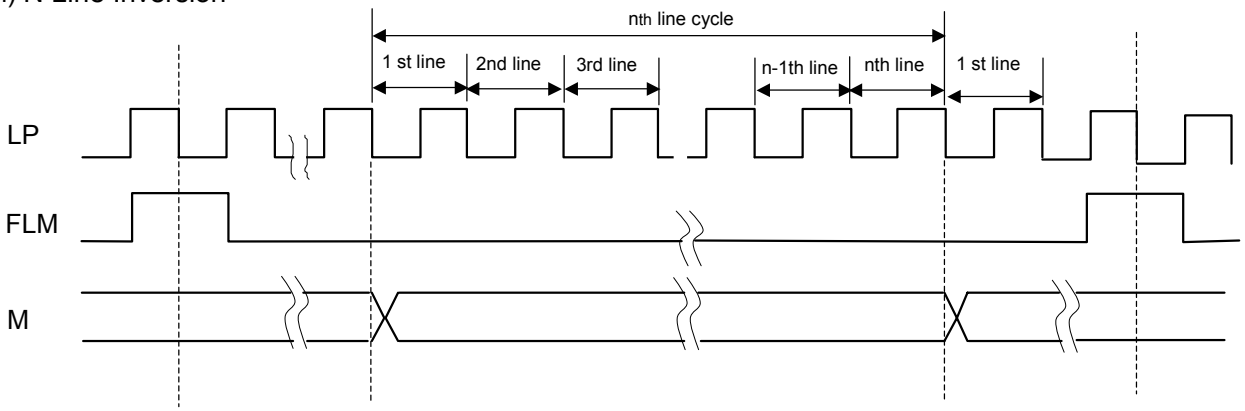
This instruction can let LCD driving signal polarity (M signal) to be alternated every N(2=<N<=132) lines. Under default setting(MC[7:0]=0H), driving signal polarity alternates every frame.

MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0	Function
0	0	0	0	0	0	0	0	Frame inversion (Default State)
0	0	0	0	0	0	0	1	2 line inversion
0	0	0	0	0	0	1	0	3 line inversion
0	0	0	0	0	0	1	1	4 line Inversion
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	1	1	132 Line Inversion
:	:	:	:	:	:	:	:	prohibited
1	0	1	1	0	0	0	0	prohibited.

(i) Frame Inversion (1/132 DUTY)



(ii) N Line Inversion



(12-20) Power Control 1

Register : TCBI TABLE1 [1H]

D7	D6	D5	D4	D3	D2	D1	D0
VGOFF	VBON	TCV1	TCV0	*	B2	B1	B0

CSb	RS	RDb	WRb
0	1	1	0

(default: VGOFF, VBON, TCV[1:0] = 0H, B[2:0] = 4H, address: 1H)

(i)VGOFF

Voltage Regulator (V_{REG} output) ON/OFF

VG OFF = 0: AMPON="1", Voltage Regulator ON

VG OFF = 1: Voltage Regulator OFF

(ii)VBON

Reference Voltage Generator (VBA output) ON/OFF

VBON = 0: Reference Voltage Circuit OFF

VBON = 1: AMPON="1" & VGOFF="0", Reference Voltage Circuit ON

(iii)TCV[1:0]

Setting temperature compensation coefficient for Reference Voltage Circuit.

TCV[1]	TCV[0]	VBA output	remark
0	0	0.0 % /°C	Default setting
0	1	- 0.13 % /°C	
1	0	- 0.20 % /°C	
1	1	- 0.24 % /°C	

(iv) B[2:0] LCD Bias Ratio

B2	B1	B0	Function
0	0	0	1/5 Bias
0	0	1	1/6 Bias
0	1	0	1/7 Bias
0	1	1	1/8 Bias
1	0	0	1/9 Bias (Initial state)
1	0	1	1/10 Bias
1	1	0	1/11 Bias
1	1	1	1/12 Bias

(12-21) Electronic Volume Control

Register: EVOL TABLE1 [2H]

D7	D6	D5	D4	D3	D2	D1	D0
*	EVOL6	EVOL5	EVOL4	EVOL3	EVOL2	EVOL1	EVOL0

CSb	RS	RDb	WRb
0	1	1	0

(default: EVOL[6:0] = 0_H, address: 2_H)

128 steps available

EVOL6	EVOL5	EVOL4	EVOL3	EVOL2	EVOL1	EVOL0	Output Voltage
0	0	0	0	0	0	0	Lower
0	0	0	0	0	0	1	
			...				...
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	Higher

V_{REG} can be calculated from the equation (1)
$V_{REG} = V_{REF} \times N$ .....(1)
(N determined by VU[2:0](boost level), RG[2:0] and GSEL bits of GVU register)

LCD driving voltage V_0 can be calculated from the equation (2)
$V0 = 0.5 \times V_{REG} + M \times (V_{REG} - 0.5\ V_{REG}) / 127$ …….....…… …….(2)
(electronic volume M determined by EVOL[6:0] bits of EVOL register)

(12-22) Display Timing Signal Monitor/PBX Palette

Register : PBX TABLE1 [3H]

D7	D6	D5	D4	D3	D2	D1	D0
MON	*	*	GS	PBX3	PBX2	PBX1	PBX0

CSb	RS	RDb	WRb
0	1	1	0

(default: MON, GS = 0_H, PBX[3:0] = 3_H, address: 3_H)

(i) MON

Setting FLM, LP and M signals output ON/OFF

MON	Function
0	FLM, LP, M signal output OFF（default）
1	FLM, LP, M signal output ON

(ii) GS, PBX[3:0]

When GS="0", palette PBX setting is available. When GS="1", PB0 is selected.

GS=1	PBX[3:0] register invalid							
GS=0	0	0	0	PBX3	PBX2	PBX1	PBX0	(Note 1)

Note 1) Under 65k colors mode , palette PBX is selected to set B data. PBX is used to display the grayscale between PB0 and PB1.

(12-23) Power Control 2

Register : POW2 TABLE1 [5H]

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	CKCONT	AMPON	HALT	DCON	RES

CSb	RS	RDb	WRb
0	1	1	0

(default: CKCONT, AMPON, HALT, DCON, RES = 0_H, address: 5_H)

(i) RES

RES = "0": Default
RES = "1": Initialization

Note 1) After initialization(RES="1"), RES bit turn to "0".
Note 2) After initialization, at least two LP signal cycles is needed to wait to execute the next instruction.

(ii) DCON

Setting voltage booster ON/OFF.

DCON= "0": voltage booster OFF
DCON= "1": voltage booster ON

(iii) HALT

Setting power save mode ON/OFF

HALT = "0": power save mode OFF(default)
HALT = "1": power save mode ON

LSI Internal status under power save mode:

a. Internal oscillator and LCD power supply is in the halted state.
b. COM/SEG outputs V_{SSH} level voltage.
c. External clock is unacceptable.
d. DDRAM data is remained
e. Instruction Register data is remained

(iv) AMPON

Using together with VGOFF and VBON bits of Power control 1register (TCBI) to set voltage converter ON/OFF.

AMPON = "0" voltage converter OFF
AMPON = "1": voltage converter ON

(v) CKCONT

Setting GCK signal and LP signal ON/OFF

CKCONT = "0": GCK and LP OFF
CKCONT = "1": GCK and LP ON

Note) NJU6854 use internal oscillator or external clock signal to generate GCK and LP signal. Not only used as display clock, GCK and LP are also used as operating clock for voltage booster. Be sure to set CKCONT="1" when voltage booster is used(DCON= "1").

(12-24) Booster Level/Amplifier Gain

Register : GVU TABLE1 [6H]

D7	D6	D5	D4	D3	D2	D1	D0
GSEL	RG2	RG1	RG0	*	VU2	VU1	VU0

CSb	RS	RDb	WRb
0	1	1	0

(default: GSEL, RG[2:0] = 0H, VU[2:0] = 0H, address: 6H)

(i) GSEL
Setting amplifier gain of VREG

GSEL = 0: Amplifier gain is determined by VU[2:0] bits as the same as the boost level.
GSEL = 1: Amplifier gain is determined by RG[2:0] bits

(ii)RG[2:0]

When GSEL="1", the relationship between RG[2:0] and amplifier gain is showed as below.

GSEL = '0'			GSEL = '1'			Amplifier gain (N)	Remark
VU2	VU1	VU0	RG2	RG1	RG0		
0	0	0				-	default VU[2:0]
0	0	1				2	
0	1	0	0	0	0	3	default RG[2:0]
0	1	1	0	0	1	4	
1	0	0	0	1	0	5	
1	0	1	0	1	1	6	
			1	0	0	6.45	
			1	0	1	7	
			1	1	0	7.3	
			1	1	1	8.0	
1	1	0				-	
1	1	1				-	

(iii) VU[2:0]

Setting boost level. And when GSEL="0", also setting amplifier gain of V_{REG}.

VU2	VU1	VU0	Function
0	0	0	No Boost Up
0	0	1	2 Times Boost Up
0	1	0	3 Times Boost Up
0	1	1	4 Times Boost Up
1	0	0	5 Times Boost Up
1	0	1	6 Times Boost Up
1	1	0	Forbidden
1	1	1	Forbidden

(12-25) Voltage Booster Clock

Register : BCK TABLE1 [7H]

D7	D6	D5	D4	D3	D2	D1	D0
BCKS	BCKG	*	*	BCK3	BCK2	BCK1	BCK0

CSb	RS	RDb	WRb
0	1	1	0

(default: BCKS, BCKG, BCK[3:0] = 0_H, address: 7_H)

Note) NJU6854 use internal oscillator or external clock to generate GCK and LP signal. Not only used as display clock, GCK and LP are also used as operating clock for voltage booster. Be sure to set CKCONT="1" when voltage booster is used(DCON= "1").

(i) BCK[3:0]

Setting dividing ratio for the oscillating signal or external clock to generate GCK and LP.

BCK3	BCK2	BCK1	BCK0	Function
0	0	0	0	1/1 Dividing (There is a restriction)
0	0	0	1	1/2 Dividing
0	0	1	0	1/3 Dividing
0	0	1	1	1/4 Dividing
0	1	0	0	1/5 Dividing
...				...
1	0	1	1	1/12 Dividing
1	1	0	0	1/13 Dividing
1	1	0	1	1/14 Dividing
1	1	1	0	1/15 Dividing
1	1	1	1	1/16 Dividing

Note) When BCK[3:0]=[0000, MDIV[2:0]=[000] and BCKS="1" settings are prohibited.

(ii) BCKG

When BCKG="1", MDIV output signal is equally divided into 8 time slots.

(iii) BCKS

Selecting divided clock signal.

BCKS = "0" : LP signal

BCKS = "1" : BCKG signal

Note) There is a trade-off relationship between voltage booster driving capability and current consumption, so the optimal booster clock shall be decided by your LCD module.

(12-26) Display Control

Register : Display TABLE1 [8H]

D7	D6	D5	D4	D3	D2	D1	D0
REF	SWAP	*	SHIFT1	SHIFT0	TBC	TEN	ON/OFF

CSb	RS	RDb	WRb
0	1	1	0

(default: REF, SWAP, SHIFT[1:0], TBC, TEN, ON/OFF = 0_H, address: 8_H)

(i) ON/OFF

Display Control ON/OFF

ON/OFF = "0": Display OFF

ON/OFF = "1": Display ON

(ii) TEN

TEN = "0": Normal

TEN = "1": Independent from DDRAM data, pixels are forced to be ON or OFF.

(iii) TBC(TEN = "1")

TBC = "0" : All pixels ON

TBC = "1" : All pixels OFF

(iv) SHIFT[1:0]

Setting the shift direction of the COM drivers' output.

(v) SWAP

Switching corresponding relationship between DDRAM data and palette A, B, C. This bit shall be set before DDRAM data writing.

SWAP = "0": Normal

SWAP = "1": SWAP

(vi) REF

Reversing the shift direction of SEG drivers' output by redirecting X address. This bit shall be set before DDRAM data writing.

REF = "0": Normal

REF = "1": Opposite Direction

(12-27) PWM Control

Register : PWM TABLE1 [9H]

D7	D6	D5	D4	D3	D2	D1	D0
*	*	PWMC1	PWMC0	PWMB1	PWMB0	PWMA1	PWMA0

CSb	RS	RDb	WRb
0	1	1	0

(default: PWMC[1:0], PWMB[1:0],PWMA[1:0] = 0_H, address: 9_H)

(i) PWMC[1:0], PWMB[1:0], PWMA[1:0]
Setting PWM signals for SEGA, SEGB, and SEGC respectively.

SEGAi (i=0~131)

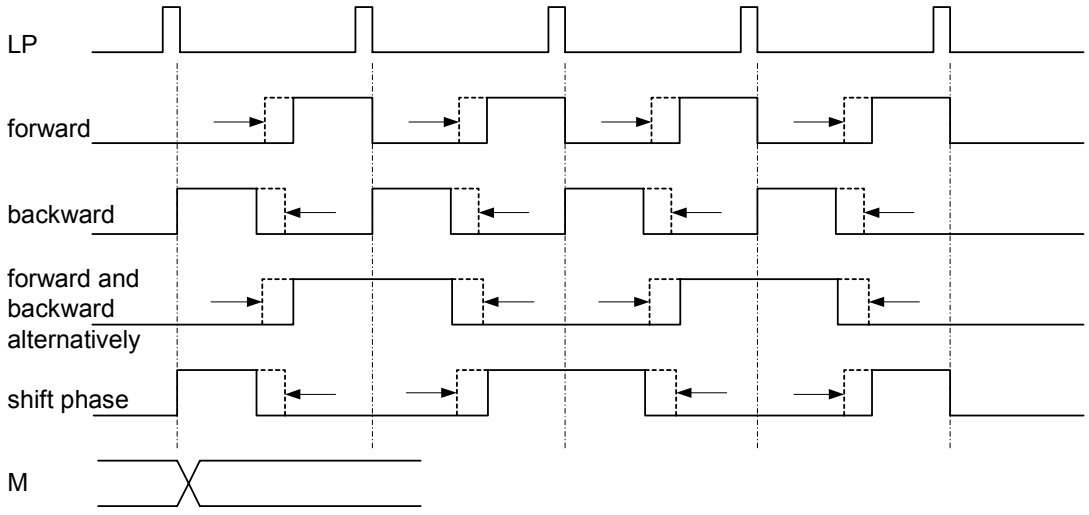
PWMA1	PWMA0	Output Timing
0	0	Forward PWM
0	1	Backward PWM
1	0	Forward and Backward alternately
1	1	Shift Phase

SEGBi (i=0~131)

PWMB1	PWMB0	Output Timing
0	0	Forward PWM
0	1	Backward PWM
1	0	Forward and Backward alternately
1	1	Shift Phase

SEGCi (i=0~131)

PWMC1	PWMC0	Output Timing
0	0	Forward PWM
0	1	Backward PWM
1	0	Forward and Backward alternately
1	1	Shift Phase



(12-28) Three Partial Display Areas/ LED Driver Control/REV Bit

Register : ECONT TABLE1 [AH]

D7	D6	D5	D4	D3	D2	D1	D0
TST0	EN3PTL	ENLED	REV	LED13	LED12	LED11	LED10

CSb	RS	RDb	WRb
0	1	1	0

(default: TST0, EN3PTL, ENLED, REV, LED1[3:0] = 0_H, address: A_H)

(i) TST0

For maker testing, usually set to ”0”.

(ii) EN3PTL

When EN3PTL=”1”, three specified partial areas can be displayed through setting SSC1[7:0]~SSC3[7:0] and PCC1[7:0]~PCC3[7:0]. If setting EN3PTL=”0”, one or two partial area can be displayed.

(iii) ENLED

When ENLED=”1”, data saved at LED1[3:0] can be used to control white LED through control port(LDAT, LSCK, LREQ, LRESB)

ENLED = 0 : LDAT, LSCK, LREQ, LRESB ports invalid (high impedance)

ENLED = 1 : LDAT, LSCK, LREQ, LRESB ports valid.

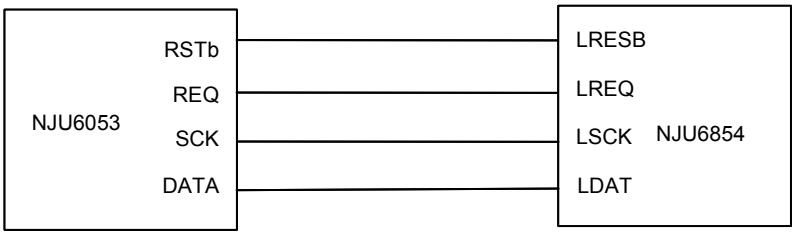
(iv) LED1 [3:0]

When ENLED=”1”, white LED control ports (LDAT, LSCK, LREQ, LRESB) are valid, LED control signal output from LDAT, LSCK, LREQ and LRESB to LED10, LED11, LED12 and LED13 respectively.

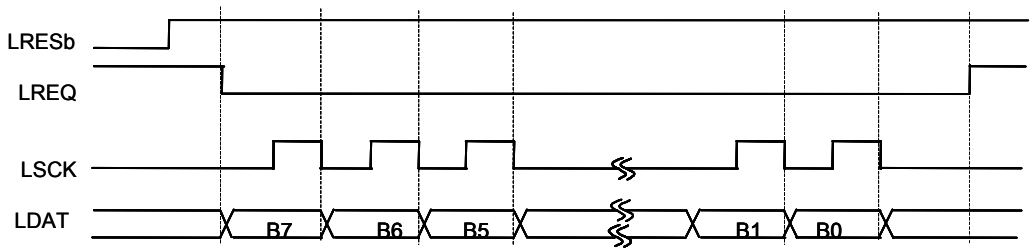
Concerning white LED driver, please refer to NJRC white LED controller series (NJU6051/52/53). Besides, the above mentioned bits and ports can be used as general-purpose ports too.

Note) For NJRC white LED driver, data pin state will be changed according to request pin. When request pin is “L”, data pin of white LED driver is in input state, and when request pin is “H”, data pin become output state. when LREQ pin of NJU6854 is “L”, LDAT pin output signals, and when LREQ is “H”, LDAT is in input state. So, if LDAT, LSCK, LREQ and LRESB are used as common ports, please pay attention to this point. LSCK, LREQ and LRESB pins can be used as 3-bit general-purpose ports too.

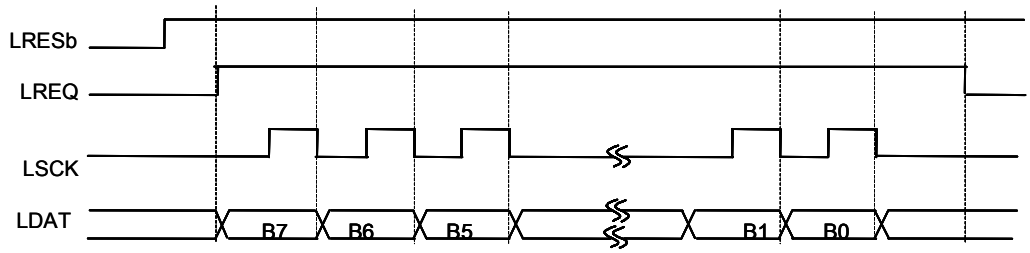
Example of connection with NJU6053



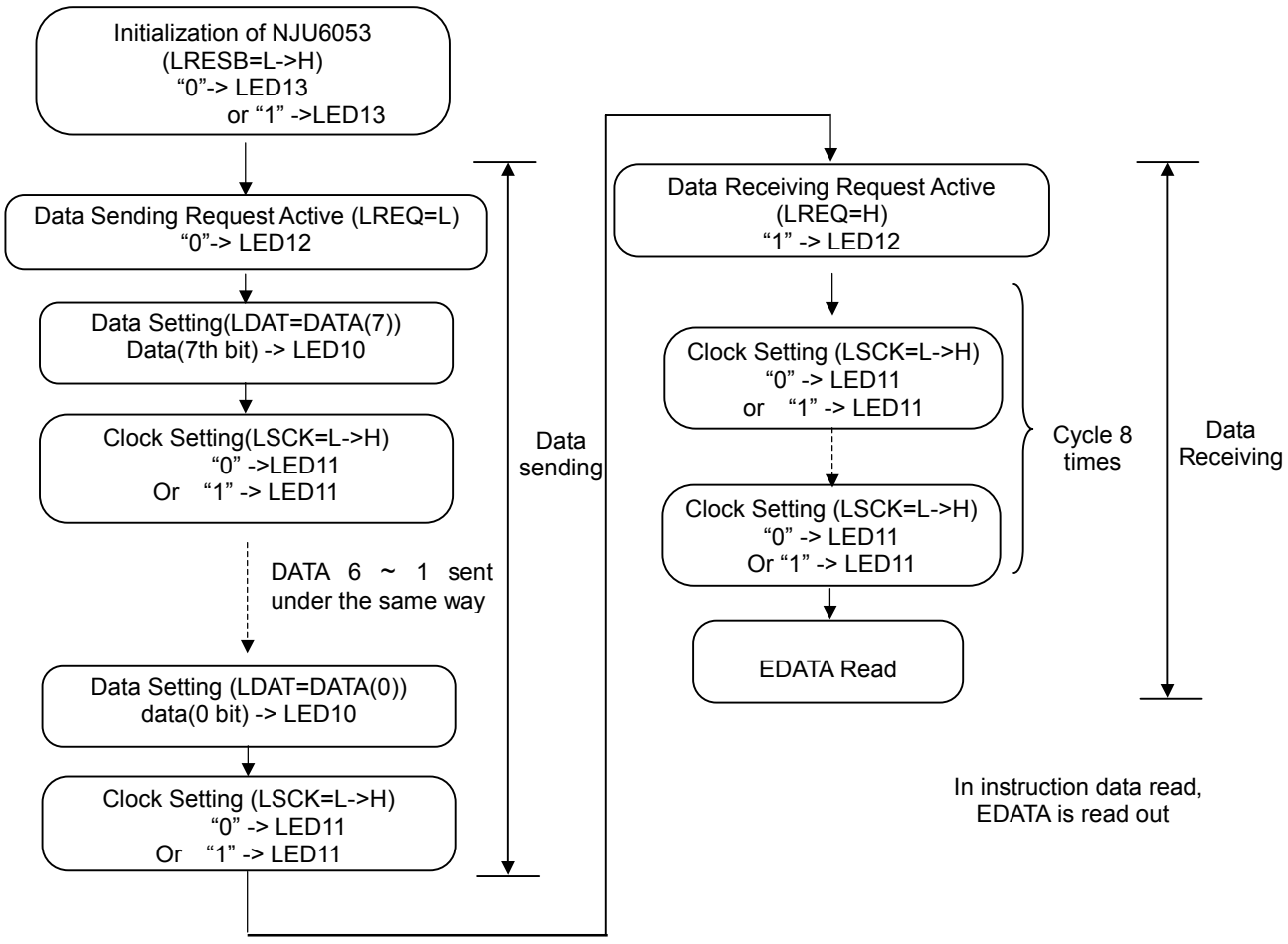
Timing Sequence of data sending



Timing Sequence of data receiving



Follow Chart of NJU6053 Operation



(v) REV

Without changing data in DDRAM, pixel display state can be inverted

REV = "0": data="1" pixel ON (Normal)

REV = "1": data="0" pixel ON (Reversed)

(12-29) Discharge ON/OFF

Register : DIS TABLE1 [BH]

D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	*	*	*	DIS2	DIS1

CSb	RS	RDb	WRb
0	1	1	0

(default: DIS[2:1] = 0_H, address: B_H)

(i) DIS1

If DIS1="1", the capacitors connected to V_0~V_4 pins discharge.

DIS1 = "0": Discharge OFF

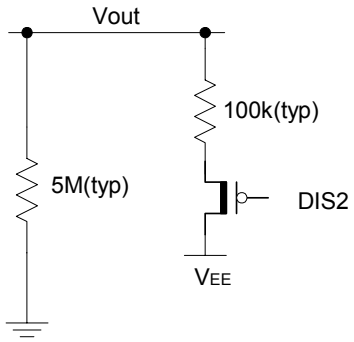
DIS1 = "1": Discharge ON

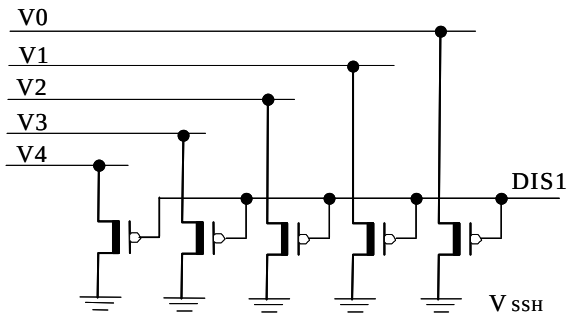
(ii) DIS2

If DIS2="1", the capacitor connected to V_{OUT} pin discharge

DIS2 = "0": discharge OFF

DIS2 = "1": discharge ON





(12-30) LED Driver Data

Register : EDATA TABLE1 [CH]

D7	D6	D5	D4	D3	D2	D1	D0
LED27	LED26	LED25	LED24	LED23	LED22	LED21	LED20

CSb	RS	RDb	WRb
0	1	1	0

(default: LED2[7:0] = 0_H, address: C_H)

(i)LED2[7:0]

Data from NJRC white LED driver(NJU6051/52/53) is saved in this register.

(12-31) Instruction Table/Address

Register : RA TABLE1 [DH]

D7	D6	D5	D4	D3	D2	D1	D0
RSS	RA6	RA5	RA4	RA3	RA2	RA1	RA0

CSb	RS	RDb	WRb
0	1	1	0

(default: RA[6:0] = 0_H, address: D_H)

RA[6:4] : Instruction table selection

RA6	RA5	RA4	Table indicator
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

RA[3:0] :Register address selection during direct access, or increment number selection in auto increment mode.

RA3	RA2	RA1	RA0	Direct access (address selection)	Auto increment (setting increment number)
0	0	0	0	0_H	1
0	0	0	1	1_H	2
0	0	1	0	2_H	3
0	0	1	1	3_H	4
0	1	0	0	4_H	5
0	1	0	1	5_H	6
0	1	1	0	6_H	7
0	1	1	1	7_H	8
...				...	...
1	0	1	1	B_H	12
1	1	0	0	C_H	13
1	1	0	1	D_H	14
1	1	1	0	E_H	15
1	1	1	1	F_H	0

RSS: RSS = "1": increment number in auto increment mode.
RSS = "0": register address selection for direct access

(12-32) Scan Start COM 3

Register : SSC3 TABLE1 [EH]

D7	D6	D5	D4	D3	D2	D1	D0
SSC37	SSC36	SSC35	SSC34	SSC33	SSC32	SSC31	SSC30

CSb	RS	RDb	WRb
0	1	1	0

(default: SSC3[7:0] = 0_H, address: E_H)

This instruction sets the logical number of the scan start COM driver for the third partial display, and the setting method just as of the Scan Start COM 1 or 2. This instruction can not be used with normal display and single partial display. When EN3PTL = "1", the setting is valid.

Range: SSC2 + PCC2 ≤ SSC3 ≤ (VPC – 1)

(12-33) Line Number of Partial Display 3

Register : PCC3 TABLE1 [FH]

D7	D6	D5	D4	D3	D2	D1	D0
PCC37	PCC36	PCC35	PCC34	PCC33	PCC32	PCC31	PCC30

CSb	RS	RDb	WRb
0	1	1	0

(default: PCC3[7:0] = 0_H, address: F_H)

This instruction set line number(DDRAM Y address range) for the third partial display area. In the partial display mode, this instruction has priority over the Display Line Number(VPC) setting. PCC1+PCC2+PCC3 will be the display duty. When EN3PTL = "1", the setting is valid

Range: 0 ≤ PCC3 ≤ (VPC – SSC3)

(12-34) Grayscale Palette (PA0~PA31, PB0~PB31, PC0~PC31)

Register : PA0 TABLE2 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA06	PA05	PA04	PA03	PA02	PA01	PA00

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA0[6:0] = 0_H, Register Address: 0_H)

Register : PA1 TABLE2 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA16	PA15	PA14	PA13	PA12	PA11	PA10

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA1[6:0] = 6_H, Register Address: 1_H)

Register : PA2 TABLE2 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA26	PA25	PA24	PA23	PA22	PA21	PA20

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA2[6:0] = A_H, Register Address: 2_H)

Register : PA3 TABLE2 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA36	PA35	PA34	PA33	PA32	PA31	PA30

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA3[6:0] = E_H, Register Address: 3_H)

Register : PA4 TABLE2 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA46	PA45	PA44	PA43	PA42	PA41	PA40

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA4[6:0] = 12_H, Register Address: 4_H)

Register : PA5 TABLE2 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA56	PA55	PA54	PA53	PA52	PA51	PA50

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA5[6:0] = 16_H, Register Address: 5_H)

Register : PA6 TABLE2 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA66	PA65	PA64	PA63	PA62	PA61	PA60

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA6[6:0] = $1A_H$, Register Address: 6_H)

Register : PA7 TABLE2 [7_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA76	PA75	PA74	PA73	PA72	PA71	PA70

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA7[6:0] = $1E_H$, Register Address: 7_H)

Register : PA8 TABLE2 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA86	PA85	PA84	PA83	PA82	PA81	PA80

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA8[6:0] = 22_H, Register Address: 8_H)

Register : PA9 TABLE2 [9_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA96	PA95	PA94	PA93	PA92	PA91	PA90

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA9[6:0] = 26_H, Register Address: 9_H)

Register : PA10 TABLE2 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA106	PA105	PA104	PA103	PA102	PA101	PA100

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA10[6:0] = $2A_H$, Register Address: A_H)

Register : PA11 TABLE2 [B_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA116	PA115	PA114	PA113	PA112	PA111	PA110

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA11[6:0] = $2E_H$, Register Address: B_H)

Register : PA12 TABLE2 [C_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA126	PA125	PA124	PA123	PA122	PA121	PA120

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA12[6:0] = 32_H, Register Address: C_H)

Register : PA13 TABLE2 [D_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA136	PA135	PA134	PA133	PA132	PA131	PA130

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA13[6:0] = 36_H, Register Address: D_H)

Register : PA14 TABLE2 [E_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA146	PA145	PA144	PA143	PA142	PA141	PA140

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA14[6:0] = $3A_H$, Register Address: E_H)

Register : PA15 TABLE2 [F_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA156	PA155	PA154	PA153	PA152	PA151	PA150

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA15[6:0] = $3E_H$, Register Address: F_H)

Register : PA16 TABLE3 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA166	PA165	PA164	PA163	PA162	PA161	PA160

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA16[6:0] = 42_H, Register Address: 0_H)

Register : PA17 TABLE3 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA176	PA175	PA174	PA173	PA172	PA171	PA170

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA17[6:0] = 46_H, Register Address: 1_H)

Register : PA18 TABLE3 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA186	PA185	PA184	PA183	PA182	PA181	PA180

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA18[6:0] = $4A_H$, Register Address: 2_H)

Register : PA19 TABLE3 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA196	PA195	PA194	PA193	PA192	PA191	PA190

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA19[6:0] = $4E_H$, Register Address: 3_H)

Register : PA20 TABLE3 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA206	PA205	PA204	PA203	PA202	PA201	PA200

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA20[6:0] = 52_H, Register Address: 4_H)

Register : PA21 TABLE3 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA216	PA215	PA214	PA213	PA212	PA211	PA210

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA21[6:0] = 56_H, Register Address: 5_H)

Register : PA22 TABLE3 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA226	PA225	PA224	PA223	PA222	PA221	PA220

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA22[6:0] = $5A_H$, Register Address: 6_H)

Register : PA23 TABLE3 [7_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA236	PA235	PA234	PA233	PA232	PA231	PA230

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA23[6:0] = $5E_H$, Register Address: 7_H)

Register : PA24 TABLE3 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA246	PA245	PA244	PA243	PA242	PA241	PA240

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA24[6:0] = 62_H, Register Address: 8_H)

Register : PA25 TABLE3 [9_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA256	PA255	PA254	PA253	PA252	PA251	PA250

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA25[6:0] = 66_H, Register Address: 9_H)

Register : PA26 TABLE3 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA266	PA265	PA264	PA263	PA262	PA261	PA260

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA26[6:0] = $6A_H$, Register Address: A_H)

Register : PA27 TABLE3 [B_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA276	PA275	PA274	PA273	PA272	PA271	PA270

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA27[6:0] = $6E_H$, Register Address: B_H)

Register : PA28 TABLE3 [C_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA286	PA285	PA284	PA283	PA282	PA281	PA280

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA28[6:0] = 72_H, Register Address: C_H)

Register : PA29 TABLE3 [D_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA296	PA295	PA294	PA293	PA292	PA291	PA290

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA29[6:0] = 76_H, Register Address: D_H)

Register : PA30 TABLE3 [E_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA306	PA305	PA304	PA303	PA302	PA301	PA300

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA30[6:0] = $7A_H$, Register Address: E_H)

Register : PA31 TABLE3 [F_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PA316	PA315	PA314	PA313	PA312	PA311	PA310

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PA31[6:0] = $7F_H$, Register Address: F_H)

Register : PB0 TABLE4 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB06	PB05	PB04	PB03	PB02	PB01	PB00

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB0[6:0] = 0_H, Register Address: 0_H)

Register : PB1 TABLE4 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB16	PB15	PB14	PB13	PB12	PB11	PB10

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB1[6:0] = 6_H, Register Address: 1_H)

Register : PB2 TABLE4 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB26	PB25	PB24	PB23	PB22	PB21	PB20

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB2[6:0] = A_H, Register Address: 2_H)

Register : PB3 TABLE4 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB36	PB35	PB34	PB33	PB32	PB31	PB30

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB3[6:0] = E_H, Register Address: 3_H)

Register : PB4 TABLE4 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB46	PB45	PB44	PB43	PB42	PB41	PB40

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB4[6:0] = 12_H, Register Address: 4_H)

Register : PB5 TABLE4 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB56	PB55	PB54	PB53	PB52	PB51	PB50

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB5[6:0] = 16_H, Register Address: 5_H)

Register : PB6 TABLE4 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB66	PB65	PB64	PB63	PB62	PB61	PB60

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB6[6:0] = $1A_H$, Register Address: 6_H)

Register : PB7 TABLE4 [7_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB76	PB75	PB74	PB73	PB72	PB71	PB70

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB7[6:0] = $1E_H$, Register Address: 7_H)

Register : PB8 TABLE4 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB86	PB85	PB84	PB83	PB82	PB81	PB80

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB8[6:0] = 22_H, Register Address: 8_H)

Register : PB9 TABLE4 [9_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB96	PB95	PB94	PB93	PB92	PB91	PB90

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB9[6:0] = 26_H, Register Address: 9_H)

Register : PB10 TABLE4 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB106	PB105	PB104	PB103	PB102	PB101	PB100

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB10[6:0] = $2A_H$, Register Address: A_H)

Register : PB11 TABLE4 [B_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB116	PB115	PB114	PB113	PB112	PB111	PB110

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB11[6:0] = $2E_H$, Register Address: B_H)

Register : PB12 TABLE4 [C_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB126	PB125	PB124	PB123	PB122	PB121	PB120

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB12[6:0] = 32_H, Register Address: C_H)

Register : PB13 TABLE4 [D_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB136	PB135	PB134	PB133	PB132	PB131	PB130

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB13[6:0] = 36_H, Register Address: D_H)

Register : PB14 TABLE4 [E_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB146	PB145	PB144	PB143	PB142	PB141	PB140

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB14[6:0] = $3A_H$, Register Address: E_H)

Register : PB15 TABLE4 [F_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB156	PB155	PB154	PB153	PB152	PB151	PB150

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB15[6:0] = $3E_H$, Register Address: F_H)

Register : PB16 TABLE5 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB166	PB165	PB164	PB163	PB162	PB161	PB160

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB16[6:0] = 42_H, Register Address: 0_H)

Register : PB17 TABLE5 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB176	PB175	PB174	PB173	PB172	PB171	PB170

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB17[6:0] = 46_H, Register Address: 1_H)

Register : PB18 TABLE5 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB186	PB185	PB184	PB183	PB182	PB181	PB180

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB18[6:0] = $4A_H$, Register Address: 2_H)

Register : PB19 TABLE5 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB196	PB195	PB194	PB193	PB192	PB191	PB190

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB19[6:0] = $4E_H$, Register Address: 3_H)

Register : PB20 TABLE5 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB206	PB205	PB204	PB203	PB202	PB201	PB200

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB20[6:0] = 52_H, Register Address: 4_H)

Register : PB21 TABLE5 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB216	PB215	PB214	PB213	PB212	PB211	PB210

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB21[6:0] = 56_H, Register Address: 5_H)

Register : PB22 TABLE5 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB226	PB225	PB224	PB223	PB222	PB221	PB220

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB22[6:0] = $5A_H$, Register Address: 6_H)

Register : PB23 TABLE5 [7_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB236	PB235	PB234	PB233	PB232	PB231	PB230

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB23[6:0] = $5E_H$, Register Address: 7_H)

Register : PB24 TABLE5 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB246	PB245	PB244	PB243	PB242	PB241	PB240

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB24[6:0] = 62_H, Register Address: 8_H)

Register : PB25 TABLE5 [9_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB256	PB255	PB254	PB253	PB252	PB251	PB250

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB25[6:0] = 66_H, Register Address: 9_H)

Register : PB26 TABLE5 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB266	PB265	PB264	PB263	PB262	PB261	PB260

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB26[6:0] = $6A_H$, Register Address: A_H)

Register : PB27 TABLE5 [B_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB276	PB275	PB274	PB273	PB272	PB271	PB270

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB27[6:0] = $6E_H$, Register Address: B_H)

Register : PB28 TABLE5 [C_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB286	PB285	PB284	PB283	PB282	PB281	PB280

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB28[6:0] = 72_H, Register Address: C_H)

Register : PB29 TABLE5 [D_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB296	PB295	PB294	PB293	PB292	PB291	PB290

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB29[6:0] = 76_H, Register Address: D_H)

Register : PB30 TABLE5 [E_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB306	PB305	PB304	PB303	PB302	PB301	PB300

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB30[6:0] = $7A_H$, Register Address: E_H)

Register : PB31 TABLE5 [F_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PB316	PB315	PB314	PB313	PB312	PB311	PB310

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PB31[6:0] = $7F_H$, Register Address: F_H)

Register : PC0 TABLE6 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC06	PC05	PC04	PC03	PC02	PC01	PC00

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC0[6:0] = 0_H, Register Address: 0_H)

Register : PC1 TABLE6 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC16	PC15	PC14	PC13	PC12	PC11	PC10

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC1[6:0] = 6_H, Register Address: 1_H)

Register : PC2 TABLE6 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC26	PC25	PC24	PC23	PC22	PC21	PC20

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC2[6:0] = A_H, Register Address: 2_H)

Register : PC3 TABLE6 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC36	PC35	PC34	PC33	PC32	PC31	PC30

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC3[6:0] = E_H, Register Address: 3_H)

Register : PC4 TABLE6 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC46	PC45	PC44	PC43	PC42	PC41	PC40

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC4[6:0] = 12_H, Register Address: 4_H)

Register : PC5 TABLE6 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC56	PC55	PC54	PC53	PC52	PC51	PC50

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC5[6:0] = 16_H, Register Address: 5_H)

Register : PC6 TABLE6 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC66	PC65	PC64	PC63	PC62	PC61	PC60

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC6[6:0] = $1A_H$, Register Address: 6_H)

Register : PC7 TABLE6 [7_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC76	PC75	PC74	PC73	PC72	PC71	PC70

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC7[6:0] = $1E_H$, Register Address: 7_H)

Register : PC8 TABLE6 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC86	PC85	PC84	PC83	PC82	PC81	PC80

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC8[6:0] = 22_H, Register Address: 8_H)

Register : PC9 TABLE6 [9_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC96	PC95	PC94	PC93	PC92	PC91	PC90

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC9[6:0] = 26_H, Register Address: 9_H)

Register : PC10 TABLE6 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC106	PC105	PC104	PC103	PC102	PC101	PC100

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC10[6:0] = $2A_H$, Register Address: A_H)

Register : PC11 TABLE6 [B_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC116	PC115	PC114	PC113	PC112	PC111	PC110

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC11[6:0] = $2E_H$, Register Address: B_H)

Register : PC12 TABLE6 [C_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC126	PC125	PC124	PC123	PC122	PC121	PC120

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC12[6:0] = 32_H, Register Address: C_H)

Register : PC13 TABLE6 [D_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC136	PC135	PC134	PC133	PC132	PC131	PC130

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC13[6:0] = 36_H, Register Address: D_H)

Register : PC14 TABLE6 [E_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC146	PC145	PC144	PC143	PC142	PC141	PC140

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC14[6:0] = $3A_H$, Register Address: E_H)

Register : PC15 TABLE6 [F_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC156	PC155	PC154	PC153	PC152	PC151	PC150

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC15[6:0] = $3E_H$, Register Address: F_H)

Register : PC16 TABLE7 [0_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC166	PC165	PC164	PC163	PC162	PC161	PC160

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC16[6:0] = 42_H, Register Address: 0_H)

Register : PC17 TABLE7 [1_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC176	PC175	PC174	PC173	PC172	PC171	PC170

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC17[6:0] = 46_H, Register Address: 1_H)

Register : PC18 TABLE7 [2_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC186	PC185	PC184	PC183	PC182	PC181	PC180

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC18[6:0] = $4A_H$, Register Address: 2_H)

Register : PC19 TABLE7 [3_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC196	PC195	PC194	PC193	PC192	PC191	PC190

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC19[6:0] = $4E_H$, Register Address: 3_H)

Register : PC20 TABLE7 [4_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC206	PC205	PC204	PC203	PC202	PC201	PC200

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC20[6:0] = 52_H, Register Address: 4_H)

Register : PC21 TABLE7 [5_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC216	PC215	PC214	PC213	PC212	PC211	PC210

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC21[6:0] = 56_H, Register Address: 5_H)

Register : PC22 TABLE7 [6_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC226	PC225	PC224	PC223	PC222	PC221	PC220

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC22[6:0] = $5A_H$, Register Address: 6_H)

Register : PC23 TABLE7 [7_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC236	PC235	PC234	PC233	PC232	PC231	PC230

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC23[6:0] = $5E_H$, Register Address: 7_H)

Register : PC24 TABLE7 [8_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC246	PC245	PC244	PC243	PC242	PC241	PC240

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC24[6:0] = 62_H, Register Address: 8_H)

Register : PC25 TABLE7 [9_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC256	PC255	PC254	PC253	PC252	PC251	PC250

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC25[6:0] = 66_H, Register Address: 9_H)

Register : PC26 TABLE7 [A_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC266	PC265	PC264	PC263	PC262	PC261	PC260

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC26[6:0] = $6A_H$, Register Address: A_H)

Register : PC27 TABLE7 [B_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC276	PC275	PC274	PC273	PC272	PC271	PC270

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC27[6:0] = $6E_H$, Register Address: B_H)

Register : PC28 TABLE7 [C_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC286	PC285	PC284	PC283	PC282	PC281	PC280

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC28[6:0] = 72_H, Register Address: C_H)

Register : PC29 TABLE7 [D_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC296	PC295	PC294	PC293	PC292	PC291	PC290

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC29[6:0] = 76_H, Register Address: D_H)

Register : PC30 TABLE7 [E_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC306	PC305	PC304	PC303	PC302	PC301	PC300

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC30[6:0] = $7A_H$, Register Address: E_H)

Register : PC31 TABLE8 [F_H]

D7	D6	D5	D4	D3	D2	D1	D0
*	PC316	PC315	PC314	PC313	PC312	PC311	PC310

CSb	RS	RDb	WRb
0	1	1	0

(Initialization: PC31[6:0] = $7F_H$, Register Address: F_H)

65k-color Mode(32 Grayscale from 128 Levels, PWM1=1, PWM0=1)

[Three groups of palettes Aj, Bj and Cj (j=0~31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks(2)
0 0 0 0 0 0 0	0/127	Palette 0 initial value[6:0]
0 0 0 0 0 0 1	1/127	
0 0 0 0 0 1 0	2/127	
0 0 0 0 0 1 1	3/127	Palette X initial value [6:0](1)
0 0 0 0 1 0 0	4/127	
0 0 0 0 1 0 1	5/127	
0 0 0 0 1 1 0	6/127	Palette 1 initial value[6:0]
0 0 0 0 1 1 1	7/127	
0 0 0 1 0 0 0	8/127	
0 0 0 1 0 0 1	9/127	
0 0 0 1 0 1 0	10/127	Palette 2 initial value[6:0]
0 0 0 1 0 1 1	11/127	
0 0 0 1 1 0 0	12/127	
0 0 0 1 1 0 1	13/127	
0 0 0 1 1 1 0	14/127	Palette 3 initial value[6:0]
0 0 0 1 1 1 1	15/127	
0 0 1 0 0 0 0	16/127	
0 0 1 0 0 0 1	17/127	
0 0 1 0 0 1 0	18/127	Palette 4 initial value[6:0]
0 0 1 0 0 1 1	19/127	
0 0 1 0 1 0 0	20/127	
0 0 1 0 1 0 1	21/127	
0 0 1 0 1 1 0	22/127	Palette 5 initial value[6:0]
0 0 1 0 1 1 1	23/127	
0 0 1 1 0 0 0	24/127	
0 0 1 1 0 0 1	25/127	
0 0 1 1 0 1 0	26/127	Palette 6 initial value[6:0]
0 0 1 1 0 1 1	27/127	
0 0 1 1 1 0 0	28/127	
0 0 1 1 1 0 1	29/127	
0 0 1 1 1 1 0	30/127	Palette 7 initial value[6:0]
0 0 1 1 1 1 1	31/127	
0 1 0 0 0 0 0	32/127	
0 1 0 0 0 0 1	33/127	
0 1 0 0 0 1 0	34/127	Palette 8 initial value[6:0]
0 1 0 0 0 1 1	35/127	
0 1 0 0 1 0 0	36/127	
0 1 0 0 1 0 1	37/127	
0 1 0 0 1 1 0	38/127	Palette 9 initial value[6:0]
0 1 0 0 1 1 1	39/127	
0 1 0 1 0 0 0	40/127	
0 1 0 1 0 0 1	41/127	
0 1 0 1 0 1 0	42/127	Palette 10 initial value[6:0]
0 1 0 1 0 1 1	43/127	
0 1 0 1 1 0 0	44/127	
0 1 0 1 1 0 1	45/127	
0 1 0 1 1 1 0	46/127	Palette 11 initial value[6:0]
0 1 0 1 1 1 1	47/127	
0 1 1 0 0 0 0	48/127	
0 1 1 0 0 0 1	49/127	
0 1 1 0 0 1 0	50/127	Palette 12 initial value[6:0]
0 1 1 0 0 1 1	51/127	
0 1 1 0 1 0 0	52/127	
0 1 1 0 1 0 1	53/127	
0 1 1 0 1 1 0	54/127	Palette 13 initial value[6:0]
0 1 1 0 1 1 1	55/127	
0 1 1 1 0 0 0	56/127	
0 1 1 1 0 0 1	57/127	
0 1 1 1 0 1 0	58/127	Palette 14 initial value[6:0]
0 1 1 1 0 1 1	59/127	
0 1 1 1 1 0 0	60/127	
0 1 1 1 1 0 1	61/127	
0 1 1 1 1 1 0	62/127	Palette 15 initial value[6:0]
0 1 1 1 1 1 1	63/127	

Palette	Grayscale level	Remarks(2)
1 0 0 0 0 0 0	64/127	
1 0 0 0 0 0 1	65/127	
1 0 0 0 0 1 0	66/127	Palette 16 initial value[6:0]
1 0 0 0 0 1 1	67/127	
1 0 0 0 1 0 0	68/127	
1 0 0 0 1 0 1	69/127	
1 0 0 0 1 1 0	70/127	Palette 17 initial value[6:0]
1 0 0 0 1 1 1	71/127	
1 0 0 1 0 0 0	72/127	
1 0 0 1 0 0 1	73/127	
1 0 0 1 0 1 0	74/127	Palette 18 initial value[6:0]
1 0 0 1 0 1 1	75/127	
1 0 0 1 1 0 0	76/127	
1 0 0 1 1 0 1	77/127	
1 0 0 1 1 1 0	78/127	Palette 19 initial value[6:0]
1 0 0 1 1 1 1	79/127	
1 0 1 0 0 0 0	80/127	
1 0 1 0 0 0 1	81/127	
1 0 1 0 0 1 0	82/127	Palette 20 initial value[6:0]
1 0 1 0 0 1 1	83/127	
1 0 1 0 1 0 0	84/127	
1 0 1 0 1 0 1	85/127	
1 0 1 0 1 1 0	86/127	Palette 21 initial value[6:0]
1 0 1 0 1 1 1	87/127	
1 0 1 1 0 0 0	88/127	
1 0 1 1 0 0 1	89/127	
1 0 1 1 0 1 0	90/127	Palette 22 initial value[6:0]
1 0 1 1 0 1 1	91/127	
1 0 1 1 1 0 0	92/127	
1 0 1 1 1 0 1	93/127	
1 0 1 1 1 1 0	94/127	Palette 23 initial value[6:0]
1 0 1 1 1 1 1	95/127	
1 1 0 0 0 0 0	96/127	
1 1 0 0 0 0 1	97/127	
1 1 0 0 0 1 0	98/127	Palette 24 initial value[6:0]
1 1 0 0 0 1 1	99/127	
1 1 0 0 1 0 0	100/127	
1 1 0 0 1 0 1	101/127	
1 1 0 0 1 1 0	102/127	Palette 25 initial value[6:0]
1 1 0 0 1 1 1	103/127	
1 1 0 1 0 0 0	104/127	
1 1 0 1 0 0 1	105/127	
1 1 0 1 0 1 0	106/127	Palette 26 initial value[6:0]
1 1 0 1 0 1 1	107/127	
1 1 0 1 1 0 0	108/127	
1 1 0 1 1 0 1	109/127	
1 1 0 1 1 1 0	110/127	Palette 27 initial value[6:0]
1 1 0 1 1 1 1	111/127	
1 1 1 0 0 0 0	112/127	
1 1 1 0 0 0 1	113/127	
1 1 1 0 0 1 0	114/127	Palette 28 initial value[6:0]
1 1 1 0 0 1 1	115/127	
1 1 1 0 1 0 0	116/127	
1 1 1 0 1 0 1	117/127	
1 1 1 0 1 1 0	118/127	Palette 29 initial value[6:0]
1 1 1 0 1 1 1	119/127	
1 1 1 1 0 0 0	120/127	
1 1 1 1 0 0 1	121/127	
1 1 1 1 0 1 0	122/127	Palette 30 initial value[6:0]
1 1 1 1 0 1 1	123/127	
1 1 1 1 1 0 0	124/127	
1 1 1 1 1 0 1	125/127	
1 1 1 1 1 1 0	126/127	
1 1 1 1 1 1 1	127/127	Palette 31 initial value[6:0]

Remark 1) PBX[6:0] grayscale palette is enable under GS = '0'(defaults) setting.
Remark 2) Please refer to the description of setting range, effective bit and rule for each grayscale palettes

65k-color Mode(32 Grayscale from 64 Levels, PWM1=0, PWM0=0)

[Three groups of palettes Aj, Bj and Cj (j=0~31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks
0 0 0 0 0 0 X	0/63	Palette 0 initial value[6:1]
0 0 0 0 0 1 X	1/63	Palette X initial value[6:1]
0 0 0 0 1 0 X	2/63	
0 0 0 0 1 1 X	3/63	Palette 1 initial value[6:1]
0 0 0 1 0 0 X	4/63	
0 0 0 1 0 1 X	5/63	Palette 2 initial value[6:1]
0 0 0 1 1 0 X	6/63	
0 0 0 1 1 1 X	7/63	Palette 3 initial value[6:1]
0 0 1 0 0 0 X	8/63	
0 0 1 0 0 1 X	9/63	Palette 4 initial value[6:1]
0 0 1 0 1 0 X	10/63	
0 0 1 0 1 1 X	11/63	Palette 5 initial value[6:1]
0 0 1 1 0 0 X	12/63	
0 0 1 1 0 1 X	13/63	Palette 6 initial value[6:1]
0 0 1 1 1 0 X	14/63	
0 0 1 1 1 1 X	15/63	Palette 7 initial value[6:1]
0 1 0 0 0 0 X	16/63	
0 1 0 0 0 1 X	17/63	Palette 8 initial value[6:1]
0 1 0 0 1 0 X	18/63	
0 1 0 0 1 1 X	19/63	Palette 9 initial value[6:1]
0 1 0 1 0 0 X	20/63	
0 1 0 1 0 1 X	21/63	Palette 10 initial value[6:1]
0 1 0 1 1 0 X	22/63	
0 1 0 1 1 1 X	23/63	Palette 11 initial value[6:1]
0 1 1 0 0 0 X	24/63	
0 1 1 0 0 1 X	25/63	Palette 12 initial value[6:1]
0 1 1 0 1 0 X	26/63	
0 1 1 0 1 1 X	27/63	Palette 13 initial value[6:1]
0 1 1 1 0 0 X	28/63	
0 1 1 1 0 1 X	29/63	Palette 14 initial value[6:1]
0 1 1 1 1 0 X	30/63	
0 1 1 1 1 1 X	31/63	Palette 15 initial value[6:1]

Palette	Grayscale level	Remarks
1 0 0 0 0 0 X	32/63	
1 0 0 0 0 1 X	33/63	Palette 16 initial value[6:1]
1 0 0 0 1 0 X	34/63	
1 0 0 0 1 1 X	35/63	Palette 17 initial value[6:1]
1 0 0 1 0 0 X	36/63	
1 0 0 1 0 1 X	37/63	Palette 18 initial value[6:1]
1 0 0 1 1 0 X	38/63	
1 0 0 1 1 1 X	39/63	Palette 19 initial value[6:1]
1 0 1 0 0 0 X	40/63	
1 0 1 0 0 1 X	41/63	Palette 20 initial value[6:1]
1 0 1 0 1 0 X	42/63	
1 0 1 0 1 1 X	43/63	Palette 21 initial value[6:1]
1 0 1 1 0 0 X	44/63	
1 0 1 1 0 1 X	45/63	Palette 22 initial value[6:1]
1 0 1 1 1 0 X	46/63	
1 0 1 1 1 1 X	47/63	Palette 23 initial value[6:1]
1 1 0 0 0 0 X	48/63	
1 1 0 0 0 1 X	49/63	Palette 24 initial value[6:1]
1 1 0 0 1 0 X	50/63	
1 1 0 0 1 1 X	51/63	Palette 25 initial value[6:1]
1 1 0 1 0 0 X	52/63	
1 1 0 1 0 1 X	53/63	Palette 26 initial value[6:1]
1 1 0 1 1 0 X	54/63	
1 1 0 1 1 1 X	55/63	Palette 27 initial value[6:1]
1 1 1 0 0 0 X	56/63	
1 1 1 0 0 1 X	57/63	Palette 28 initial value][6:1]
1 1 1 0 1 0 X	58/63	
1 1 1 0 1 1 X	59/63	Palette 29 initial value[6:1]
1 1 1 1 0 0 X	60/63	
1 1 1 1 0 1 X	61/63	Palette 30 initial value[6:1]
1 1 1 1 1 0 X	62/63	
1 1 1 1 1 1 X	63/63	Palette 31 initial value[6:1]

65k-color Mode(32 Grayscale from 32 Levels, PWM1=0, PWM0=1)

[Three groups of palettes Aj, Bj and Cj (j=0~31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks
0 0 0 0 0 X X	0/31	Palette 0/X initial value[6:2]
0 0 0 0 1 X X	1/31	Palette 1 initial value[6:2]
0 0 0 1 0 X X	2/31	Palette 2 initial value[6:2]
0 0 0 1 1 X X	3/31	Palette 3 initial value[6:2]
0 0 1 0 0 X X	4/31	Palette 4 initial value[6:2]
0 0 1 0 1 X X	5/31	Palette 5 initial value[6:2]
0 0 1 1 0 X X	6/31	Palette 6 initial value[6:2]
0 0 1 1 1 X X	7/31	Palette 7 initial value[6:2]
0 1 0 0 0 X X	8/31	Palette 8 initial value[6:2]
0 1 0 0 1 X X	9/31	Palette 9 initial value[6:2]
0 1 0 1 0 X X	10/31	Palette 10 initial value[6:2]
0 1 0 1 1 X X	11/31	Palette 11 initial value[6:2]
0 1 1 0 0 X X	12/31	Palette 12 initial value[6:2]
0 1 1 0 1 X X	13/31	Palette 13 initial value[6:2]
0 1 1 1 0 X X	14/31	Palette 14 initial value[6:2]
0 1 1 1 1 X X	15/31	Palette 15 initial value[6:2]

Palette	Grayscale level	Remarks
1 0 0 0 0 X X	16/31	Palette 16 initial value[6:2]
1 0 0 0 1 X X	17/31	Palette 17 initial value[6:2]
1 0 0 1 0 X X	18/31	Palette 18 initial value[6:2]
1 0 0 1 1 X X	19/31	Palette 19 initial value[6:2]
1 0 1 0 0 X X	20/31	Palette 20 initial value[6:2]
1 0 1 0 1 X X	21/31	Palette 21 initial value[6:2]
1 0 1 1 0 X X	22/31	Palette 22 initial value[6:2]
1 0 1 1 1 X X	23/31	Palette 23 initial value[6:2]
1 1 0 0 0 X X	24/31	Palette 24 initial value[6:2]
1 1 0 0 1 X X	25/31	Palette 25 initial value[6:2]
1 1 0 1 0 X X	26/31	Palette 26 initial value[6:2]
1 1 0 1 1 X X	27/31	Palette 27 initial value[6:2]
1 1 1 0 0 X X	28/31	Palette 28 initial value][6:2]
1 1 1 0 1 X X	29/31	Palette 29 initial value[6:2]
1 1 1 1 0 X X	30/31	Palette 30 initial value[6:2]
1 1 1 1 1 X X	31/31	Palette 31 initial value[6:2]

4k-color Mode(16 Grayscale from 128 Levels, PWM1=1, PWM0=1)

Only odd number palettes (ex palette1 palette3 .. palette31)are effective under 4k color mode.

[Three groups of palettes Aj, Bj and Cj (j=1,3,5 …29, 31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks
0 0 0 0 0 0 0	0/127	
0 0 0 0 0 0 1	1/127	
0 0 0 0 0 1 0	2/127	
0 0 0 0 0 1 1	3/127	
0 0 0 0 1 0 0	4/127	
0 0 0 0 1 0 1	5/127	
0 0 0 0 1 1 0	6/127	Palette 1 initial value[6:0]
0 0 0 0 1 1 1	7/127	
0 0 0 1 0 0 0	8/127	
0 0 0 1 0 0 1	9/127	
0 0 0 1 0 1 0	10/127	
0 0 0 1 0 1 1	11/127	
0 0 0 1 1 0 0	12/127	
0 0 0 1 1 0 1	13/127	
0 0 0 1 1 1 0	14/127	Palette 3 initial value[6:0]
0 0 0 1 1 1 1	15/127	
0 0 1 0 0 0 0	16/127	
0 0 1 0 0 0 1	17/127	
0 0 1 0 0 1 0	18/127	
0 0 1 0 0 1 1	19/127	
0 0 1 0 1 0 0	20/127	
0 0 1 0 1 0 1	21/127	
0 0 1 0 1 1 0	22/127	Palette 5 initial value[6:0]
0 0 1 0 1 1 1	23/127	
0 0 1 1 0 0 0	24/127	
0 0 1 1 0 0 1	25/127	
0 0 1 1 0 1 0	26/127	
0 0 1 1 0 1 1	27/127	
0 0 1 1 1 0 0	28/127	
0 0 1 1 1 0 1	29/127	
0 0 1 1 1 1 0	30/127	Palette 7 initial value[6:0]
0 0 1 1 1 1 1	31/127	
0 1 0 0 0 0 0	32/127	
0 1 0 0 0 0 1	33/127	
0 1 0 0 0 1 0	34/127	
0 1 0 0 0 1 1	35/127	
0 1 0 0 1 0 0	36/127	
0 1 0 0 1 0 1	37/127	
0 1 0 0 1 1 0	38/127	Palette 9 initial value[6:0]
0 1 0 0 1 1 1	39/127	
0 1 0 1 0 0 0	40/127	
0 1 0 1 0 0 1	41/127	
0 1 0 1 0 1 0	42/127	
0 1 0 1 0 1 1	43/127	
0 1 0 1 1 0 0	44/127	
0 1 0 1 1 0 1	45/127	
0 1 0 1 1 1 0	46/127	Palette 11 initial value[6:0]
0 1 0 1 1 1 1	47/127	
0 1 1 0 0 0 0	48/127	
0 1 1 0 0 0 1	49/127	
0 1 1 0 0 1 0	50/127	
0 1 1 0 0 1 1	51/127	
0 1 1 0 1 0 0	52/127	
0 1 1 0 1 0 1	53/127	
0 1 1 0 1 1 0	54/127	Palette 13 initial value[6:0]
0 1 1 0 1 1 1	55/127	
0 1 1 1 0 0 0	56/127	
0 1 1 1 0 0 1	57/127	
0 1 1 1 0 1 0	58/127	
0 1 1 1 0 1 1	59/127	
0 1 1 1 1 0 0	60/127	
0 1 1 1 1 0 1	61/127	
0 1 1 1 1 1 0	62/127	Palette 15 initial value[6:0]
0 1 1 1 1 1 1	63/127	

Palette	Grayscale level	Remarks
1 0 0 0 0 0 0	64/127	
1 0 0 0 0 0 1	65/127	
1 0 0 0 0 1 0	66/127	
1 0 0 0 0 1 1	67/127	
1 0 0 0 1 0 0	68/127	
1 0 0 0 1 0 1	69/127	
1 0 0 0 1 1 0	70/127	Palette 17 initial value[6:0]
1 0 0 0 1 1 1	71/127	
1 0 0 1 0 0 0	72/127	
1 0 0 1 0 0 1	73/127	
1 0 0 1 0 1 0	74/127	
1 0 0 1 0 1 1	75/127	
1 0 0 1 1 0 0	76/127	
1 0 0 1 1 0 1	77/127	
1 0 0 1 1 1 0	78/127	Palette 19 initial value[6:0]
1 0 0 1 1 1 1	79/127	
1 0 1 0 0 0 0	80/127	
1 0 1 0 0 0 1	81/127	
1 0 1 0 0 1 0	82/127	
1 0 1 0 0 1 1	83/127	
1 0 1 0 1 0 0	84/127	
1 0 1 0 1 0 1	85/127	
1 0 1 0 1 1 0	86/127	Palette 21 initial value[6:0]
1 0 1 0 1 1 1	87/127	
1 0 1 1 0 0 0	88/127	
1 0 1 1 0 0 1	89/127	
1 0 1 1 0 1 0	90/127	
1 0 1 1 0 1 1	91/127	
1 0 1 1 1 0 0	92/127	
1 0 1 1 1 0 1	93/127	
1 0 1 1 1 1 0	94/127	Palette 23 initial value[6:0]
1 0 1 1 1 1 1	95/127	
1 1 0 0 0 0 0	96/127	
1 1 0 0 0 0 1	97/127	
1 1 0 0 0 1 0	98/127	
1 1 0 0 0 1 1	99/127	
1 1 0 0 1 0 0	100/127	
1 1 0 0 1 0 1	101/127	
1 1 0 0 1 1 0	102/127	Palette 25 initial value[6:0]
1 1 0 0 1 1 1	103/127	
1 1 0 1 0 0 0	104/127	
1 1 0 1 0 0 1	105/127	
1 1 0 1 0 1 0	106/127	
1 1 0 1 0 1 1	107/127	
1 1 0 1 1 0 0	108/127	
1 1 0 1 1 0 1	109/127	
1 1 0 1 1 1 0	110/127	Palette 27 initial value[6:0]
1 1 0 1 1 1 1	111/127	
1 1 1 0 0 0 0	112/127	
1 1 1 0 0 0 1	113/127	
1 1 1 0 0 1 0	114/127	
1 1 1 0 0 1 1	115/127	
1 1 1 0 1 0 0	116/127	
1 1 1 0 1 0 1	117/127	
1 1 1 0 1 1 0	118/127	Palette 29 initial value[6:0]
1 1 1 0 1 1 1	119/127	
1 1 1 1 0 0 0	120/127	
1 1 1 1 0 0 1	121/127	
1 1 1 1 0 1 0	122/127	
1 1 1 1 0 1 1	123/127	
1 1 1 1 1 0 0	124/127	
1 1 1 1 1 0 1	125/127	
1 1 1 1 1 1 0	126/127	
1 1 1 1 1 1 1	127/127	Palette 31 initial value[6:0]

4k-color Mode(16 Grayscale from 64 Levels, PWM1=0, PWM0=0)

[Three groups of palettes Aj, Bj and Cj (j=1,3,5 …29, 31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks
0 0 0 0 0 0 X	0/63	
0 0 0 0 0 1 X	1/63	
0 0 0 0 1 0 X	2/63	
0 0 0 0 1 1 X	3/63	Palette 1 initial value[6:1]
0 0 0 1 0 0 X	4/63	
0 0 0 1 0 1 X	5/63	
0 0 0 1 1 0 X	6/63	
0 0 0 1 1 1 X	7/63	Palette 3 initial value[6:1]
0 0 1 0 0 0 X	8/63	
0 0 1 0 0 1 X	9/63	
0 0 1 0 1 0 X	10/63	
0 0 1 0 1 1 X	11/63	Palette 5 initial value[6:1]
0 0 1 1 0 0 X	12/63	
0 0 1 1 0 1 X	13/63	
0 0 1 1 1 0 X	14/63	
0 0 1 1 1 1 X	15/63	Palette 7 initial value[6:1]
0 1 0 0 0 0 X	16/63	
0 1 0 0 0 1 X	17/63	
0 1 0 0 1 0 X	18/63	
0 1 0 0 1 1 X	19/63	Palette 9 initial value[6:1]
0 1 0 1 0 0 X	20/63	
0 1 0 1 0 1 X	21/63	
0 1 0 1 1 0 X	22/63	
0 1 0 1 1 1 X	23/63	Palette 11 initial value[6:1]
0 1 1 0 0 0 X	24/63	
0 1 1 0 0 1 X	25/63	
0 1 1 0 1 0 X	26/63	
0 1 1 0 1 1 X	27/63	Palette 13 initial value[6:1]
0 1 1 1 0 0 X	28/63	
0 1 1 1 0 1 X	29/63	
0 1 1 1 1 0 X	30/63	
0 1 1 1 1 1 X	31/63	Palette 15 initial value[6:1]

Palette	Grayscale level	Remarks
1 0 0 0 0 0 X	32/63	
1 0 0 0 0 1 X	33/63	
1 0 0 0 1 0 X	34/63	
1 0 0 0 1 1 X	35/63	Palette 17 initial value[6:1]
1 0 0 1 0 0 X	36/63	
1 0 0 1 0 1 X	37/63	
1 0 0 1 1 0 X	38/63	
1 0 0 1 1 1 X	39/63	Palette 19 initial value[6:1]
1 0 1 0 0 0 X	40/63	
1 0 1 0 0 1 X	41/63	
1 0 1 0 1 0 X	42/63	
1 0 1 0 1 1 X	43/63	Palette 21 initial value[6:1]
1 0 1 1 0 0 X	44/63	
1 0 1 1 0 1 X	45/63	
1 0 1 1 1 0 X	46/63	
1 0 1 1 1 1 X	47/63	Palette 23 initial value[6:1]
1 1 0 0 0 0 X	48/63	
1 1 0 0 0 1 X	49/63	
1 1 0 0 1 0 X	50/63	
1 1 0 0 1 1 X	51/63	Palette 25 initial value[6:1]
1 1 0 1 0 0 X	52/63	
1 1 0 1 0 1 X	53/63	
1 1 0 1 1 0 X	54/63	
1 1 0 1 1 1 X	55/63	Palette 27 initial value[6:1]
1 1 1 0 0 0 X	56/63	
1 1 1 0 0 1 X	57/63	
1 1 1 0 1 0 X	58/63	
1 1 1 0 1 1 X	59/63	Palette 29 initial value[6:1]
1 1 1 1 0 0 X	60/63	
1 1 1 1 0 1 X	61/63	
1 1 1 1 1 0 X	62/63	
1 1 1 1 1 1 X	63/63	Palette 31 initial value[6:1]

4k-color Mode(16 Grayscale from 32 Levels, PWM1=0, PWM0=1)

[Three groups of palettes Aj, Bj and Cj (j=1,3,5 …29, 31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks
0 0 0 0 0 X X	0/31	
0 0 0 0 1 X X	1/31	Palette 1 initial value[6:2]
0 0 0 1 0 X X	2/31	
0 0 0 1 1 X X	3/31	Palette 3 initial value[6:2]
0 0 1 0 0 X X	4/31	
0 0 1 0 1 X X	5/31	Palette 5 initial value[6:2]
0 0 1 1 0 X X	6/31	
0 0 1 1 1 X X	7/31	Palette 7 initial value[6:2]
0 1 0 0 0 X X	8/31	
0 1 0 0 1 X X	9/31	Palette 9 initial value[6:2]
0 1 0 1 0 X X	10/31	
0 1 0 1 1 X X	11/31	Palette 11 initial value[6:2]
0 1 1 0 0 X X	12/31	
0 1 1 0 1 X X	13/31	Palette 13 initial value[6:2]
0 1 1 1 0 X X	14/31	
0 1 1 1 1 X X	15/31	Palette 15 initial value[6:2]

Palette	Grayscale level	Remarks
1 0 0 0 0 X X	16/31	
1 0 0 0 1 X X	17/31	Palette 17 initial value[6:2]
1 0 0 1 0 X X	18/31	
1 0 0 1 1 X X	19/31	Palette 19 initial value[6:2]
1 0 1 0 0 X X	20/31	
1 0 1 0 1 X X	21/31	Palette 21 initial value[6:2]
1 0 1 1 0 X X	22/31	
1 0 1 1 1 X X	23/31	Palette 23 initial value[6:2]
1 1 0 0 0 X X	24/31	
1 1 0 0 1 X X	25/31	Palette 25 initial value[6:2]
1 1 0 1 0 X X	26/31	
1 1 0 1 1 X X	27/31	Palette 27 initial value[6:2]
1 1 1 0 0 X X	28/31	
1 1 1 0 1 X X	29/31	Palette 29 initial value[6:2]
1 1 1 1 0 X X	30/31	
1 1 1 1 1 X X	31/31	Palette 31 initial value[6:2]

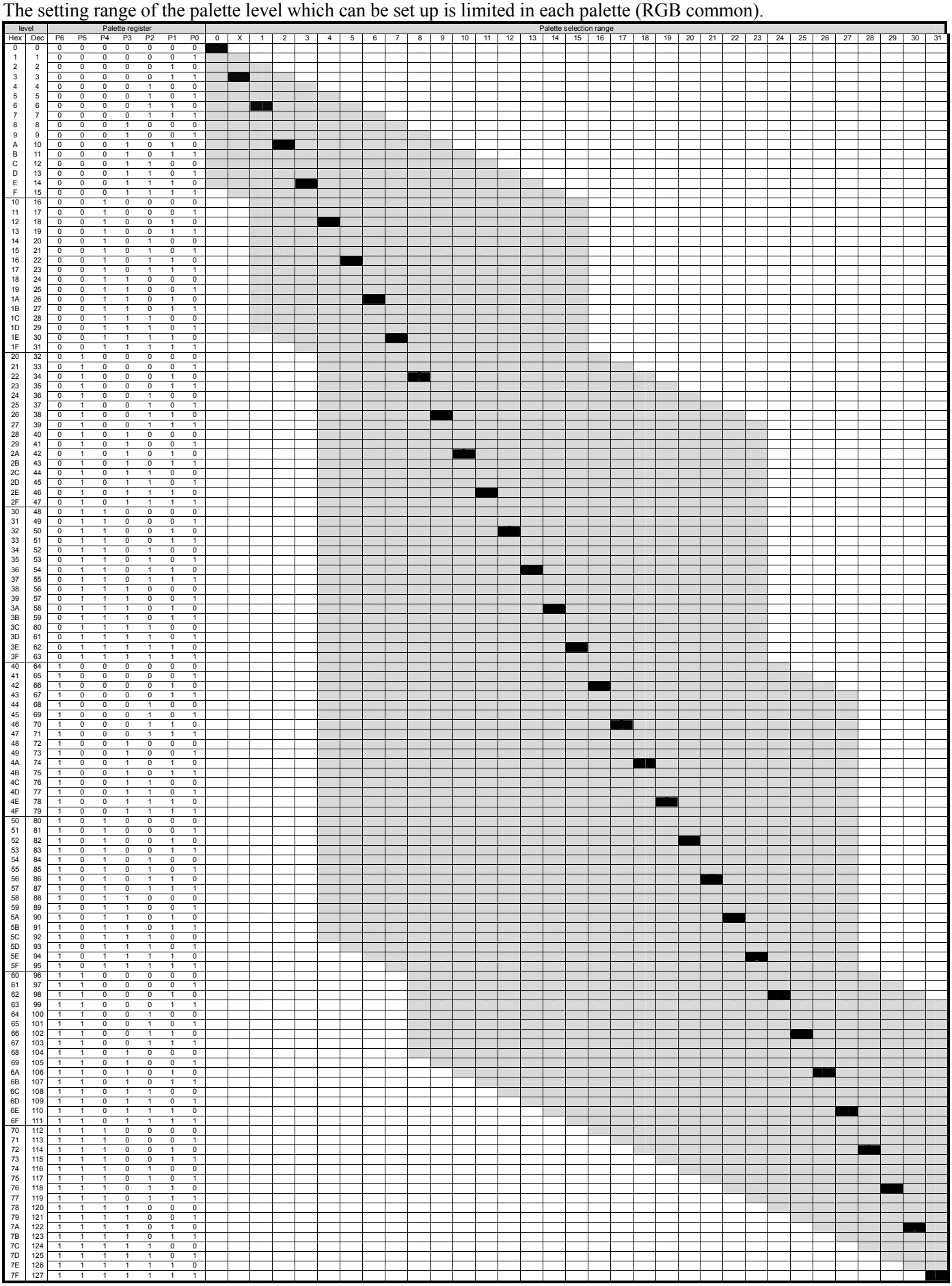
4k-color Mode(16 Grayscale from 16 Levels, PWM1=1, PWM0=0)

[Three groups of palettes Aj, Bj and Cj (j=1,3,5 …29, 31) are available] (marking points are default positions)

Palette	Grayscale level	Remarks
0 0 0 0 X X X	0/15	Palette 1 initial value[6:3]
0 0 0 1 X X X	1/15	Palette 3 initial value[6:3]
0 0 1 0 X X X	2/15	Palette 5 initial value[6:3]
0 0 1 1 X X X	3/15	Palette 7 initial value[6:3]
0 1 0 0 X X X	4/15	Palette 9 initial value[6:3]
0 1 0 1 X X X	5/15	Palette 11 initial value[6:3]
0 1 1 0 X X X	6/15	Palette 13 initial value[6:3]
0 1 1 1 X X X	7/15	Palette 15 initial value[6:3]

Palette	Grayscale level	Remarks
1 0 0 0 X X X	8/15	Palette 17 initial value[6:3]
1 0 0 1 X X X	9/15	Palette 19 initial value[6:3]
1 0 1 0 X X X	10/15	Palette 21 initial value[6:3]
1 0 1 1 X X X	11/15	Palette 23 initial value[6:3]
1 1 0 0 X X X	12/15	Palette 25 initial value[6:3]
1 1 0 1 X X X	13/15	Palette 27 initial value[6:3]
1 1 1 0 X X X	14/15	Palette 29 initial value[6:3]
1 1 1 1 X X X	15/15	Palette 31 initial value[6:3]

The setting range of the palette level which can be set up is limited in each palette (RGB common).



Caution: Do not set same level for each grayscale palette ($palette_m = palette_n$, m = 0~31, n = 0~31) Forbidden random level palette ($palette_n > palette_{n+1}$)

The setting range of the palette level can be expressed as the following table.

Palette No.	Palette register						
	MSB						LSB
	6	5	4	3	2	1	0
0	0			Anything			
X	0			Anything			
1	0		Anything				
2	0		Anything				
3	0		Anything				
4	Except(1,1)		Anything				
5	Except(1,1)		Anything				
6	Except(1,1)		Anything				
7	Except(1,1)		Anything				
8	Anything						
9	Anything						
10	Anything						
11	Anything						
12	Anything						
13	Anything						
14	Anything						
15	Anything						
16	Except(0,0)		Anything				
17	Except(0,0)		Anything				
18	Except(0,0)		Anything				
19	Except(0,0)		Anything				
20	Except(0,0)		Anything				
21	Except(0,0)		Anything				
22	Except(0,0)		Anything				
23	Except(0,0)		Anything				
24	1	Anything					
25	1	Anything					
26	1	Anything					
27	1	Anything					
28	1		Anything				
29	1		Anything				
30	1		Anything				
31	1		Anything				

Caution:
(1) Do not set the same grayscale level in each grayscale palette(forbidden case: $palette_m = palette_{m+n}$, m=0~31 n=0~31)
(2) Do not set the zigzag typed grayscale palette. (forbidden case: $palette_n > palette_{n+1}$, n=0~31)

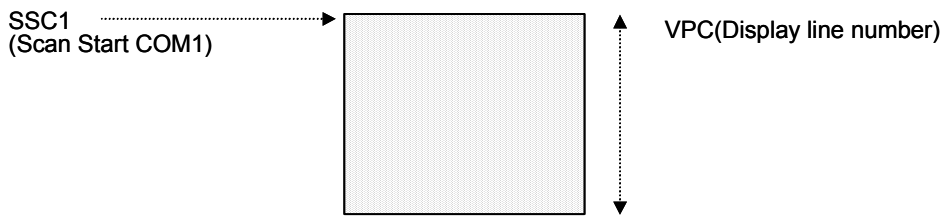
(13) PARTIAL DISPLAY FUNCTION

Partial display function is used to save power. In the partial display mode, only specified common drivers output scanning signals, therefore part of the panel area is selected for display. Because the duty ratio and LCD driving voltage are lowed in partial display mode. Current consumption can be minimized.

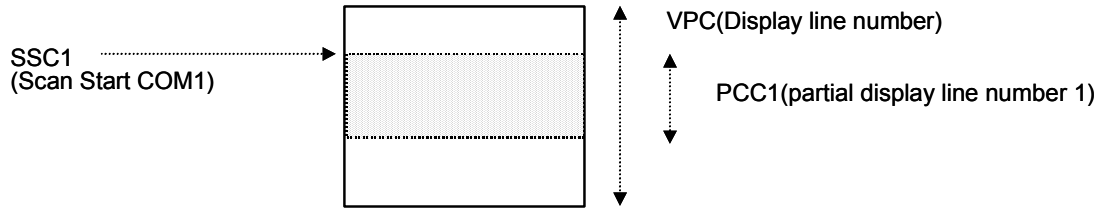
NJU6854 can realize 3 partial display areas on the screen once. The setting of Partial display function is conducted through Scan Start COM 1~3(SSC1~3) registers, Partial Display Line Number 1~3(PCC1~3) registers, Power Control 1~2 (TCBI,POW2) registers, Amplifier Gain/Booster Level(GVU) register, and 3 Partial Display/LED Control/Rev (ECONT) register. Refer to (15)TYPICAL INSTRUCTION SEQUENCES for the functions setting

The image of partial display.

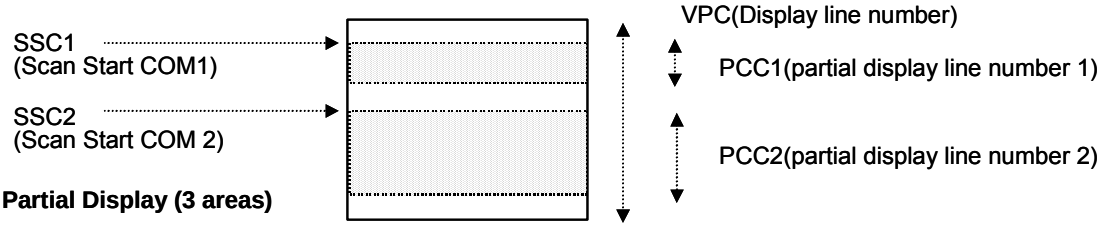
(i) Full Screen Display



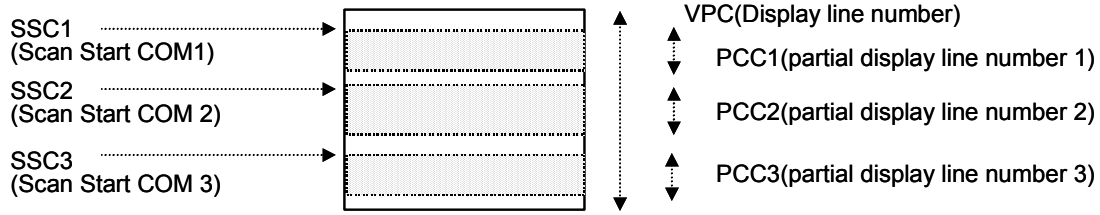
(ii) Partial Display (1 area)



(iii) Partial Display (2 areas)



(iv) Partial Display (3 areas)



Note) For the full screen display, set the Scan Start COM 1(SCC1) and the Display Line Number(VPC).
For the partial display, set the Scan Start COM 1~3(SCC1~3) and the Partial Display Line Number 1~3(PCC1~3). In this case, the Partial Display Line Number 1~3(PCC1~3) have priority over the Display Line Number(VPC), and thus the display duty is: Duty=PCC1+PCC2+PCC.

(14) RELATIONSHIP BETWEEN LOGICAL COM NUMBER AND PHYSICAL COMMON DRIVER

(EN3PTL='0')

VPC (Display line number)	106							
HCT (Header COM)	13							
SHIFT[1] (COM shift A/B set)	'0' (A start-> A end -> B start -> B end)							
SHIFT[0] (COM shift direction)	'0'				'1'			
SSC1 (Scan Start COM 1)	logical	0	10	36	logical	0	96	11
SSC2 (Scan Start COM 2)	COM	0	0	80	COM	0	0	50
PCC1 (Line No. of partial display 1)	number	0	0	20	number	0	0	15
PCC2 (Line No. of partial display 2)		0	0	15		0	0	20
SSC3 (Scan Start COM 3)		*	*	*		*	*	*
PCC3 (Line No. of partial display 3)		*	*	*		*	*	*

Physical COM name	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
	COMA0	COMB0	-	-							-	-						
	COMA1	COMB1	-	-							-	-						
	COMA2	COMB2	-	-							-	-						
	COMA3	COMB3	-	-							-	-						
	COMA4	COMB4	-	-							-	-						
	COMA5	COMB5	-	-							-	-						
	COMA6	COMB6	-	-							-	-						
	COMA7	COMB7	-	-							-	-						
	COMA8	COMB8	-	-							-	-						
	COMA9	COMB9	-	-							-	-						
	COMA10	COMB10	-	-							-	-						
	COMA11	COMB11	-	-							-	-						
	COMA12	COMB12	-	-							-	-						
	COMA13	COMB13	0	53	0	53	96	43		17	105	52	105	52	9	62		17
	COMA14	COMB14	1	54	1	54	97	44		18	104	51	104	51	8	61		16
	COMA15	COMB15	2	55	2	55	98	45		19	103	50	103	50	7	60		15
	COMA16	COMB16	3	56	3	56	99	46			102	49	102	49	6	59		
	COMA17	COMB17	4	57	4	57	100	47			101	48	101	48	5	58		
	COMA18	COMB18	5	58	5	58	101	48			100	47	100	47	4	57		
	COMA19	COMB19	6	59	6	59	102	49			99	46	99	46	3	56		
	COMA20	COMB20	7	60	7	60	103	50			98	45	98	45	2	55		
	COMA21	COMB21	8	61	8	61	104	51			97	44	97	44	1	54		
	COMA22	COMB22	9	62	9	62	105	52			96	43	96	43	0	53		
	COMA23	COMB23	10	63	10	63	0	53			95	42	95	42	105	52		
	COMA24	COMB24	11	64	11	64	1	54			94	41	94	41	104	51		
	COMA25	COMB25	12	65	12	65	2	55			93	40	93	40	103	50		
	COMA26	COMB26	13	66	13	66	3	56			92	39	92	39	102	49		
	COMA27	COMB27	14	67	14	67	4	57			91	38	91	38	101	48		
	COMA28	COMB28	15	68	15	68	5	58			90	37	90	37	100	47		
	COMA29	COMB29	16	69	16	69	6	59			89	36	89	36	99	46		
	COMA30	COMB30	17	70	17	70	7	60			88	35	88	35	98	45		
	COMA31	COMB31	18	71	18	71	8	61			87	34	87	34	97	44		
	COMA32	COMB32	19	72	19	72	9	62			86	33	86	33	96	43		
	COMA33	COMB33	20	73	20	73	10	63			85	32	85	32	95	42		
	COMA34	COMB34	21	74	21	74	11	64			84	31	84	31	94	41		
	COMA35	COMB35	22	75	22	75	12	65			83	30	83	30	93	40		
	COMA36	COMB36	23	76	23	76	13	66			82	29	82	29	92	39		
	COMA37	COMB37	24	77	24	77	14	67			81	28	81	28	91	38		
	COMA38	COMB38	25	78	25	78	15	68			80	27	80	27	90	37		
	COMA39	COMB39	26	79	26	79	16	69			79	26	79	26	89	36		
	COMA40	COMB40	27	80	27	80	17	70		20	78	25	78	25	88	35		14
	COMA41	COMB41	28	81	28	81	18	71		21	77	24	77	24	87	34		13
	COMA42	COMB42	29	82	29	82	19	72		22	76	23	76	23	86	33		12
	COMA43	COMB43	30	83	30	83	20	73		23	75	22	75	22	85	32		11
	COMA44	COMB44	31	84	31	84	21	74		24	74	21	74	21	84	31		10
	COMA45	COMB45	32	85	32	85	22	75		25	73	20	73	20	83	30		9
	COMA46	COMB46	33	86	33	86	23	76		26	72	19	72	19	82	29		8
	COMA47	COMB47	34	87	34	87	24	77		27	71	18	71	18	81	28		7
	COMA48	COMB48	35	88	35	88	25	78		28	70	17	70	17	80	27		6
	COMA49	COMB49	36	89	36	89	26	79	0	29	69	16	69	16	79	26	34	5
	COMA50	COMB50	37	90	37	90	27	80	1	30	68	15	68	15	78	25	33	4
	COMA51	COMB51	38	91	38	91	28	81	2	31	67	14	67	14	77	24	32	3
	COMA52	COMB52	39	92	39	92	29	82	3	32	66	13	66	13	76	23	31	2
	COMA53	COMB53	40	93	40	93	30	83	4	33	65	12	65	12	75	22	30	1
	COMA54	COMB54	41	94	41	94	31	84	5	34	64	11	64	11	74	21	29	0
	COMA55	COMB55	42	95	42	95	32	85	6		63	10	63	10	73	20	28	
	COMA56	COMB56	43	96	43	96	33	86	7		62	9	62	9	72	19	27	
	COMA57	COMB57	44	97	44	97	34	87	8		61	8	61	8	71	18	26	
	COMA58	COMB58	45	98	45	98	35	88	9		60	7	60	7	70	17	25	
	COMA59	COMB59	46	99	46	99	36	89	10		59	6	59	6	69	16	24	
	COMA60	COMB60	47	100	47	100	37	90	11		58	5	58	5	68	15	23	
	COMA61	COMB61	48	101	48	101	38	91	12		57	4	57	4	67	14	22	
	COMA62	COMB62	49	102	49	102	39	92	13		56	3	56	3	66	13	21	
	COMA63	COMB63	50	103	50	103	40	93	14		55	2	55	2	65	12	20	
	COMA64	COMB64	51	104	51	104	41	94	15		54	1	54	1	64	11	19	
	COMA65	COMB65	52	105	52	105	42	95	16		53	0	53	0	63	10	18	

REMARK	(A -> B)	one area	one area	two area	(A <- B)	one area	one area	two area
		Normal				Reversed		

(EN3PTL= '1')

VPC (Display line number)	106							
HCT (Header COM)	13							
SHIFT[1] (COM shift A/B set)	'1' (B start-> B end -> A start -> A end)							
SHIFT[0] (COM shift direction)	'0'				'1'			
SSC1 (Scan Start COM 1)	logical	0	10	36	logical	0	96	11
SSC2 (Scan Start COM 2)	COM	0	0	80	COM	0	0	50
PCC1 (Line No. of partial display 1)	number	0	0	20	number	0	0	15
PCC2 (Line No. of partial display 2)		0	0	15		0	0	20
SSC3 (Scan Start COM 3)		*	*	*		*	*	*
PCC3 (Line No. of partial display 3)		*	*	*		*	*	*

	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
Physical COM name	COMA0	COMB0	-	-							-	-						
	COMA1	COMB1	-	-							-	-						
	COMA2	COMB2	-	-							-	-						
	COMA3	COMB3	-	-							-	-						
	COMA4	COMB4	-	-							-	-						
	COMA5	COMB5	-	-							-	-						
	COMA6	COMB6	-	-							-	-						
	COMA7	COMB7	-	-							-	-						
	COMA8	COMB8	-	-							-	-						
	COMA9	COMB9	-	-							-	-						
	COMA10	COMB10	-	-							-	-						
	COMA11	COMB11	-	-							-	-						
	COMA12	COMB12	-	-							-	-						
	COMA13	COMB13	53	0	53	0	43	96	17		52	105	52	105	62	9	17	
	COMA14	COMB14	54	1	54	1	44	97	18		51	104	51	104	61	8	16	
	COMA15	COMB15	55	2	55	2	45	98	19		50	103	50	103	60	7	15	
	COMA16	COMB16	56	3	56	3	46	99			49	102	49	102	59	6		
	COMA17	COMB17	57	4	57	4	47	100			48	101	48	101	58	5		
	COMA18	COMB18	58	5	58	5	48	101			47	100	47	100	57	4		
	COMA19	COMB19	59	6	59	6	49	102			46	99	46	99	56	3		
	COMA20	COMB20	60	7	60	7	50	103			45	98	45	98	55	2		
	COMA21	COMB21	61	8	61	8	51	104			44	97	44	97	54	1		
	COMA22	COMB22	62	9	62	9	52	105			43	96	43	96	53	0		
	COMA23	COMB23	63	10	63	10	53	0			42	95	42	95	52	105		
	COMA24	COMB24	64	11	64	11	54	1			41	94	41	94	51	104		
	COMA25	COMB25	65	12	65	12	55	2			40	93	40	93	50	103		
	COMA26	COMB26	66	13	66	13	56	3			39	92	39	92	49	102		
	COMA27	COMB27	67	14	67	14	57	4			38	91	38	91	48	101		
	COMA28	COMB28	68	15	68	15	58	5			37	90	37	90	47	100		
	COMA29	COMB29	69	16	69	16	59	6			36	89	36	89	46	99		
	COMA30	COMB30	70	17	70	17	60	7			35	88	35	88	45	98		
	COMA31	COMB31	71	18	71	18	61	8			34	87	34	87	44	97		
	COMA32	COMB32	72	19	72	19	62	9			33	86	33	86	43	96		
	COMA33	COMB33	73	20	73	20	63	10			32	85	32	85	42	95		
	COMA34	COMB34	74	21	74	21	64	11			31	84	31	84	41	94		
	COMA35	COMB35	75	22	75	22	65	12			30	83	30	83	40	93		
	COMA36	COMB36	76	23	76	23	66	13			29	82	29	82	39	92		
	COMA37	COMB37	77	24	77	24	67	14			28	81	28	81	38	91		
	COMA38	COMB38	78	25	78	25	68	15			27	80	27	80	37	90		
	COMA39	COMB39	79	26	79	26	69	16			26	79	26	79	36	89		
	COMA40	COMB40	80	27	80	27	70	17	20		25	78	25	78	35	88	14	
	COMA41	COMB41	81	28	81	28	71	18	21		24	77	24	77	34	87	13	
	COMA42	COMB42	82	29	82	29	72	19	22		23	76	23	76	33	86	12	
	COMA43	COMB43	83	30	83	30	73	20	23		22	75	22	75	32	85	11	
	COMA44	COMB44	84	31	84	31	74	21	24		21	74	21	74	31	84	10	
	COMA45	COMB45	85	32	85	32	75	22	25		20	73	20	73	30	83	9	
	COMA46	COMB46	86	33	86	33	76	23	26		19	72	19	72	29	82	8	
	COMA47	COMB47	87	34	87	34	77	24	27		18	71	18	71	28	81	7	
	COMA48	COMB48	88	35	88	35	78	25	28		17	70	17	70	27	80	6	
	COMA49	COMB49	89	36	89	36	79	26	29	0	16	69	16	69	26	79	5	34
	COMA50	COMB50	90	37	90	37	80	27	30	1	15	68	15	68	25	78	4	33
	COMA51	COMB51	91	38	91	38	81	28	31	2	14	67	14	67	24	77	3	32
	COMA52	COMB52	92	39	92	39	82	29	32	3	13	66	13	66	23	76	2	31
	COMA53	COMB53	93	40	93	40	83	30	33	4	12	65	12	65	22	75	1	30
	COMA54	COMB54	94	41	94	41	84	31	34	5	11	64	11	64	21	74	0	29
	COMA55	COMB55	95	42	95	42	85	32		6	10	63	10	63	20	73		28
	COMA56	COMB56	96	43	96	43	86	33		7	9	62	9	62	19	72		27
	COMA57	COMB57	97	44	97	44	87	34		8	8	61	8	61	18	71		26
	COMA58	COMB58	98	45	98	45	88	35		9	7	60	7	60	17	70		25
	COMA59	COMB59	99	46	99	46	89	36		10	6	59	6	59	16	69		24
	COMA60	COMB60	100	47	100	47	90	37		11	5	58	5	58	15	68		23
	COMA61	COMB61	101	48	101	48	91	38		12	4	57	4	57	14	67		22
	COMA62	COMB62	102	49	102	49	92	39		13	3	56	3	56	13	66		21
	COMA63	COMB63	103	50	103	50	93	40		14	2	55	2	55	12	65		20
	COMA64	COMB64	104	51	104	51	94	41		15	1	54	1	54	11	64		19
	COMA65	COMB65	105	52	105	52	95	42		16	0	53	0	53	10	63		18

REMARK	(B -> A)	one area	one area	two area	(B <- A)	one area	one area	two area
		Normal				Reversed		

(EN3PTL= '1')

VPC (Display line number)	106							
HCT (Header COM)	13							
SHIFT[1] (COM shift A/B set)	'0' (A start-> A end -> B start -> B end)							
SHIFT[0] (COM shift direction)	'0'				'1'			
SSC1 (Scan Start COM 1)	logical	0	10	36	logical	0	96	0
SSC2 (Scan Start COM 2)	COM	0	0	80	COM	0	0	11
PCC1 (Line No. of partial display 1)	number	0	0	20	number	0	0	5
PCC2 (Line No. of partial display 2)		0	0	15		0	0	15
SSC3 (Scan Start COM 3)		0	0	101		0	0	50
PCC3 (Line No. of partial display 3)		0	0	5		0	0	20

Physical COM name																		
A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
COMA0	COMB0	-	-							-	-						
COMA1	COMB1	-	-							-	-						
COMA2	COMB2	-	-							-	-						
COMA3	COMB3	-	-							-	-						
COMA4	COMB4	-	-							-	-						
COMA5	COMB5	-	-							-	-						
COMA6	COMB6	-	-							-	-						
COMA7	COMB7	-	-							-	-						
COMA8	COMB8	-	-							-	-						
COMA9	COMB9	-	-							-	-						
COMA10	COMB10	-	-							-	-						
COMA11	COMB11	-	-							-	-						
COMA12	COMB12	-	-							-	-						
COMA13	COMB13	0	53	0	53	96	43		17	105	52	105	52	9	62		22
COMA14	COMB14	1	54	1	54	97	44		18	104	51	104	51	8	61		21
COMA15	COMB15	2	55	2	55	98	45		19	103	50	103	50	7	60		20
COMA16	COMB16	3	56	3	56	99	46			102	49	102	49	6	59		
COMA17	COMB17	4	57	4	57	100	47			101	48	101	48	5	58		
COMA18	COMB18	5	58	5	58	101	48			100	47	100	47	4	57		
COMA19	COMB19	6	59	6	59	102	49			99	46	99	46	3	56		
COMA20	COMB20	7	60	7	60	103	50			98	45	98	45	2	55		
COMA21	COMB21	8	61	8	61	104	51			97	44	97	44	1	54		
COMA22	COMB22	9	62	9	62	105	52			96	43	96	43	0	53		
COMA23	COMB23	10	63	10	63	0	53			95	42	95	42	105	52		
COMA24	COMB24	11	64	11	64	1	54			94	41	94	41	104	51		
COMA25	COMB25	12	65	12	65	2	55			93	40	93	40	103	50		
COMA26	COMB26	13	66	13	66	3	56			92	39	92	39	102	49		
COMA27	COMB27	14	67	14	67	4	57			91	38	91	38	101	48		
COMA28	COMB28	15	68	15	68	5	58			90	37	90	37	100	47		
COMA29	COMB29	16	69	16	69	6	59			89	36	89	36	99	46		
COMA30	COMB30	17	70	17	70	7	60			88	35	88	35	98	45		
COMA31	COMB31	18	71	18	71	8	61			87	34	87	34	97	44		
COMA32	COMB32	19	72	19	72	9	62			86	33	86	33	96	43		
COMA33	COMB33	20	73	20	73	10	63			85	32	85	32	95	42		
COMA34	COMB34	21	74	21	74	11	64			84	31	84	31	94	41		
COMA35	COMB35	22	75	22	75	12	65			83	30	83	30	93	40		
COMA36	COMB36	23	76	23	76	13	66			82	29	82	29	92	39		
COMA37	COMB37	24	77	24	77	14	67			81	28	81	28	91	38		
COMA38	COMB38	25	78	25	78	15	68			80	27	80	27	90	37		
COMA39	COMB39	26	79	26	79	16	69			79	26	79	26	89	36		
COMA40	COMB40	27	80	27	80	17	70		20	78	25	78	25	88	35		19
COMA41	COMB41	28	81	28	81	18	71		21	77	24	77	24	87	34		18
COMA42	COMB42	29	82	29	82	19	72		22	76	23	76	23	86	33		17
COMA43	COMB43	30	83	30	83	20	73		23	75	22	75	22	85	32		16
COMA44	COMB44	31	84	31	84	21	74		24	74	21	74	21	84	31		15
COMA45	COMB45	32	85	32	85	22	75		25	73	20	73	20	83	30		14
COMA46	COMB46	33	86	33	86	23	76		26	72	19	72	19	82	29		13
COMA47	COMB47	34	87	34	87	24	77		27	71	18	71	18	81	28		12
COMA48	COMB48	35	88	35	88	25	78		28	70	17	70	17	80	27		11
COMA49	COMB49	36	89	36	89	26	79	0	29	69	16	69	16	79	26	39	10
COMA50	COMB50	37	90	37	90	27	80	1	30	68	15	68	15	78	25	38	9
COMA51	COMB51	38	91	38	91	28	81	2	31	67	14	67	14	77	24	37	8
COMA52	COMB52	39	92	39	92	29	82	3	32	66	13	66	13	76	23	36	7
COMA53	COMB53	40	93	40	93	30	83	4	33	65	12	65	12	75	22	35	6
COMA54	COMB54	41	94	41	94	31	84	5	34	64	11	64	11	74	21	34	5
COMA55	COMB55	42	95	42	95	32	85	6		63	10	63	10	73	20	33	
COMA56	COMB56	43	96	43	96	33	86	7		62	9	62	9	72	19	32	
COMA57	COMB57	44	97	44	97	34	87	8		61	8	61	8	71	18	31	
COMA58	COMB58	45	98	45	98	35	88	9		60	7	60	7	70	17	30	
COMA59	COMB59	46	99	46	99	36	89	10		59	6	59	6	69	16	29	
COMA60	COMB60	47	100	47	100	37	90	11		58	5	58	5	68	15	28	
COMA61	COMB61	48	101	48	101	38	91	12	35	57	4	57	4	67	14	27	4
COMA62	COMB62	49	102	49	102	39	92	13	36	56	3	56	3	66	13	26	3
COMA63	COMB63	50	103	50	103	40	93	14	37	55	2	55	2	65	12	25	2
COMA64	COMB64	51	104	51	104	41	94	15	38	54	1	54	1	64	11	24	1
COMA65	COMB65	52	105	52	105	42	95	16	39	53	0	53	0	63	10	23	0

REMARK	(A -> B)	one area	one area	two area	(A <- B)	one area	one area	two area
		Normal				Reversed		

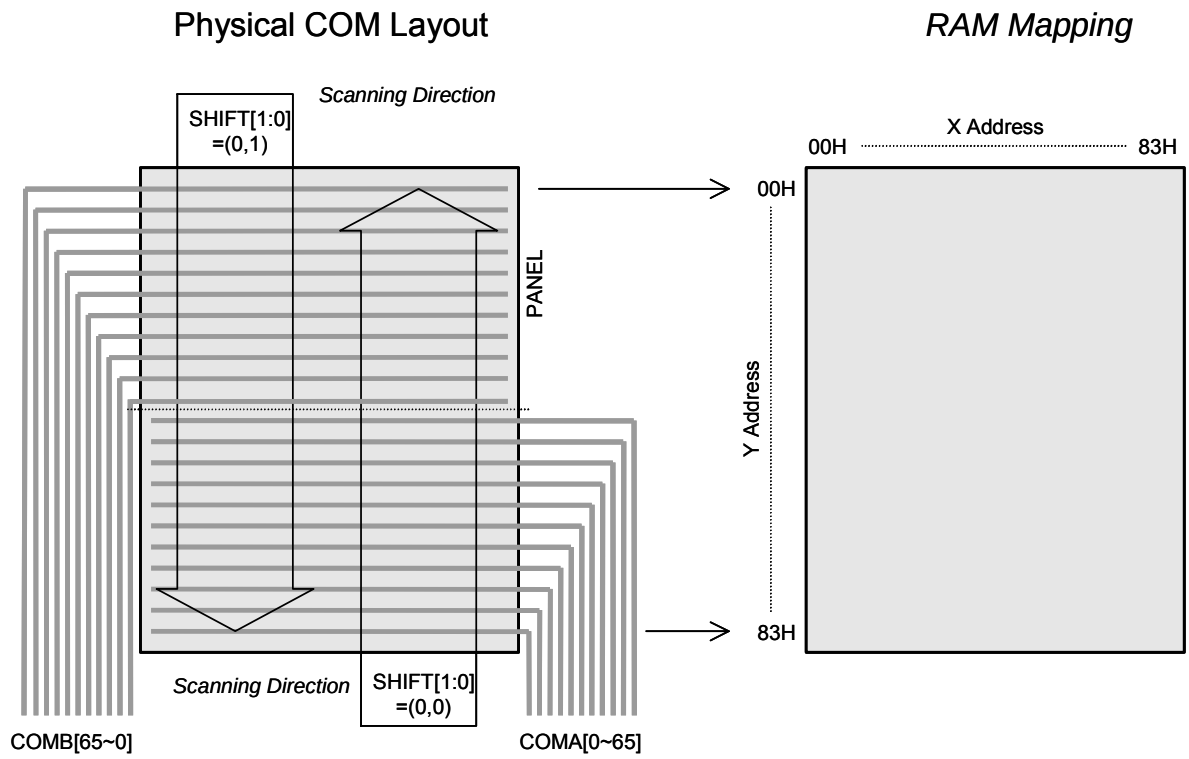
(EN3PTL= ‘1’)

VPC (Display line number)	106							
HCT (Header COM)	13							
SHIFT[1] (COM shift A/B set)	‘1’ (B start-> B end -> A start -> A end)							
SHIFT[0] (COM shift direction)	‘0’				‘1’			
SSC1 (Scan Start COM 1)	logical	0	10	36	logical	0	96	0
SSC2 (Scan Start COM 2)	COM	0	0	80	COM	0	0	11
PCC1 (Line No. of partial display 1)	number	0	0	20	number	0	0	5
PCC2 (Line No. of partial display 2)		0	0	15		0	0	15
SSC3 (Scan Start COM 3)		0	0	101		0	0	20
PCC3 (Line No. of partial display 3)		0	0	5		0	0	10

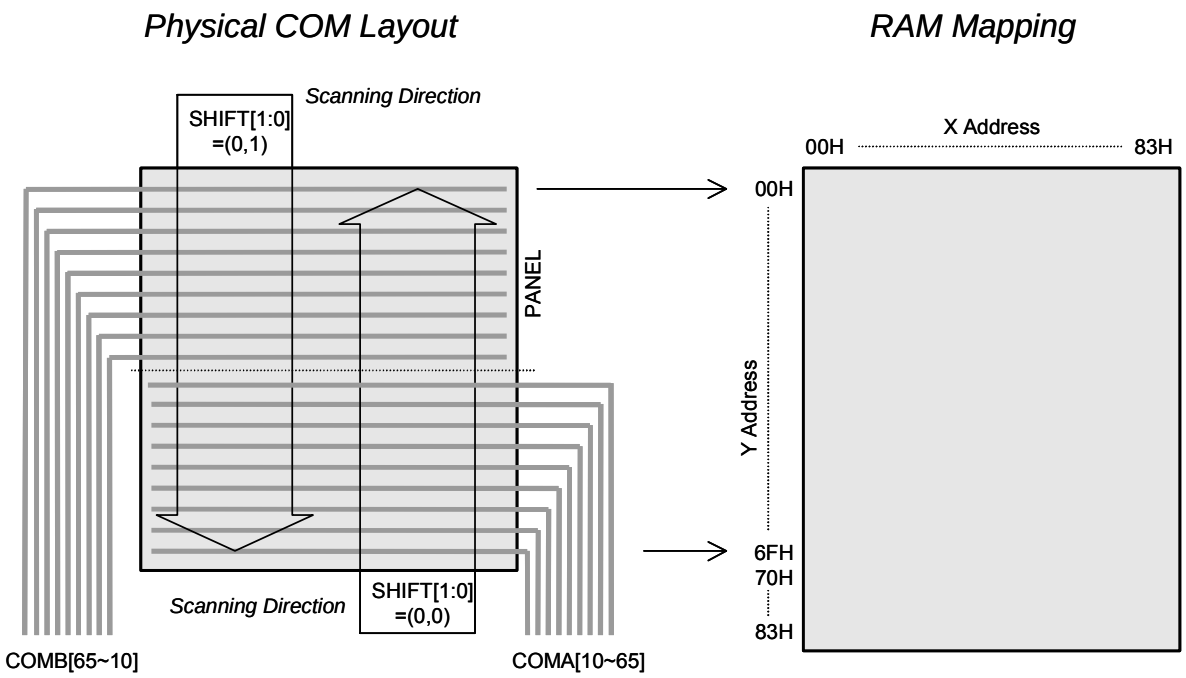
Physical COM name																		
	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B	A	B
	COMA0	COMB0	-	-							-	-						
	COMA1	COMB1	-	-							-	-						
	COMA2	COMB2	-	-							-	-						
	COMA3	COMB3	-	-							-	-						
	COMA4	COMB4	-	-							-	-						
	COMA5	COMB5	-	-							-	-						
	COMA6	COMB6	-	-							-	-						
	COMA7	COMB7	-	-							-	-						
	COMA8	COMB8	-	-							-	-						
	COMA9	COMB9	-	-							-	-						
	COMA10	COMB10	-	-							-	-						
	COMA11	COMB11	-	-							-	-						
	COMA12	COMB12	-	-							-	-						
	COMA13	COMB13	53	0	53	0	43	96	17		52	105	52	105	62	9	22	
	COMA14	COMB14	54	1	54	1	44	97	18		51	104	51	104	61	8	21	
	COMA15	COMB15	55	2	55	2	45	98	19		50	103	50	103	60	7	20	
	COMA16	COMB16	56	3	56	3	46	99			49	102	49	102	59	6		
	COMA17	COMB17	57	4	57	4	47	100			48	101	48	101	58	5		
	COMA18	COMB18	58	5	58	5	48	101			47	100	47	100	57	4		
	COMA19	COMB19	59	6	59	6	49	102			46	99	46	99	56	3		
	COMA20	COMB20	60	7	60	7	50	103			45	98	45	98	55	2		
	COMA21	COMB21	61	8	61	8	51	104			44	97	44	97	54	1		
	COMA22	COMB22	62	9	62	9	52	105			43	96	43	96	53	0		
	COMA23	COMB23	63	10	63	10	53	0			42	95	42	95	52	105		
	COMA24	COMB24	64	11	64	11	54	1			41	94	41	94	51	104		
	COMA25	COMB25	65	12	65	12	55	2			40	93	40	93	50	103		
	COMA26	COMB26	66	13	66	13	56	3			39	92	39	92	49	102		
	COMA27	COMB27	67	14	67	14	57	4			38	91	38	91	48	101		
	COMA28	COMB28	68	15	68	15	58	5			37	90	37	90	47	100		
	COMA29	COMB29	69	16	69	16	59	6			36	89	36	89	46	99		
	COMA30	COMB30	70	17	70	17	60	7			35	88	35	88	45	98		
	COMA31	COMB31	71	18	71	18	61	8			34	87	34	87	44	97		
	COMA32	COMB32	72	19	72	19	62	9			33	86	33	86	43	96		
	COMA33	COMB33	73	20	73	20	63	10			32	85	32	85	42	95		
	COMA34	COMB34	74	21	74	21	64	11			31	84	31	84	41	94		
	COMA35	COMB35	75	22	75	22	65	12			30	83	30	83	40	93		
	COMA36	COMB36	76	23	76	23	66	13			29	82	29	82	39	92		
	COMA37	COMB37	77	24	77	24	67	14			28	81	28	81	38	91		
	COMA38	COMB38	78	25	78	25	68	15			27	80	27	80	37	90		
	COMA39	COMB39	79	26	79	26	69	16			26	79	26	79	36	89		
	COMA40	COMB40	80	27	80	27	70	17	20		25	78	25	78	35	88	19	
	COMA41	COMB41	81	28	81	28	71	18	21		24	77	24	77	34	87	18	
	COMA42	COMB42	82	29	82	29	72	19	22		23	76	23	76	33	86	17	
	COMA43	COMB43	83	30	83	30	73	20	23		22	75	22	75	32	85	16	
	COMA44	COMB44	84	31	84	31	74	21	24		21	74	21	74	31	84	15	
	COMA45	COMB45	85	32	85	32	75	22	25		20	73	20	73	30	83	14	
	COMA46	COMB46	86	33	86	33	76	23	26		19	72	19	72	29	82	13	
	COMA47	COMB47	87	34	87	34	77	24	27		18	71	18	71	28	81	12	
	COMA48	COMB48	88	35	88	35	78	25	28		17	70	17	70	27	80	11	
	COMA49	COMB49	89	36	89	36	79	26	29	0	16	69	16	69	26	79	10	39
	COMA50	COMB50	90	37	90	37	80	27	30	1	15	68	15	68	25	78	9	38
	COMA51	COMB51	91	38	91	38	81	28	31	2	14	67	14	67	24	77	8	37
	COMA52	COMB52	92	39	92	39	82	29	32	3	13	66	13	66	23	76	7	36
	COMA53	COMB53	93	40	93	40	83	30	33	4	12	65	12	65	22	75	6	35
	COMA54	COMB54	94	41	94	41	84	31	34	5	11	64	11	64	21	74	5	34
	COMA55	COMB55	95	42	95	42	85	32		6	10	63	10	63	20	73		33
	COMA56	COMB56	96	43	96	43	86	33		7	9	62	9	62	19	72		32
	COMA57	COMB57	97	44	97	44	87	34		8	8	61	8	61	18	71		31
	COMA58	COMB58	98	45	98	45	88	35		9	7	60	7	60	17	70		30
	COMA59	COMB59	99	46	99	46	89	36		10	6	59	6	59	16	69		29
	COMA60	COMB60	100	47	100	47	90	37		11	5	58	5	58	15	68		28
	COMA61	COMB61	101	48	101	48	91	38	35	12	4	57	4	57	14	67	4	27
	COMA62	COMB62	102	49	102	49	92	39	36	13	3	56	3	56	13	66	3	26
	COMA63	COMB63	103	50	103	50	93	40	37	14	2	55	2	55	12	65	2	25
	COMA64	COMB64	104	51	104	51	94	41	38	15	1	54	1	54	11	64	1	24
	COMA65	COMB65	105	52	105	52	95	42	39	16	0	53	0	53	10	63	0	23

REMARK	(B -> A)	one area	one area	two area	(B <- A)	one area	one area	two area
		Normal				Reversed		

Example of panel connection 1 (HCT=00H)

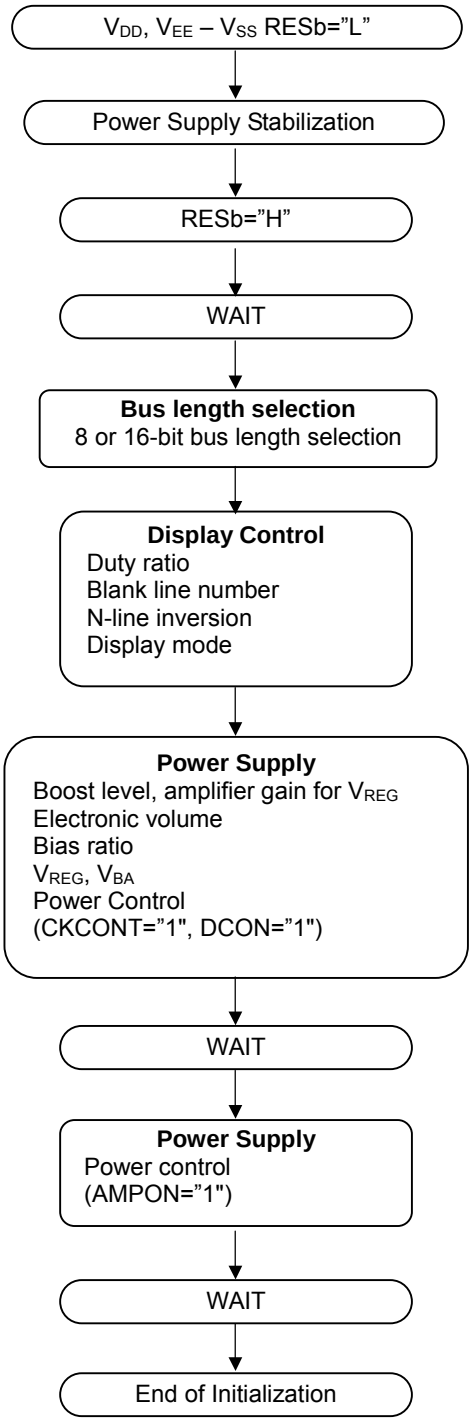


Example of panel connection 2 (HCT=0AH)



(15) TYPICAL INSTRUCTION SEQUENCES

(1) Initialization (internal power supply)



Note 1) If V_{EE} is different from V_{DD}, input V_{DD} first

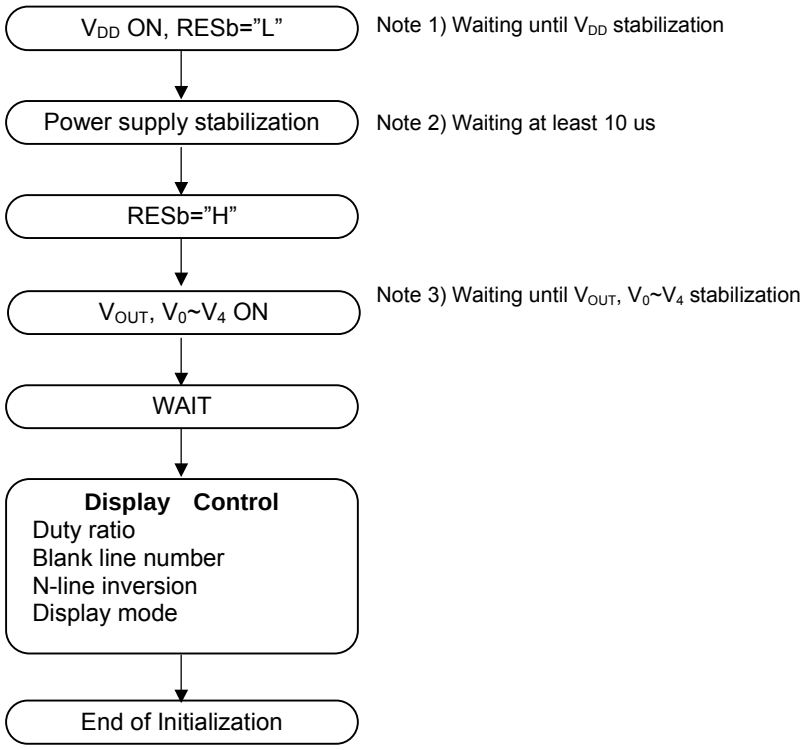
Note 2) Waiting until V_{DD} and V_{EE} stabilization

Note 3) Waiting at least 10 us

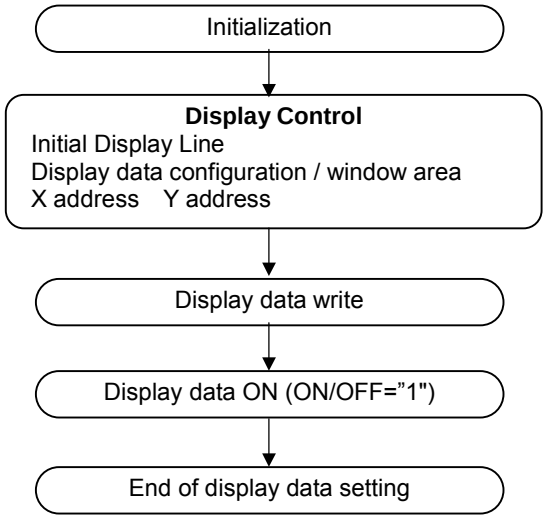
Note 4) Waiting until V_{OUT} stabilization

Note 5) Waiting until V_0 and V_1~V_4 stabilization

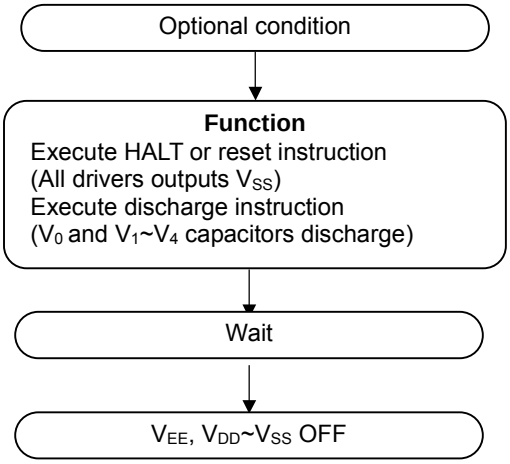
(2) Initialization (external power supply)



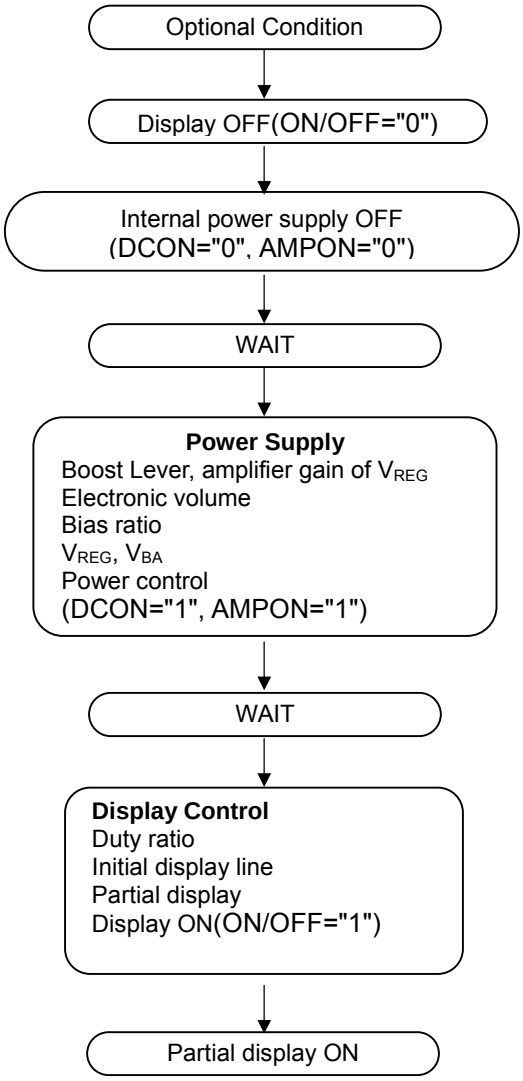
(3) Data Write



(4) Power OFF



(5) Partial Display



Note 1) Waiting until voltage booster OFF

Note 2) Waiting until V_{OUT} stabilization

Note 3) Waiting until V_{OUT} V_0 and V_1 ~V_4 stabilization

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	V_{SS}=0V Ta = +25°C	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +20.0	V
Supply Voltage (5)	V0		V0	-0.3 to +20.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to V0 + 0.3	V
Input Voltage	V_I		*1	-0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{stg}			-45 to +125	°C

Note 1) D_0 ~ D_{15}, CSb, RS, RDb, WRb, OSCI, RESb pins
Note 2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS}, V_{EE} and V_{SSH}.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	*1
	V_{DD2}		2.4		3.3	V	*2
	V_{EE}	V_{EE}	2.4		3.3	V	*3
Operating Voltage	V_0	V_0	5		18.0	V	*4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	1.59(TBD)		3.3	V	*5
Operating Temperature	T_{opr}		-30		85	°C	

Note1) Applies to the condition when the reference voltage generator is not used.
Note2) Applies to the condition when the reference voltage generator is used.
Note3) Applies to the condition when the voltage booster is used.
Note4) The following relationship among the supply voltages must be maintained.
$V_{SSH}<V_4<V_3<V_2<V_1<V_0 \leq V_{OUT}$
Note5) The relationship: $V_{REF}<V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

V_{SS} = 0V, V_{DD} = +1.7 to +3.3V, Ta = -30 to +85°C

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNIT	NOTE
High level input voltage	V_{IH}			0.8 V_{DD}		V_{DD}	V	*1
Low level input voltage	V_{IL}			0		0.2V_{DD}	V	*1
High level output voltage	V_{OH1}	I_{OH} = -0.4mA		V_{DD} - 0.4			V	*2
Low level output voltage	V_{OL1}	I_{OL} = 0.4mA				0.4	V	*2
High level output voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DD} - 0.4			V	*3
Low level output voltage	V_{OL2}	I_{OL} = 0.1mA				0.4	V	*3
Input leakage current	IL_I	V_I = V_{SS} or V_{DD}		-10		10	µA	*4
Output leakage current	IL_O	V_I = V_{SS} or V_{DD}		-10		10	µA	*5
Driver ON-resistance	R_{ON1}	$\|\Delta V_{ON}\|$ = 0.5V	V_0 = 10V		1	2	kΩ	*6
			V_0 = 6V		2	4		
Stand-by current	I_{STB}	CSb=V_{DD}, Ta=25°C	V_{DD} = 3V			15	µA	*7
Internal oscillation Frequency	f_{OSC1}	V_{DD} = 3V Ta = 25°C		TBD	730	TBD	kHz	*8
	f_{OSC2}			TBD	170	TBD		
	f_{OSC3}			TBD	1200	TBD		
	f_{OSC4}			TBD	285	TBD		
External oscillation Frequency	f_{r1}	Rf=15kΩ, V_{DD} = 3V,Ta = 25°C			730		kHz	*9
Voltage converter output voltage	V_{OUT}	N-time booster (N=2 to 6) RL = 500kΩ (V_{OUT} - V_{SS})		(N x V_{EE}) x 0.95			V	*10
Supply current (1)	I_{DD1}	V_{DD} = 3V, 6-time booster Whole ON pattern			TBD(760)	TBD(1140)	µA	*11
Supply current (2)	I_{DD2}	V_{DD} = 3V, 6-time booster Checker pattern			TBD(930)	TBD(1400)		
Supply current (3)	I_{DD3}	V_{DD} = 3V, 5-time booster Whole ON pattern			TBD(520)	TBD(780)		
Supply current (4)	I_{DD4}	V_{DD} = 3V, 5-time booster Checker pattern			TBD(650)	TBD(980)		
Supply current (5)	I_{DD5}	V_{DD} = 3V, 4-time booster Whole ON pattern			TBD(360)	TBD(540)		
Supply current (6)	I_{DD6}	V_{DD} = 3V, 4-time booster Checker pattern			TBD(450)	TBD(680)		
V_{BA} Operating voltage	V_{BA}	V_{EE} = 2.4 to 3.3V@ T=25°C		1.86	1.9	1.94	V	*12
V_{REG} Operating voltage	V_{REG}	V_{EE} = 2.4 to 3.3V V_{REF} = 1.9 N-time booster (N=2 to 6)		(V_{REF} x N) x 0.97	(V_{REF} x N)	(V_{REF} x N) x 1.03	V	*13
Output Voltage	V_2			-100	0	+100	mV	*14
	V_3			-100	0	+100		
	V_{D12}			-30	0	+30		
	V_{D34}			-30	0	+30		
	V_{D24}			-30	0	+30		

● Applicable Pins and Conditions

*1 D_0-D_{15}, CSb, RS, RDb, WRb, PS, SEL68, RESb

*2 D_0-D_{15}

*3 LP, FLM, M

*4 CSb, RS, SEL68, RDb, WRb, PS, RESb, OSCI

*5 D_0-D_{15} , M, FLM, LP in the high impedance

*6 $SEGA_0$-$SEGA_{131}$, $SEGB_0$-$SEGB_{131}$, $SEGC_0$-$SEGC_{131}$, $COMA_0$-$COMA_{65}$, $COMB_0$-$COMB_{65}$
Defines the resistance between the COM/SEG terminals and the power supply terminals (V_0, V_1, V_2, V_3 and V_4) at the condition of 0.5V deference and 1/9 LCD bias ratio.

*7 V_{DD}
The oscillator is halted, CSb="1" (disabled), No-load on the COM/SEG drivers

*8 f_{OSCI}
- Defines the internal oscillation frequency at (CRF, CRS1, CRS0) = (0, 0, 0).

f_{OSC2}
- Defines the internal oscillation frequency at (CRF, CRS1, CRS0) = (0, 0, 1).

f_{OSC3}
- Defines the internal oscillation frequency at (CRF, CRS1, CRS0) = (1, 0, 0).

f_{OSC4}
- Defines the internal oscillation frequency at (CRF, CRS1, CRS0) = (1, 0, 1).

*9 f_{r1}
- Defines the internal oscillation frequency at (CRF, CRS1, CRS0) = (0, 1, 0).

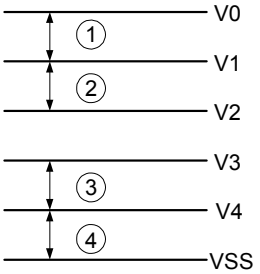
*10 V_{OUT}
- N x boosting (N=2~6), applicable under internal oscillator circuit and internal power circuit are ON state.
- V_{EE}=2.4V to 3.3V, EVR= (1,1,1,1,1,1,1), 1/5 to 1/12 LCD bias, duty is 1/132 , No loads on COM/SEG drivers.
- RL=500KΩ between the V_{OUT} and the V_{SS}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1"

*11 V_{DD}
- Applies to the condition using the internal oscillator and internal power circuits, no access between the LSI and MPU. EVR value is '1,1,1,1,1,1,1'.
Driving patterns are 'all pixels turned-on' or 'checkerboard' display in grayscale mode.
No load are connected on the COM/SEG drivers.
- V_{DD}=V_{EE}, V_{REF}=0.9V_{EE}, CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="1", AMPON="1", NLIN="0", 1/132 Duty cycle, Ta=25°C

*12 V_{BA}
V_{EE}=2.4V to 3.3V , Ta=25°C

*13 V_{REG}
- V_{EE}=2.4V to 3.3V, V_{REF}=1.9(external)V, V_{OUT}=18V, bias ratio is from 1/5 to 1/12, 1/132 duty cycle, EVR=(1,1,1,1,1,1,1), Checkerboard display, No-load on the COM/SEG drivers, the voltage booster N=2 to 6. CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1", NLIN="0"

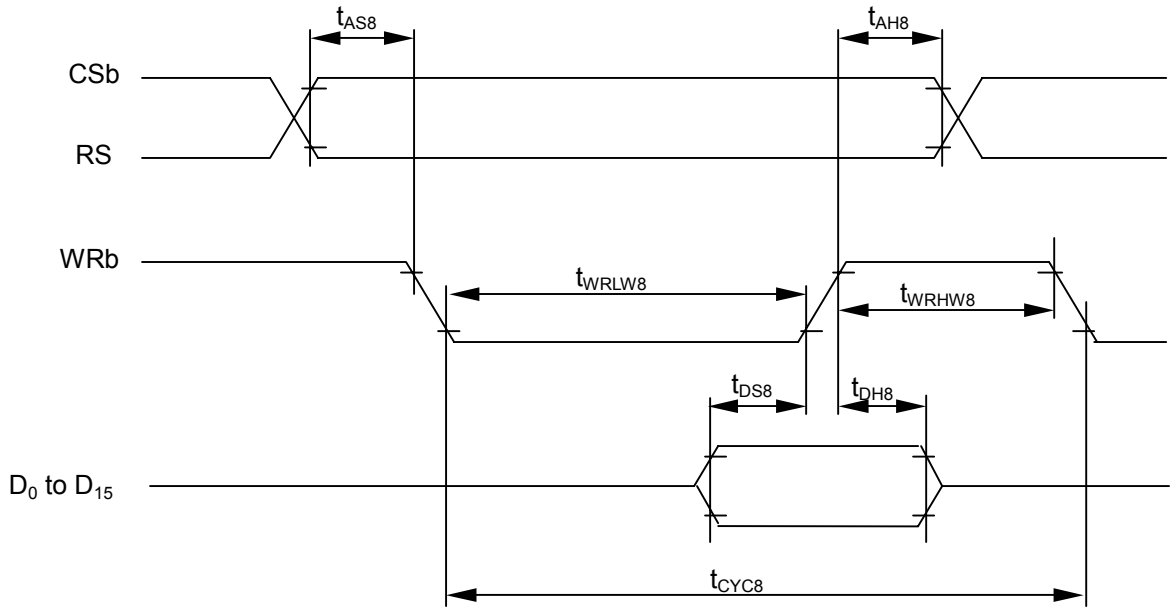
*14 V0, V_1, V_2, V_3, V_4
- V_{EE}=3.0V, V_{REF}=0.9V_{EE}, V_{OUT}=15V, 1/5 to 1/12 LCD Bias, EVR= (1,1,1,1,1,1,1), Display OFF, No-load on the COM/SEG drivers, voltage booster N=5. CA_1=CA_2=1.0uF, CA_3=0.1uF, DCON="0", AMPON="1"



VD12 = ① - ②
VD34 = ③ - ④
VD24 = ② - ④ (VD24 is applied to the condition that VD12 and VD34 are out of specifications.)

■ AC CHARACTERISTICS

(1) Write operation (80-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

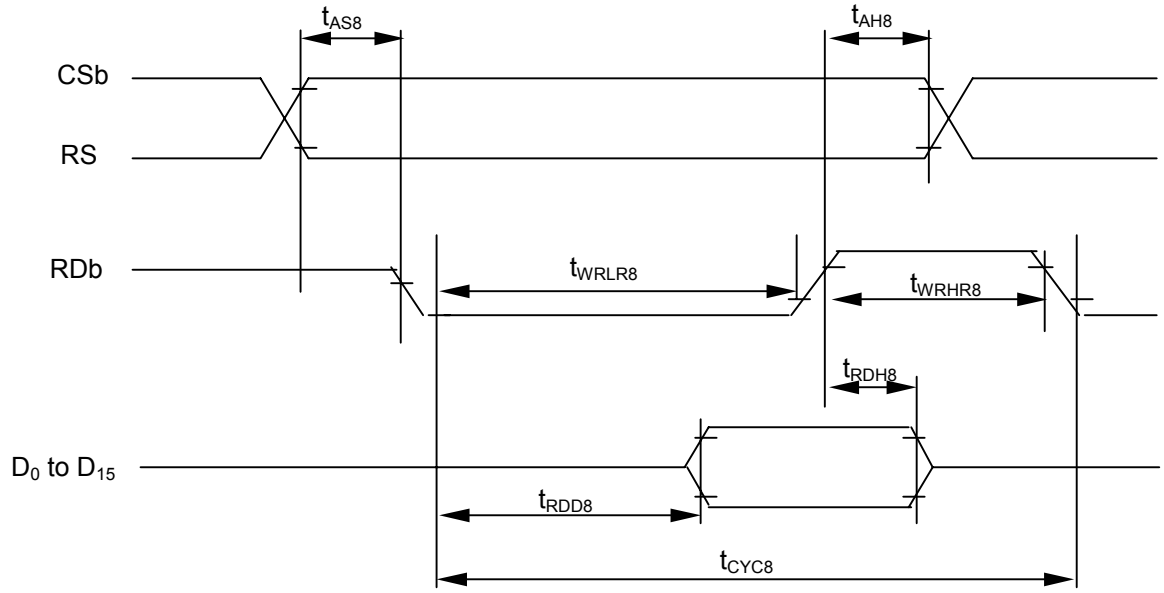
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		240		ns	
Enable ”L” level pulse width	t_{WRLW8}		110		ns	WRb
Enable ”H” level pulse width	t_{WRHW8}		110		ns	
Data setup time	t_{DS8}		60		ns	D_0 to D_{15}
Data hold time	t_{DH8}		15		ns	

(V_{DD}=1.7 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		300		ns	
Enable ”L” level pulse width	t_{WRLW8}		95		ns	WRb
Enable ”H” level pulse width	t_{WRHW8}		95		ns	
Data setup time	t_{DS8}		80		ns	D_0 to D_{15}
Data hold time	t_{DH8}		20		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

(2) Read operation (80-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

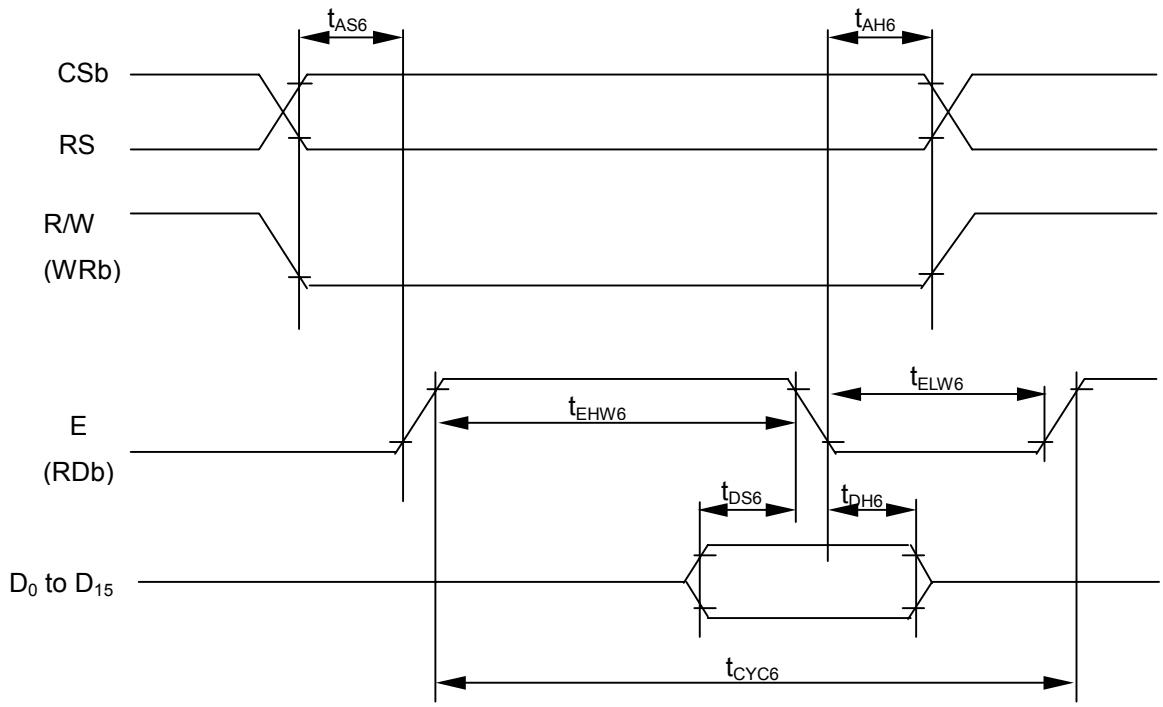
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		260		ns	
Enable ”L” level pulse width	t_{WRLR8}		120		ns	RDb
Enable ”H” level pulse width	t_{WRHR8}		120		ns	
Read Data delay time	T_{RDD8}	CL=15pF		90	ns	D_0 to D_{15}
Read Data hold time	T_{RDH8}		0		ns	

(V_{DD}=1.7 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		360		ns	
Enable ”L” level pulse width	t_{WRLR8}		170		ns	RDb
Enable ”H” level pulse width	t_{WRHR8}		170		ns	
Read Data delay time	t_{RDD8}	CL=15pF		150	ns	D_0 to D_{15}
Read Data hold time	t_{RDH8}		0		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

(3) Write operation (68-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

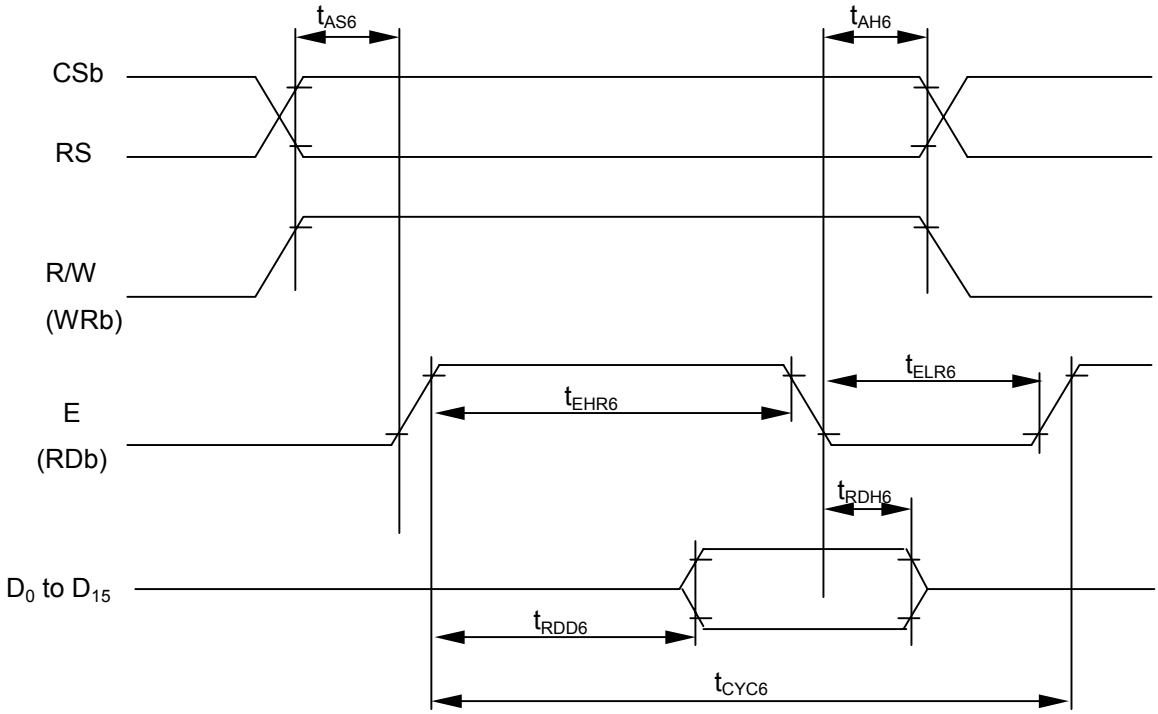
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		240		ns	
Enable ”L” level pulse width	t_{ELW6}		110		ns	E
Enable ”H” level pulse width	t_{EHW6}		110		ns	
Data setup time	t_{DS6}		70		ns	D_0 to D_{15}
Data hold time	t_{DH6}		15		ns	

(V_{DD}=1.7 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		300		ns	
Enable ”L” level pulse width	t_{ELW6}		95		ns	E
Enable ”H” level pulse width	t_{EHW6}		95		ns	
Data setup time	t_{DS6}		80		ns	D_0 to D_{15}
Data hold time	t_{DH6}		20		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

(4) Read operation (68-type MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

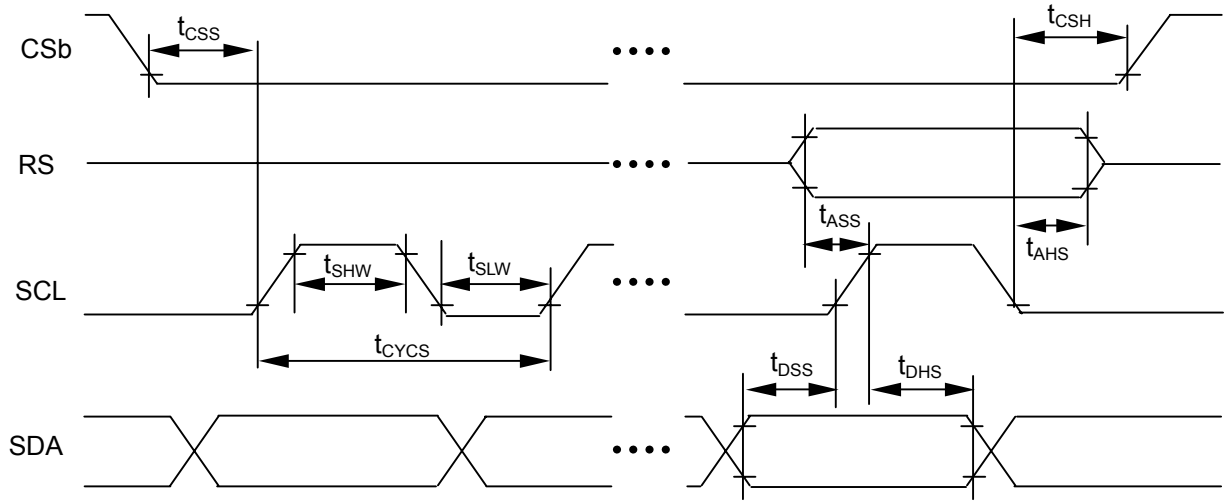
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		260		ns	
Enable ”L” level pulse width	t_{ELR6}		120		ns	E
Enable ”H” level pulse width	t_{EHR6}		120		ns	
Read Data delay time	t_{RDD6}	CL=15pF		100	ns	D_0 to D_{15}
Read Data hold time	t_{RDH6}		0		ns	

(V_{DD}=1.7 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		360		ns	
Enable ”L” level pulse width	t_{ELR6}		170		ns	E
Enable ”H” level pulse width	t_{EHR6}		170		ns	
Read Data delay time	t_{RDD6}	CL=15pF		150	ns	D0 to D15
Read Data hold time	t_{RDH6}		0		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

(5) Serial interface



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

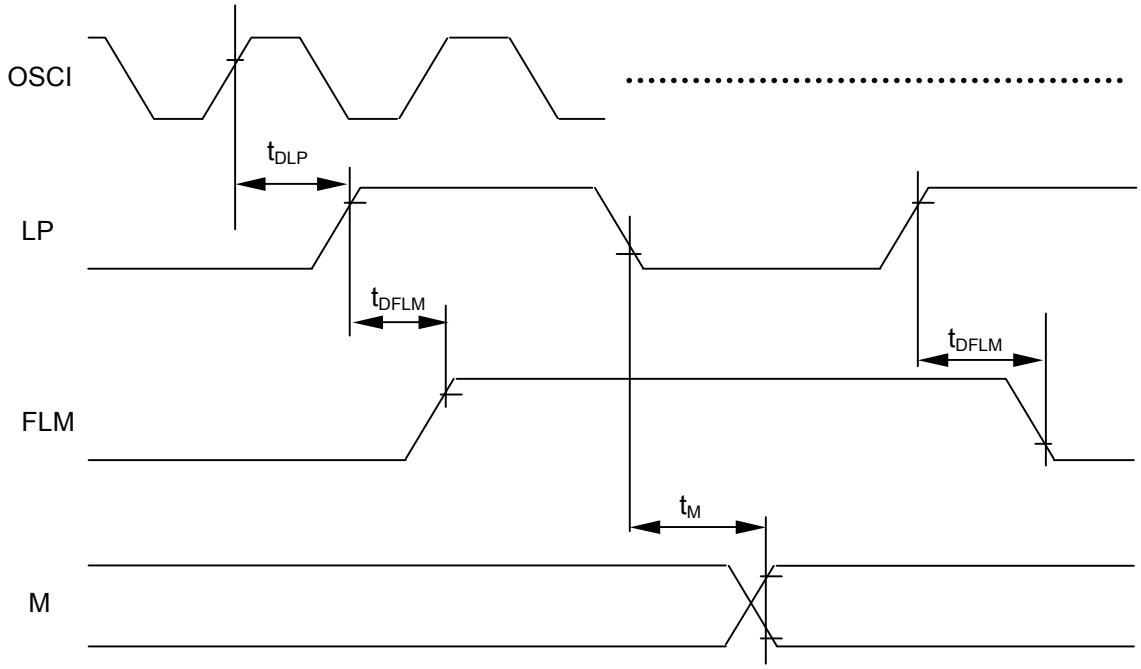
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		TBD(75)		ns	SCL
SCL "H" level pulse width	t_{SHW}		TBD(33)		ns	
SCL "L" level pulse width	t_{SLW}		TBD(33)		ns	
Address setup time	t_{ASS}		TBD(33)		ns	RS
Address hold time	t_{AHS}		TBD(33)		ns	
Data setup time	t_{DSS}		TBD(33)		ns	SDA
Data hold time	t_{DHS}		TBD(33)		ns	
CSb – SCL time	t_{CSS}		TBD(33)		ns	CSb
CSb hold time	t_{CSH}		TBD(33)		ns	

(V_{DD}=1.7 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		TBD(120)		ns	SCL
SCL "H" level pulse width	t_{SHW}		TBD(55)		ns	
SCL "L" level pulse width	t_{SLW}		TBD(55)		ns	
Address setup time	t_{ASS}		TBD(55)		ns	RS
Address hold time	t_{AHS}		TBD(55)		ns	
Data setup time	t_{DSS}		TBD(55)		ns	SDA
Data hold time	t_{DHS}		TBD(55)		ns	
CSb – SCL time	t_{CSS}		TBD(55)		ns	CSb
CSb hold time	t_{CSH}		TBD(55)		ns	

Note) Each timing is specified based on 20% and 80% of V_{DD}.

(6) Display control timing



Output timing (V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

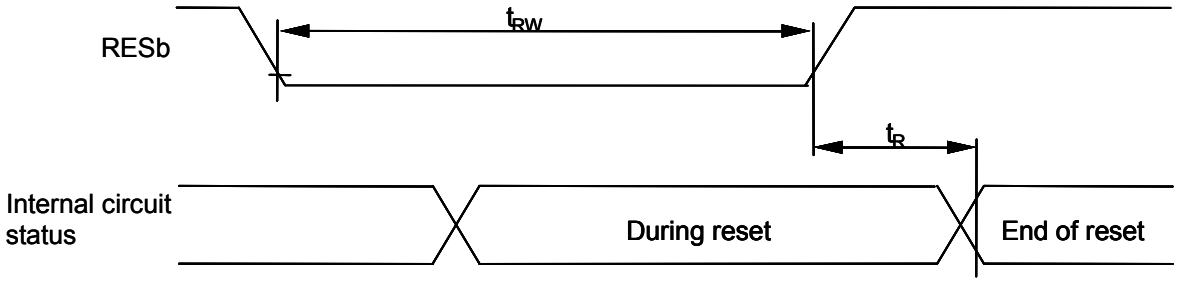
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Output timing (V_{DD}=1.7 to 2.5V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DFLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

Note) Each timing is specified based on 20% and 80% of V_{DD}.

(7) Reset input timing



(V_{DD}=2.4 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

(V_{DD}=1.7 to 2.4V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	µs	
RESb "L" level pulse width	t_{RW}		10.0		µs	RESb

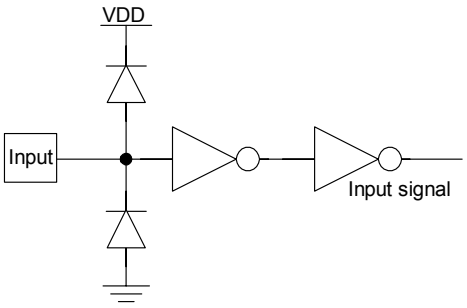
Note) Each timing is specified based on 20% and 80% of V_{DD}.

■ INPUT/OUTPUT BLOCK DIAGRAM

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Basic delay time of gate	Ta=+25°C, V_{SS}=0V, V_{DD}=3.0V		10		ns

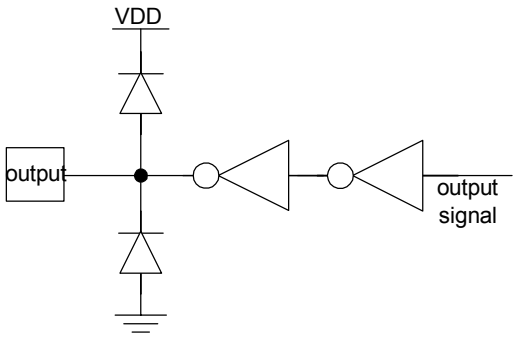
I/O circuit types

(a) Input Circuit



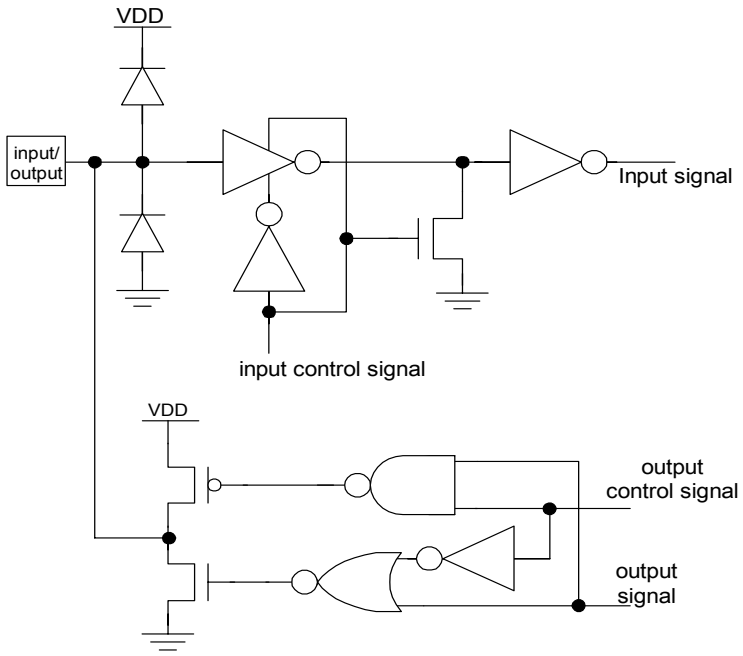
Applicable Pins : CSb, RS RDb, WRb, SEL68, P/S, RESb, TEST, OSCI

(b) Output Circuit



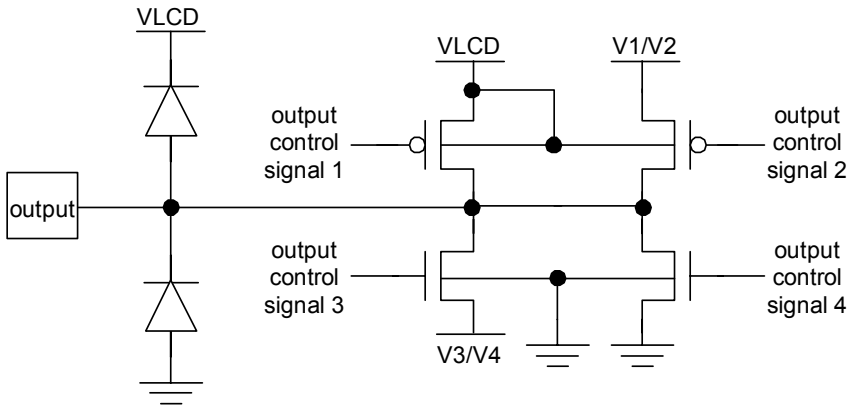
Applicable Pins : FLM, LP, M, OSCO

(c) Input/Output Circuit



Applicable Pins : D0 ~ D15,

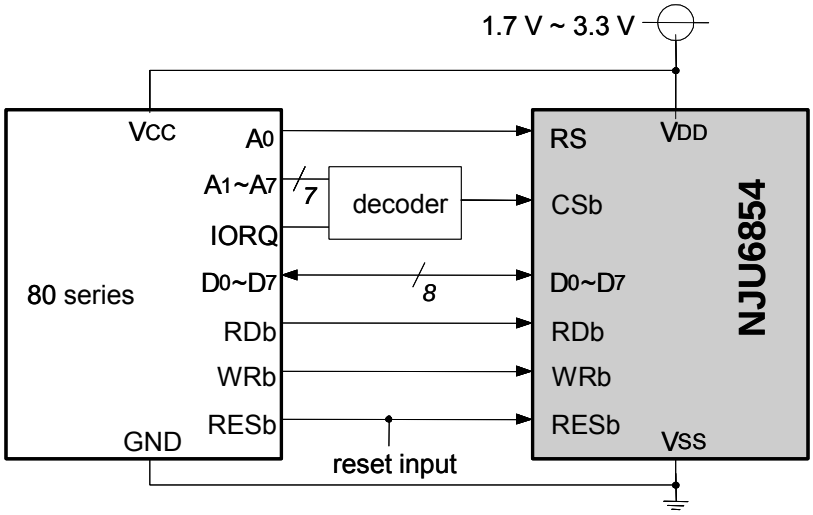
(d) LCD Drive Circuit for Graphic Display



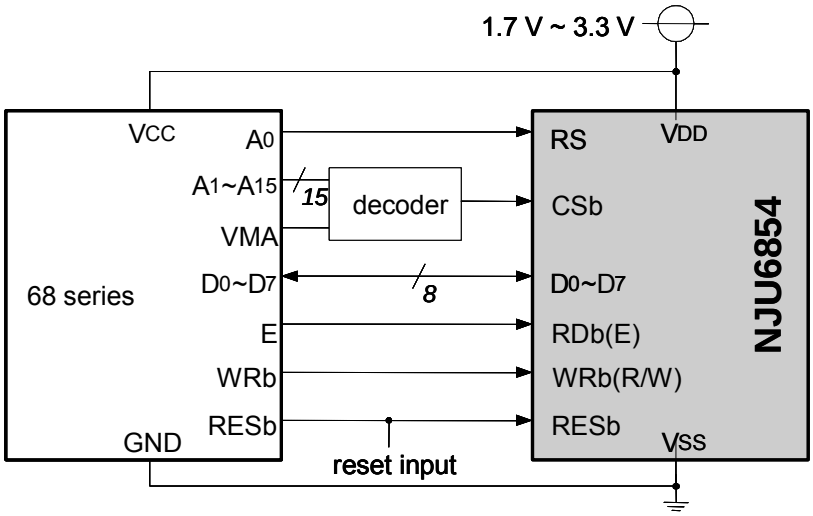
Applicable Pins : $SEGA_0$ to $SEGA_{131}$
$SEGB_0$ to $SEGB_{131}$
$SEGC_0$ to $SEGC_{131}$
$COMA_0$ to $COMA_{65}$
$COMB_0$ to $COMB_{65}$

■ MPU Connections

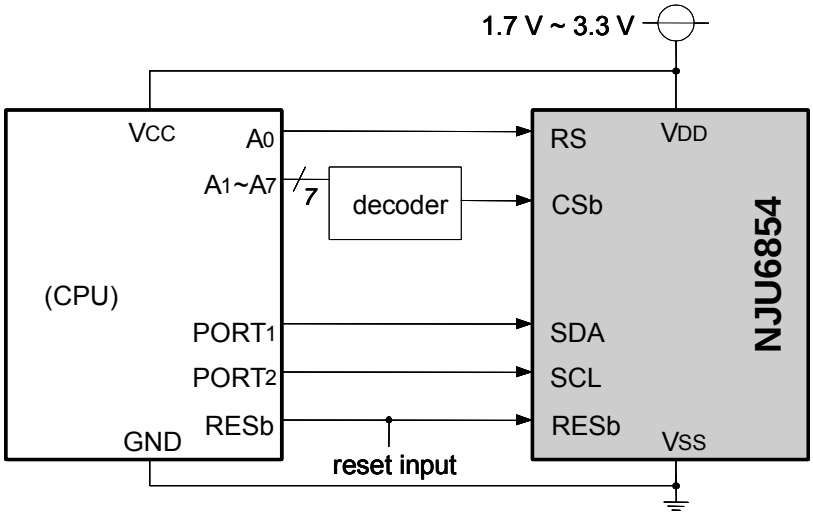
80-type MPU interface



68-type MPU interface



Serial interface



Memo