ELECTRONICS, INC.
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NTE5538
Silicon Controlled Rectifier (SCR)
800V_{DRM}, 50A

Description:
The NTE5538 general purpose SCR is suited for power supplies up to 400H_Z on resistive or inductive loads.

Features:
- Glass Passivated Chip
- High Stability and Reliability
- High Surge Capability
- High On–State Current
- Easy Mounting on Heatsink
- Isolated Package: Insulating Voltage 2500V_{RMS}

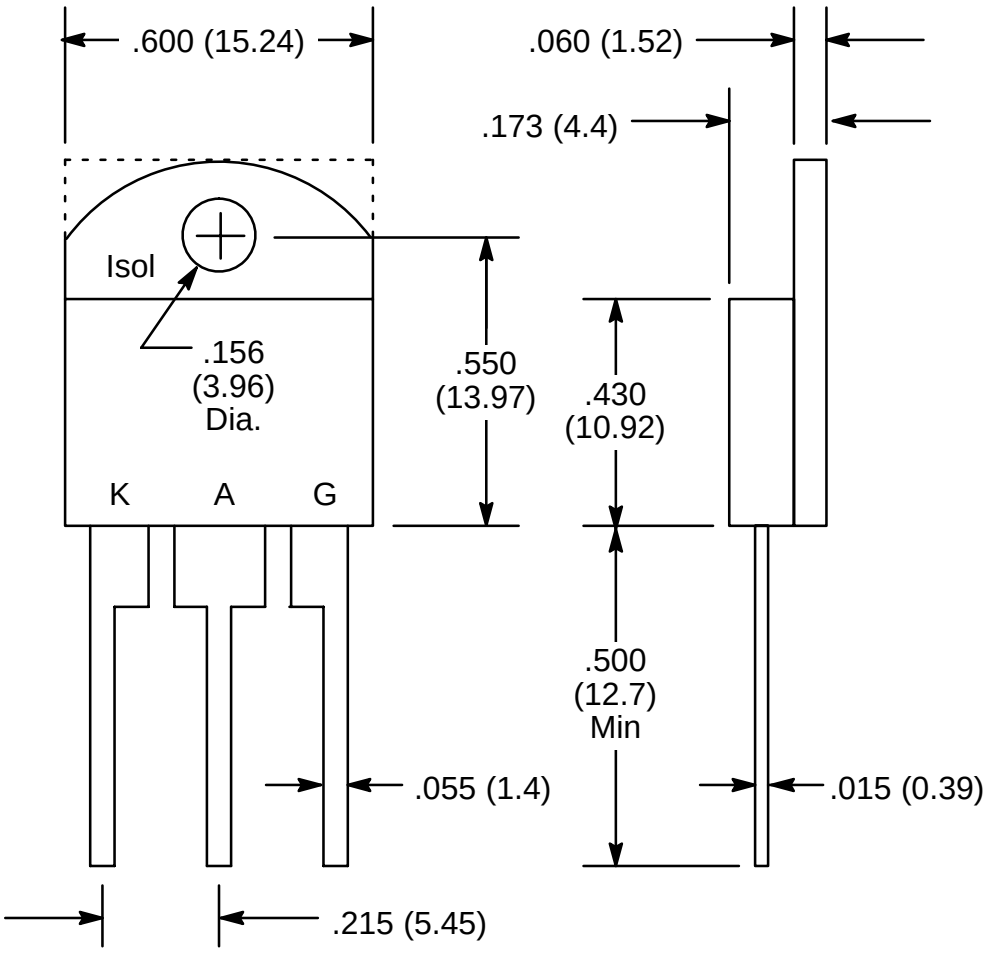
Absolute Maximum Ratings:
Peak Forward Blocking Voltage (T_J = +125°C), V_{DRM} 800V
Peak Reverse Blocking Voltage (T_J = +125°C), V_{RRM} 800V
RMS On–State Current (T_C = +70°C, Note 1), $I_{T\ (RMS)}$ 50A
Average On–State Current (T_C = +70°C, Note 1), $I_{T(AV)}$ 32A
Non–Repetitive Surge Peak On–State Current (T_J initial = +25°C, Note 2), I_{TSM}
(t = 8.3ms) 525A
(t = 10ms) 500A
I^2t Value (t = 10ms), I^2t . . . . . 1250A^2sec
Critical Rate of Rise of On–State Current (Note 3), di/dt 100A/μs
Storage and Operating Junction Temperature Range, T_{stg}, T_J . . . . . –40° to +125°C
Thermal Resistance
Junction–to–Case for DC, R_{thJC} . . . . . 1°C/W
Contact (Case–to–Heatsink), R_{thCH} . . . . . 0.2°C/W

Note 1. Single phase circuit, 180° conducting angle.
Note 2. Half sine wave.
Note 3. I_G = 800mA, di_G/dt = 1A/μs.

Gate Characteristics: (Maximum Values)
Peak Gate Power (t = 10μs), P_{GM} 50W
Average Gate Power Dissipation, $P_{G\ (AV)}$ 1W
Peak Forward Gate Current (t = 10μs), I_{FGM} 2A
Peak Forward Gate Voltage (t = 10μs), V_{FGM} 15V
Peak Reverse Gate Voltage, V_{RGM} 5V

Electrical Characteristics: (T_J = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Gate Trigger Current	I_{GT}	V_D = 12V, R_L = 33Ω, $t_p \geq 20\mu s$		–	–	80	mA
Gate Trigger Voltage	V_{GT}			–	–	1.5	V
Gate Non–Trigger Voltage	V_{GD}	T_J = +125°C, V_D = 800V, R_L = 3.3kΩ		0.2	–	–	V
Holding Current	I_H	I_T = 0.5A, Gate Open		–	20	150	mA
Peak On–State Voltage	V_{TM}	I_{TM} = 100A, t_p = 10ms		–	–	1.9	V
Forward Leakage Current	I_{DRM}	V_{DRM} = 800V		–	–	0.02	mA
			T_J = +125°C	–	–	6.0	mA
Reverse Leakage Current	I_{RRM}	V_{DRM} = 800V		–	–	0.02	mA
			T_J = +125°C	–	–	6.0	mA
Total Turn–On Time	t_{gt}	I_T = 80A, V_D = 800V, I_G = 200mA, di_G/dt = 0.2A/µs		–	2	–	µs
Turn–Off Time	t_q	T_J = +125°C, I_T = 80A, V_R = 75V, V_D = 536V, di_R/dt = 30A/µs, dv/dt = 20V/µs, Gate Open		–	100	–	µs
Critical Rate of Rise of Off–State Voltage	dv/dt	T_J = +125°C, V_{DRM} = 536V, Gate Open, Linear Slope Up		500	–	–	V/µs



NOTE: Dotted line indicates that case may have square corners.