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NTE7096 & NTE7097
Integrated Circuit
Current Mode Pulse Width Modulator (PWM)
Control Circuit

Description:

The NTE7096 and NTE7097 are integrated circuits in 8–Lead DIP type packages that incorporate a new precision temperature–controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty–cycle clamp eliminates any need for an external oscillator when at, or near, a 50% duty–cycle condition. Duty–cycles greater than 50% are also possible. Special logic ensures that V_{ref} is stabilized before the output stage is enabled. Ion–implant resistors provide tighter control of under–voltage lockout.

Other features include low start–up current, pulse–by–current limiting, and high–current totem pole output for driving capacitive loads, such as the gate of a power MOSFET. The output is low in the off state, consistent with N–channel devices.

Features:

- Optimized for Off–Line Control
- Internally Trimmed Temperature Compensated Oscillator
- Maximum Duty–Cycle Clamp
- V_{ref} Stabilized before Output Stage is Enabled
- Low Start–Up Current
- Pulse–by Pulse Current Limiting
- Improved U/V Lockout
- Double Pulse Suppression
- 1% Trimmed Bandgap Reference
- High Current Totem Pole Output

Absolute Maximum Ratings:

Supply Voltage (I_{CC} < 30mA) . . . . Self Limiting
Supply Voltage (Low Impedence Source) 30V
Output Current . . . . ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pin2, Pin3) . . . . –0.3V to V_{CC}
Error Amp Output Sink Current 10mA

Elecrtrical Characteristics: ($0° \le T_A \le +70°C$, V_{CC} = 15V, R_t = 680Ω, C_t = .022µF, Note 1 unless otherwise specified)

Parameter	Test Conditions	Min	Typ	Max	Unit
Reference Section					
Output Voltage	T_J = +25°C, I_O = 1mA	4.9	5.0	5.1	V
Line Regulation	12V ≤ V_{IN} ≤ 25V	–	6	20	mV
Load Regulation	1mA ≤ I_O ≤ 20mA	–	6	25	mV
Temperature Stability	Note 2	–	0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temperature, Note 2	4.82	–	5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz, T_J = +25°C, Note 2	–	50	–	µV
Long Term Stability	T_A = +125°C, 1000Hrs., Note 2	–	5	25	mV
Output Short Circuit	T_A = +25°C	–30	–100	–180	mA
Oscillator Section					
Initial Accuracy	T_J = +25°C	47	52	57	kHz
Voltage Stability	12V ≤ V_{CC} ≤ 25V	–	0.2	1.0	%
Temperature Stability	0° ≤ T_A ≤ +70°C, Note 2	–	5	–	%
Amplitude	V_{PIN4} peak to peak	–	1.7	–	V
Discharge Current	T_J = +25°C	7.8	8.3	8.8	mA
	0° ≤ T_A ≤ +70°C	7.6	–	9.0	mA
Error Amp Section					
Input Voltage	V_{PIN1} = 2.5V	2.42	2.50	2.58	V
Input Bias Current		–	–0.3	–2.0	µA
A_{VOL}	2V ≤ V_O ≤ 4V	65	90	–	dB
Unity Gain Bandwidth	Note 2	0.7	1.0	–	MHz
PSRR	12V ≤ V_{CC} ≤ 25V	60	70	–	dB
Output Sink Current	V_{PIN2} = 2.7V, V_{PIN1} = 1.1V	2	6	–	mA
Output Source Current	V_{PIN2} = 2.3V, V_{PIN1} = 5V	–0.5	–0.8	–	mA
V_{OUT} High	V_{PIN2} = 2.3V, R_L = 15K to GND	5	6	–	V
V_{OUT} Low	V_{PIN2} = 2.7V, R_L = 15K to Pin8	–	0.7	1.1	V
Current Sense Section					
Gain	Note 3, Note 4	2.85	3.00	3.15	V/V
Maximum Input Signal	V_{PIN1} = 5V, Note 3	0.9	1.0	1.1	V
PSRR	12V ≤ V_{CC} ≤ 25V, Note 3	–	70	–	dB
Input Bias Current		–	–2	–10	µA
Delay to Output	T_J = +25°C, Note 2	–	150	300	ns
Output Section					
Output Low Level	I_{SINK} = 20mA	–	0.1	0.4	V
	I_{SINK} = 200mA	–	1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13.0	13.5	–	V
	I_{SOURCE} = 200mA	12.0	13.5	–	V
Rise Time	T_J = +25°C,C_L = 1nF, Note 2	–	50	150	ns
Fall Time	T_J = +25°C,C_L = 1nF, Note 2	–	50	150	ns
Output Leakage	V_{CC} = 14V, UVLO Active, V_{PIN6} = 0	–	–0.01	–10	µA
Total Standby Current					
Start–Up Current		–	0.5	1.0	mA
Operating Supply Current	V_{PIN2} = V_{PIN3} = 0V, R_T = 10K, C_T = 3.3nF	–	11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA	–	34	–	V

Parameter	Test Conditions	Min	Typ	Max	Unit
Under–Voltage Lockout Section					
Start Threshold NTE7096		14.5	16.0	17.5	V
NTE7097		7.8	8.4	9.0	V
Minimum Operating Voltage NTE7096	After Turn On	8.5	10.0	11.5	V
NTE7097		7.0	7.9	8.2	V

Note 1. Adjust V_{CC} above the start threshold before setting at 15V.
Note 2. These parameters, although guaranteed, are not 100% tested in production.
Note 3. Parameter measured at trip point of latch with $V_{PIN2} = 0$.
Note 4. Gain defined as:

$$A = \frac{\Delta V_{PIN1}}{\Delta V_{PIN3}} \; ; 0 \le V_{PIN3} \le 0.8V$$

Pin Connection Diagram