PHP83N03LT; PHB83N03LT; PHE83N03LT

N-channel TrenchMOS transistor

Rev. 01 — 23 January 2001 **Product specification**

1. Description

N-channel logic level field-effect power transistor in a plastic package using TrenchMOS™1 technology.

Product availability:

PHP83N03LT in a SOT78 (TO-220AB)

PHB83N03LT in a SOT404 (D^2-PAK)

PHE83N03LT in a SOT226 (I^2-PAK).

2. Features

- Low on-state resistance
- Fast switching.

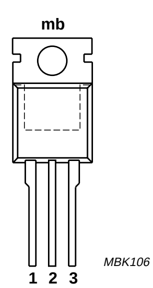
3. Applications

- High frequency computer motherboard DC to DC converters

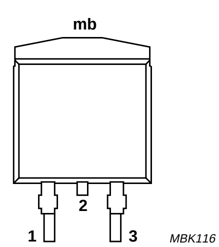
4. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT226 simplified outline and symbol

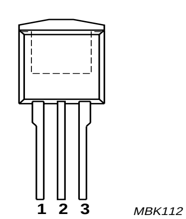
Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		



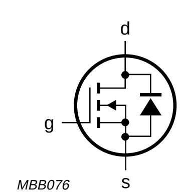
SOT78 (TO-220AB)



SOT404 (D^2-PAK)



SOT226 (I^2-PAK)



[1] It is not possible to make connection to pin 2 of the SOT404 package.

1. TrenchMOS is a trademark of Royal Phillips Electronics.

5. Quick reference data

Table 2: Quick reference data

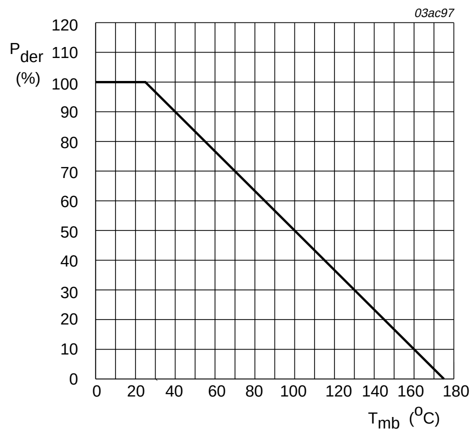
Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 175 °C	–	25	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V	–	75	A
P_{tot}	total power dissipation	T_{mb} = 25 °C	–	115	W
T_j	junction temperature		–	175	°C
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C	6.5	9	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C	10	12	mΩ

6. Limiting values

Table 3: Limiting values

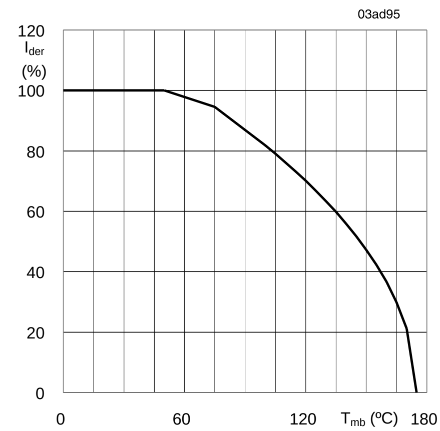
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 175 °C	–	25	V
V_{DGR}	drain-gate voltage (DC)	T_j = 25 to 175 °C; R_{GS} = 20 kΩ	–	25	V
V_{GS}	gate-source voltage (DC)		–	±15	V
V_{GSM}	gate-source voltage	$t_p \leq$ 50 µs; pulsed; duty cycle 25%; $T_j \leq$ 150 °C	–	±20	V
I_D	drain current (DC)	T_{mb} = 25 °C; V_{GS} = 5 V; Figure 2 and 3	–	75	A
		T_{mb} = 100 °C; V_{GS} = 5 V; Figure 2	–	61	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs; Figure 3	–	240	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	–	115	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	–	75	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; $t_p \leq$ 10 µs	–	240	A
Avalanche ruggedness					
E_{AS}	non-repetitive avalanche energy	unclamped inductive load; I_D = 75 A; t_p = 0.1 ms; V_{DD} = 15 V; R_{GS} = 50 Ω; V_{GS} = 5V; starting T_j = 25 °C	–	120	mJ
I_{AS}	non-repetitive avalanche current	unclamped inductive load; V_{DD} = 15 V; R_{GS} = 50 Ω; V_{GS} = 5 V; starting T_j = 25 °C	–	75	A



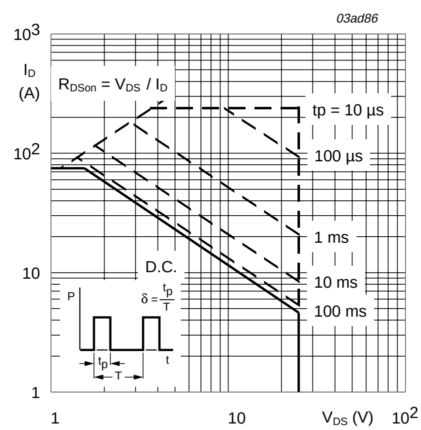
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	60	K/W
		vertical in still air; SOT226 package	65	K/W
		mounted on a printed circuit board; minimum footprint; SOT404 and SOT226 packages	50	K/W

7.1 Transient thermal impedance

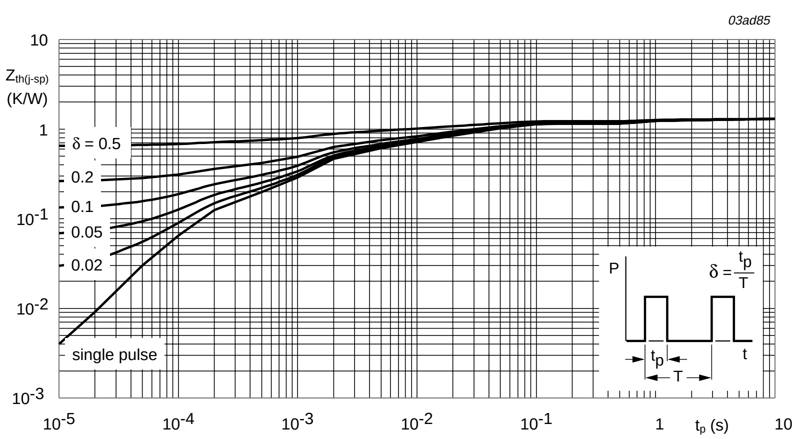
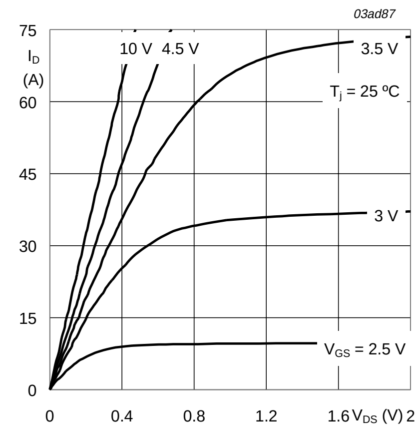


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

8. Characteristics

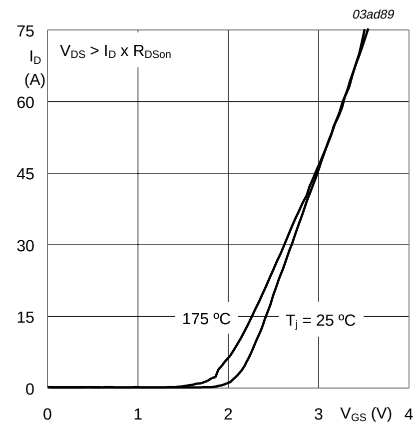
Table 5: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V				
		T_j = 25 °C	25	–	–	V
		T_j = –55 °C	22	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	–	–	V
		T_j = –55 °C	–	–	2.3	V
I_{DSS}	drain-source leakage current	V_{DS} = 25 V; V_{GS} = 0 V				
		T_j = 25 °C	–	0.05	10	µA
		T_j = 175 °C	–	–	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	–	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 25 A; Figure 7 and 8				
		T_j = 25 °C	–	10	12	mΩ
		T_j = 175 °C	–	17	20.5	mΩ
		V_{GS} = 10 V; I_D = 25 A				
		T_j = 25 °C	–	6.5	9	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 25 V; I_D = 30 A; Figure 11	–	55	–	S
$Q_{g(tot)}$	total gate charge	I_D = 30 A; V_{DD} = 15 V; V_{GS} = 5 V; Figure 14	–	33	–	nC
Q_{gs}	gate-source charge		–	7	–	nC
Q_{gd}	gate-drain (Miller) charge		–	12.5	–	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 12	–	1660	–	pF
C_{oss}	output capacitance		–	590	–	pF
C_{rss}	reverse transfer capacitance		–	380	–	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 15 V; I_D = 1 A; V_{GS} = 10 V; R_G = 6 Ω; resistive load	–	9	20	ns
t_r	turn-on rise time		–	14	30	ns
$t_{d(off)}$	turn-off delay time		–	75	95	ns
t_f	turn-off fall time		–	60	80	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 25 A; V_{GS} = 0 V; Figure 13	–	0.9	1.2	V
		I_S = 40 A; V_{GS} = 0 V	–	0.95	–	V



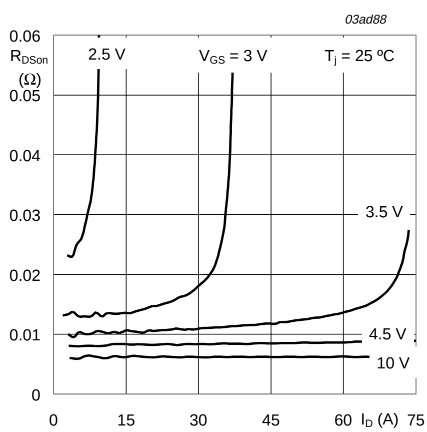
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



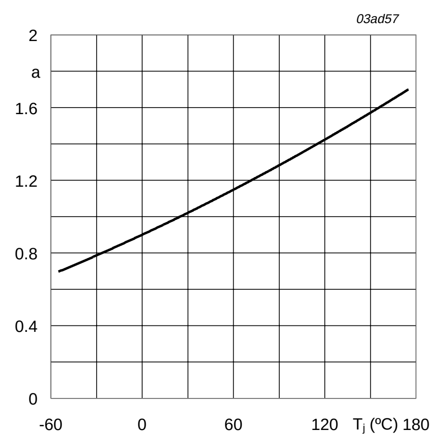
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



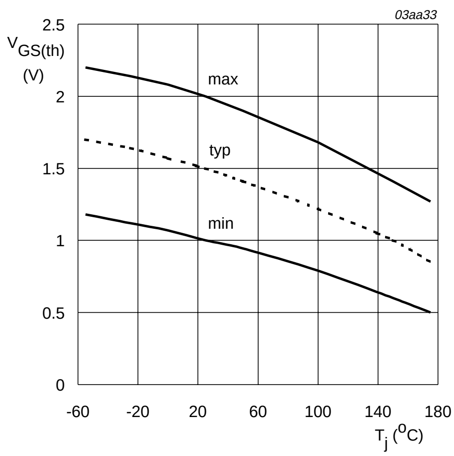
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



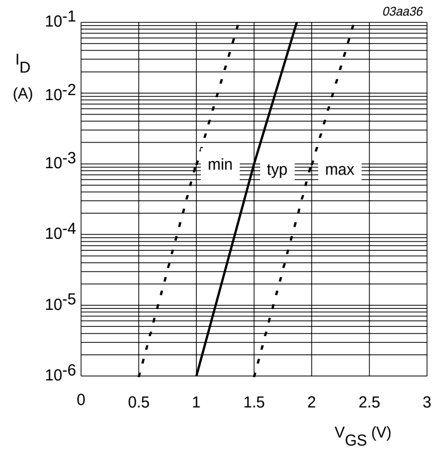
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



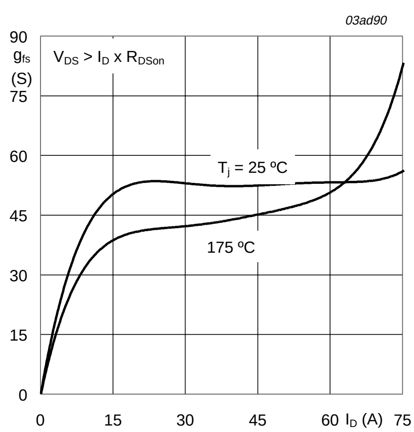
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



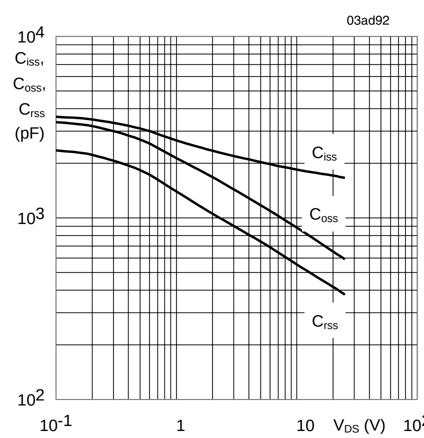
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



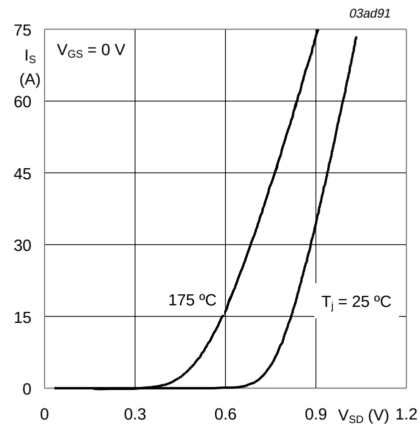
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 11. Forward transconductance as a function of drain current; typical values.



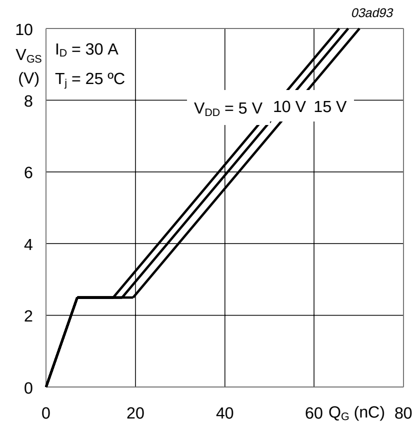
V_{GS} = 0 V; f = 1 MHz

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

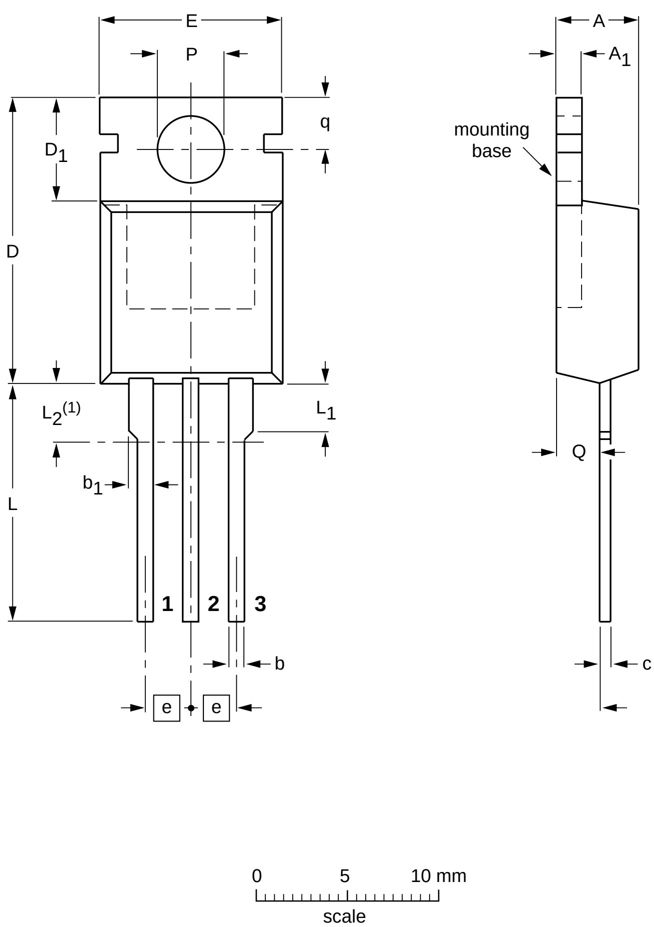


I_D = 30 A; V_{DD} = 5 V, 10 V and 15 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	$L_2^{(1)}$ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

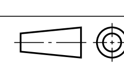
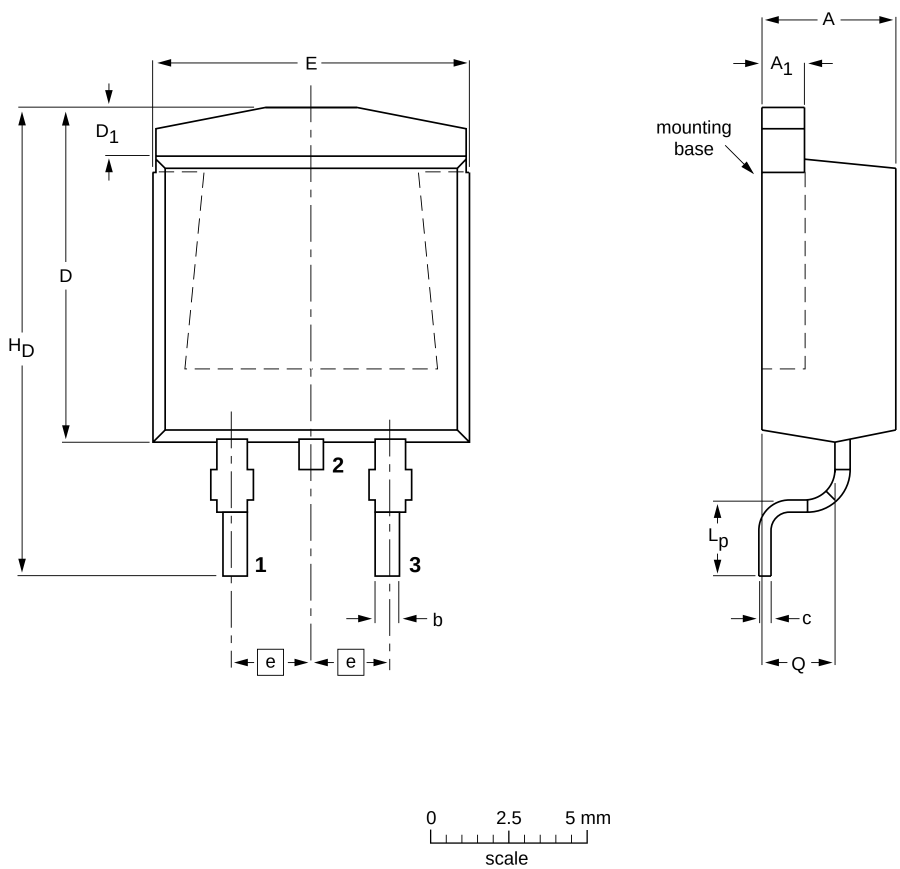
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			~~99-09-13~~ 00-09-07

Fig 15. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D^2-PAK); 3 leads (one lead cropped) **SOT404**



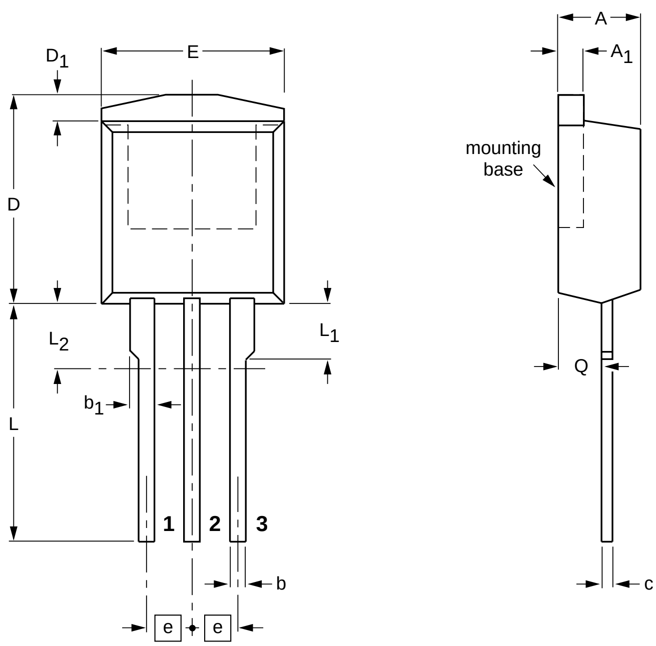
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.40 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						~~98-12-14~~ 99-06-25

Fig 16. SOT404 (D^2-PAK)

Plastic single-ended package; low-profile 3 lead TO-220AB **SOT226**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	L_2(1) max	Q
mm	4.5 4.1	1.40 1.27	0.9 0.7	1.3 1.0	0.7 0.4	9.65 8.65	1.5 1.1	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	2.6 2.2

Note

1. Terminals in this zone are not tinned.

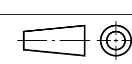
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT226		low-profile 3-lead TO-220AB				~~99-05-27~~ 99-09-13

Fig 17. SOT226 (I²-PAK)

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010123	-	Product specification; initial version

11. Data sheet status

Datasheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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(SCA71)

Contents

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