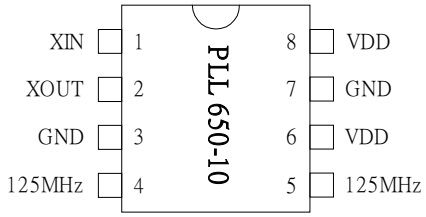
Network LAN Clock for Gigabit Ethernet

FEATURES

- Full CMOS output swing with 40-mA output drive capability. 25-mA output drive at TTL level.
- Advanced, low power, sub-micron CMOS processes.
- 25MHz fundamental crystal or clock input.
- Two outputs fixed at 125MHz..
- Zero PPM synthesis error in all clocks.
- Ideal for Network switches.
- 3.3V operation.
- Available in 8-Pin 150mil SOIC.

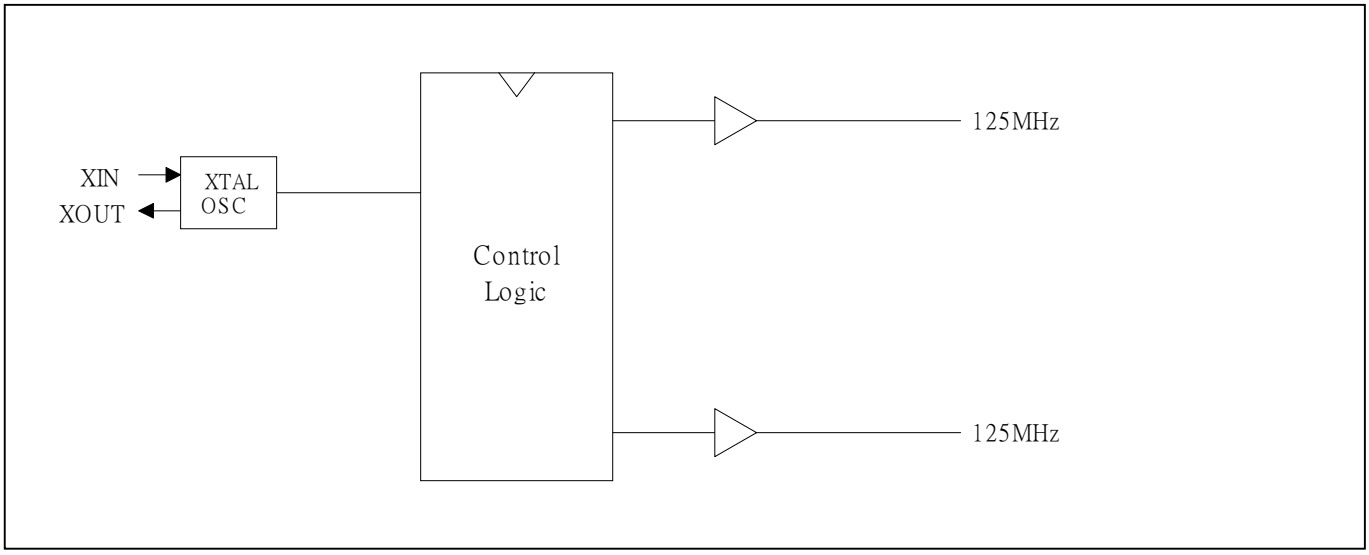
PIN CONFIGURATION



DESCRIPTIONS

The PLL 650-10 is a low cost, low jitter, and high performance clock synthesizer. With PhaseLink's proprietary analog Phase Locked Loop techniques, the chip accepts 25MHz crystal, and produces multiple output clocks for networking chips, and ASICs.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	1	I	25MHz fundamental crystal input (20pF C_L parallel resonant). C_L have been integrated into the chip. No external C_L capacitor is required.
XOUT	2	O	Crystal connection pin.
125MHz	4,5	O	125MHz outputs.
VDD	6,8	P	3.3V power supply
GND	3,7	P	Ground.

Electrical Specifications

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage Range	V_{CC}	-0.5	7	V
Input Voltage Range	V_I	-0.5	V_{CC}+0.5	V
Output Voltage Range	V_O	-0.5	V_{CC}+0.5	V
Soldering Temperature			260	°C
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature		0	70	°C

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

2. AC Specification

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Frequency		10	25	27	MHz
Output Rise Time	0.8V to 2.0V with no load			1.5	ns
Output Fall Time	2.0V to 0.8V with no load			1.5	ns
Duty Cycle	At VDD/2	45	50	55	%
Max. Absolute Jitter	Short term		±150		ps
Max. Jitter, cycle to cycle				80	ps

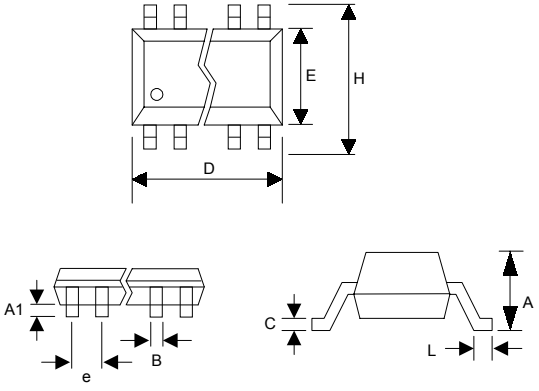
3. DC Specification

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage	VDD		3.13		3.47	V
Input High Voltage	V_{IH}			VDD/2		V
Input Low Voltage	V_{IL}			VDD/2	VDD/2 - 1	V
Input High Voltage	V_{IH}	For all normal input	2			V
Input Low Voltage	V_{IL}	For all normal input			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25mA			0.4	V
Output High Voltage At CMOS Level	V_{OH}	I_{OH} = -8mA	VDD-0.4			V
Operating Supply Current	I_{DD}	No Load		35		mA
Short-circuit Current	I_S			±100		mA
Nominal output current*	I_{out}	CMOS output level	35	40		mA
Nominal output current*	I_{out}	TTL output level	20	25		mA

PACKAGE INFORMATION

8 PIN Narrow SOIC (mm)

	SOIC	
Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
H	5.80	6.20
L	0.40	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL650-10 S C

PART NUMBER

TEMPERATURATURE
C=COMMERCIAL
M=MILITARY
I=INDUSTRAL

PACKAGE TYPE
S=SOIC