QFP-SD

Stacked Die Quad Flat Pack

- Stacking of die enables more functionality and integration in a conventional QFP package

FEATURES

- Combining devices into one package reduces PCB real estate and cost
- Increased sub-system performance by integrating multiple chips into a single package
- Die to die bonding capability for device/signal integration
- Standard and green/lead-free materials and Pb-free plating
- Options for mixed technologies, 2 or more stacked dice
- Fine pitch bonding capability
- Exposed pad provides enhanced thermal performance
- Low profile package thickness of 1.40mm (LQFP-SD and LQFP-ep-SD); 1.00mm (TQFP-ep-SD)
- Lead pitch ranges from 0.80mm to 0.40mm
- Pin count ranges from 32 to 208 leads (LQFP-SD), 64 to 216 leads (LQFP-ep-SD), 32 to 100 leads (TQFP-ep-SD)
- JEDEC standard compliant package outlines

DESCRIPTION

STATS ChipPAC's Stacked Die QFP offering includes LQFP-SD, LQFP-ep-SD and TQFP-ep-SD. LQFP-SD is a stacked die low profile QFP. LQFP-ep-SD is an exposed pad version that provides enhanced thermal performance. TQFP-ep-SD is a thin profile exposed pad version with enhanced thermal performance. STATS ChipPAC's chip stacking technology allows the integration of multiple ICs within a single package to improve package performance and functionality while reducing overall package size and cost. The die to die wire bonding capability enables device/signal integration to improve electrical performance and reduce overall package I/O requirements. STATS ChipPAC's Stacked Die QFPs with nominal package thickness of 1.40mm and 1.00mm are suitable for a variety of product applications. Stacked Die QFP packages are currently available in LQFP, LQFP-ep and TQFP-ep configurations, and are offered in standard and green/lead-free bill of materials.

APPLICATIONS

Suitable for a variety of applications including memory integration (ASIC or Logic), chipset integration (Analog/Digital), mixed technologies integration (Baseband/RF), handheld products (Cellular Phones, Pagers, MP3 Players, GPS), consumer electronics (Internet applications, Digital Cameras/Camcorders), computers (Network PCs), and PC peripherals (Disk Drivers, CD-R/RW, DVD Drivers).

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SPECIFICATIONS

Die Thickness	100-600µm (4-24mils)
Package Body Thickness	1.0, 1.4mm
Marking	Laser/ink
Packing Options	JEDEC tray/tape and reel

RELIABILITY

Moisture Sensitivity Level	JEDEC Level 3, 260°C reflow
Temperature Cycling	Condition C (-65°C to 150°C) 1000 cycles
High Temperature Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C/100% RH/2 atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs

ELECTRICAL PERFORMANCE

Package (mm)	Pad Size (mm)	Lead/Wire (mm)	Resistance (mOhm)	Inductance Self (nH)	Inductance Mutual (nH)	Capacitance Self (pF)	Capacitance Mutual (pF)
7 x 7 (32L)	138 x 138	1.4-2.2	11.0-18.0	0.64-0.99	0.31-0.49	0.21-0.33	0.07-0.12
		2	120	1.65	0.45-0.85	0.1	0.01-0.02
14 x 14 (128L)	275 x 275	3.0-4.5	24.0-36.0	1.96-2.92	1.08-1.61	0.69-1.03	0.31-0.45
		2	120	1.65	0.45-0.85	0.1	0.01-0.02

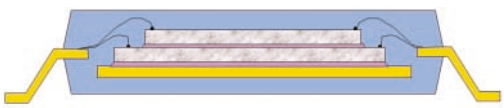
Note: Results are simulated values at 100MHz.

THERMAL PERFORMANCE

The thermal performance of each die in the stack is influenced by other die in the stack. Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and lead configuration. Simulation for specific applications should be performed.

CROSS-SECTION

LQFP-SD



LQFP-ep-SD

TQFP-ep-SD

PACKAGE CONFIGURATIONS

Package Size	Body Size (mm)	Lead Count
LQFP-SD	7 x 7 to 28 x 28	32 to 208
LQFP-ep-SD	10 x 10 to 24 x 24	64 to 216
TQFP-ep-SD	7 x 7 to 14 x 14	32 to 100

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