High Speed CMOS Bus Interface 20-Bit Buffer in QVSOP™

QS74FCT2X827T

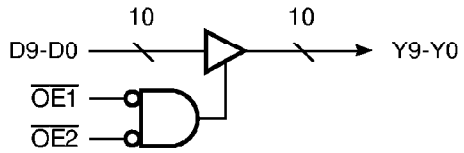
FEATURES/BENEFITS

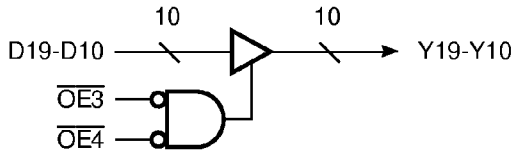
- Function compatible to the 74F827 74FCT827 and 74FCT827T
- CMOS power levels: <15 mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 48-pin 0.4 mm pitch QVSOP (Q1)
- A and C speed grades with 4.4 ns t_{PD} for C
- I_{OL} = 48 mA Com.

DESCRIPTION

The QS74FCT2X827T is a 20-bit buffer with three-state outputs that are ideal for driving high-capacitance loads as in memory address and data buses. Dual output enable controls are provided for each bank of ten outputs. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when Vcc is removed from the device.

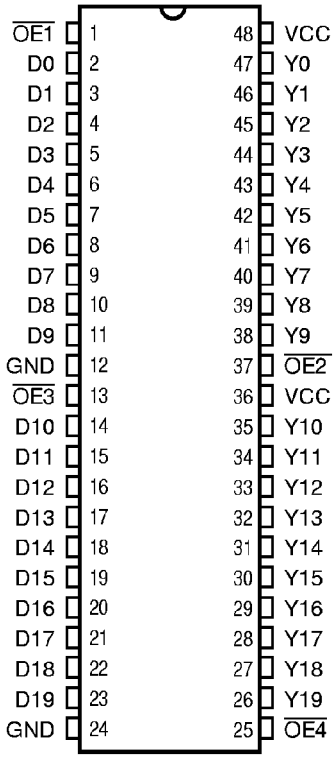
FUNCTIONAL BLOCK DIAGRAM





PIN CONFIGURATIONS (All Pins Top View)

QVSOP



PIN DESCRIPTION

Name	I/O	Description
D19-D0	I	Data Inputs
Y19-Y0	O	Data Outputs
$\overline{OE1}$, $\overline{OE2}$	I	Output Enables for 9-0
$\overline{OE3}$, $\overline{OE4}$	I	Output Enables for 19-10

FUNCTION TABLE

Inputs						Outputs		
$\overline{OE1}$	$\overline{OE2}$	$\overline{OE3}$	$\overline{OE4}$	D9-D0	D17-D10	Y9-Y0	Y19-Y10	Function
L	L	—	—	L	—	L	—	Enabled
L	L	—	—	H	—	H	—	Enabled
H	X	—	—	X	—	Hi-Z	—	High Impedance
X	H	—	—	X	—	Hi-Z	—	High Impedance
—	—	L	L	—	L	—	L	Enabled
—	—	L	L	—	H	—	H	Enabled
—	—	H	X	—	X	—	Hi-Z	High Impedance
—	—	X	H	—	X	—	Hi-Z	High Impedance