SEMTECH

Description

SC2453 is a high performance multi-output converter controller that can be configured for a variety of applications. The SC2453 utilizes synchronous rectified buck topologies where efficiency is most important. It also provides dedicated programmable positive and negative linear regulators using external transistors in conjunction with coupled windings to generate positive and negative voltages. Power up sequencing prevents converter latch-ups.

The two buck converters are out of phase, reducing input ripple, allowing for fewer input capacitors. All converters are synchronized to prevent beat frequencies. High frequency operation will reduce ripple and minimize noise. It also reduces the size of output inductors and capacitors. Other features include soft start, power-good signaling, bootstrapping for high side MOSFETs, and frequency synchronization.

Features

◆ Two synchronized converters for low noise
◆ Power up sequencing to prevent latch-ups
◆ Out of phase operation for low input ripple
◆ Over current protection
◆ Wide input range, 4.5 to 30V
◆ Programmable frequency up to 700KHz
◆ Two synchronous bucks for high efficiency at high current
◆ One dedicated programmable positive linear regulator and one dedicated programmable negative linear regulator
◆ –40 to 105 degree C operating temperature
◆ Output voltage as low as 0.5V
◆ Small package TSSOP-28

Applications

◆ DSL applications with multiple input voltage requirements
◆ Mixed-Signal applications requiring positive and negative voltages
◆ Cable modem power management
◆ Base station power management

Typical Application Circuit
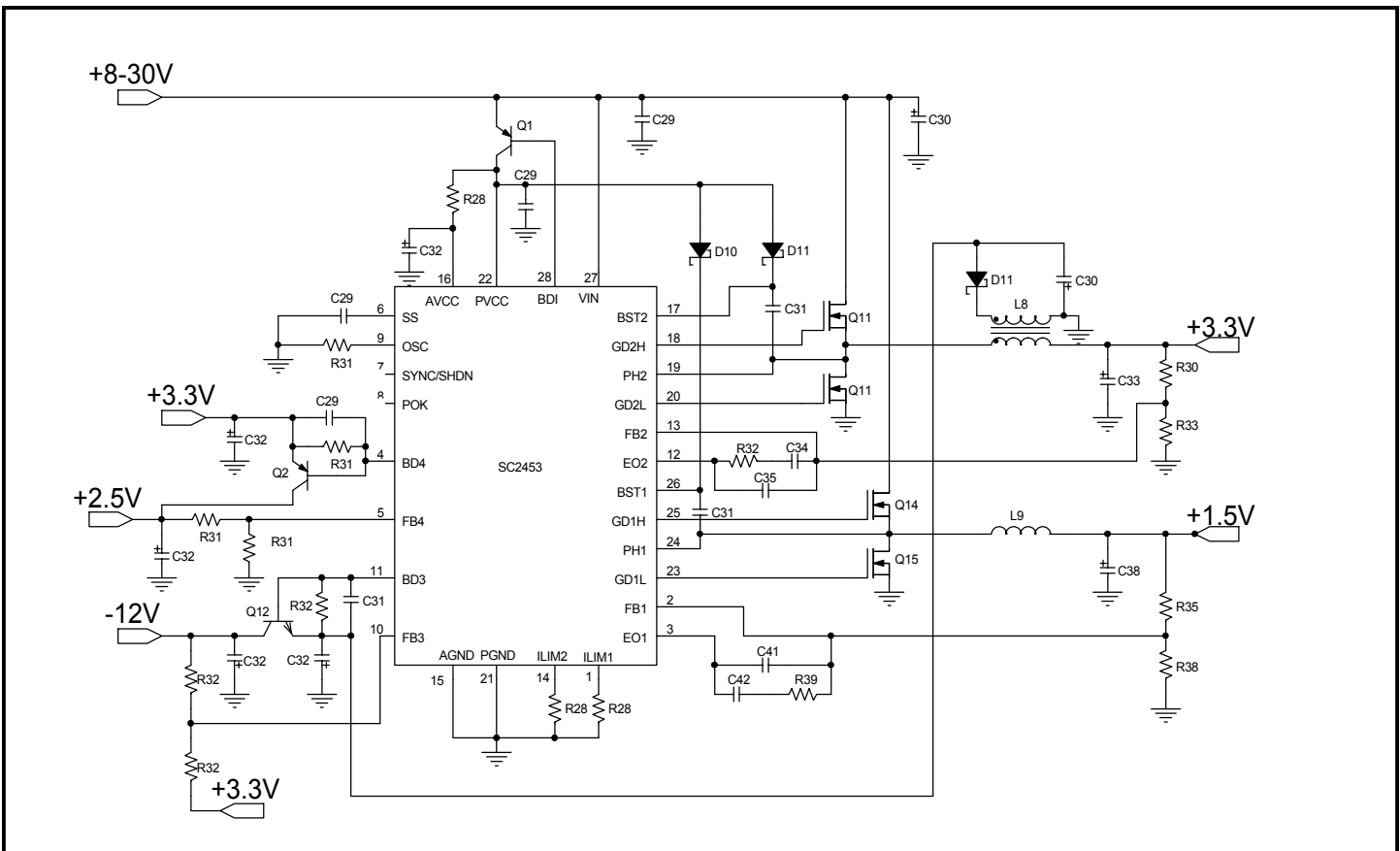
Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Maximum	Units
BST1, BST2 to PGND	35	V
VIN to PGND	30	V
PVCC, AVCC to PGND	7	V
PGND to AGND	±0.3	V
PH1 to BST1, PH2 to BST2	-6 to 0.3	V
GD1H to PH1, GD2H to PH2	7	V
GD1L, GD2L to PGND	7	V
ILIM1, ILIM2 to AGND	7	V
OSC, SYNC, POK, SS to AGND	7	V
BDI, BD3, BD4 to PGND	7	V
FB1, FB2, FB3, FB4, EO1, EO2 to AGND	7	V
GD1H, GD1L, GD2H, DG2L Source or Sink Current	1	A
Storage Temperature Range	-60 to +150	°C
Junction Temperature	-40 to +125	°C
Lead Temperature (Soldering) 10 Sec.	260	°C

Electrical Characteristics

Unless specified: T_A = 25°C, V_{CC} = 12V, fs = 600KHz, SYNC/SHDN = 5V

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Quiescent Current	SS/SHDN = 0V				µA
Operating Current	No load		7	12	mA
AVCC	VIN > 5.5V	4.5	5	5.5	V
PVCC	VIN > 5.5V	4.5	5	5.5	V
Undervoltage Lockout					
Start Threshold		4.312	4.4	4.488	V
UVLO Hysteresis			0.1		V
PWM Comparator					
Delay to Output			70		nS

SEMTECH

Electrical Characteristics (Cont.)

Parameter	Test Conditions	Min	Typ	Max	Unit
Positive Linear Regulator					
Feedback Voltage		0.49	0.5	0.51	V
Feedback Input Leakage Current					µA
Amplifier Transconductance	V_{FB4} = 0.5V, I_{B04} = 0.5 to 5mA (sink)		-2		mV
Drive Sink Current			5		mA
Negative Linear Regulator					
Feedback Voltage		-25	0	25	mV
Feedback Input Leakage Current					µA
Amplifier Trandconductance	V_{FB3} = 0V, I_{FB3} = 0.5 to 5mA (source)		-1.5		mV
Driver Source Current			5		mA
Error Amplifier					
Feedback Voltage		0.49	0.5	0.51	V
Input Bias Current				200	nA
Input Offset Voltage				5	mV
Open Loop Gain		90			dB
Unity Gain Bandwidth			3		MHz
Output Sink Current			2		mA
Output Source Current			2		mA
Slew Rate			1		V/µS
Oscillator					
Frequency Range		100		700	KHz
Frequency	R_T = TBD	540	600	660	KHz
CT Peak Voltage			3.0		V
CT Valley Voltage			0.1		V
SYNC Input High Pulse Width		100			nS
SYNC Rise/Fall Time				50	nS
SYNC Frequency Range		FOSC		FOSC ±10%	kHz
SYNC High/Low Threshold			1.5		V

POWER MANAGEMENT   **PRELIMINARY**

Electrical Characteristics (Cont.)

Unless specified: T_A = 25°C, V_{CC} = 12V, fs = 600KHz

Parameter	Test Conditions	Min	Typ	Min	Units
Duty Cycle					
PWM 1 & 2 Maximum Duty Cycle	fs = 100kHz		96		%
PWM 1 & 2 Maximum Duty Cycle	fs = 700kHz		77		%
PWM 1 & 2 Minimum Duty Cycle			5		%
Current Limit					
CH1& 2 ILIM Set Voltage			2		V
Soft Start/Shut Down					
Charge Current			5		µA
Discharge Current			2		mA
Disable Threshold Voltage			0.5		V
Disable Low to Shut Down			50		µs
Output					
Gate Drive On-Resistance(H)			2		Ω
Gate Drive On-Resistance(L)			2		Ω
Rise Time	C_{OUT} = 1000pF		20		nS
Fall Time	C_{OUT} = 1000pF		20		nS
Power Good					
FB1 & FB2 High Trip Level			0.55		V
Hysteresis			1		%
FB1 & FB2 Low Trip Level			0.45		V
Hysteresis			1		%
PWR OK Output Low Level					V
PWR OK Output High Leakage					µA

POWER MANAGEMENT

Pin Configuration

Top View

ILIM1	1	28	BDI
FB1	2	27	VIN
EO1	3	26	BST1
BD4	4	25	GD1H
FB4	5	24	PH1
SS/SHDN	6	23	GD1L
SYNC	7	22	PVCC
POK	8	21	PGND
OSC	9	20	GD2L
FB3	10	19	PH2
BD3	11	18	GD2H
EO2	12	17	BST2
FB2	13	16	AVCC
ILIM2	14	15	AGND

(28 Pin TSSOP)
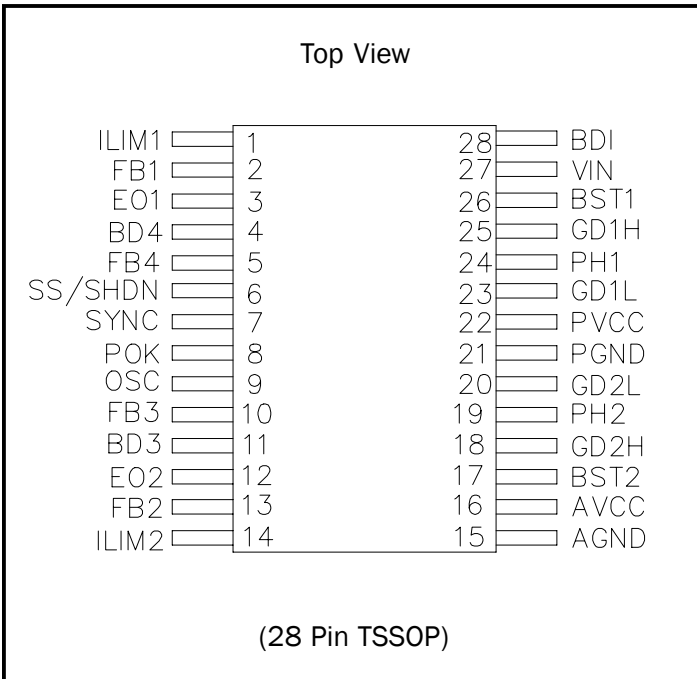
Ordering Information

Part Number	Package	Temp. Range (T$_J$)
SC2453ITSTR	TSSOP-28	-40°C to +85°C

Note:
Only available in tape and reel packaging. A reel contains 2500 devices.

Marking Information

TOP

SC2453ITS
yyww
xxxxxx

nnnn = Part Number (Example: 1406)
yyww = Date Code (Example: 0012)
xxxxx = Semtech Lot No. (Example: P94A01)
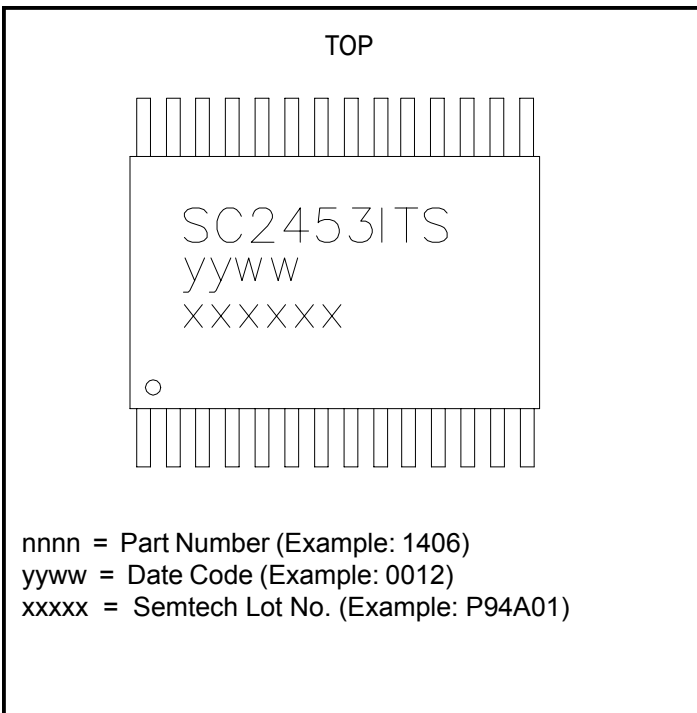
Pin Descriptions

Pin #	Pin Name	Pin Function
1	ILIM1	Current limit threshold set for the OUTPUT1. An external resistor adjusts the limit.
2	FB1	Feedback input for OUTPUT1.
3	EO1	Error amplifier output for compensation of OUTPUT1.
4	BD4	Positive linear regulator base driver.
5	FB4	Feedback input for OUTPUT4.
6	SS/SHDN	Soft start pin. Hold low to shutdown part.
7	SYNC	Oscillator synchronization pin.
8	POK	Open drain power good output.
9	OSC	Connect a resistor to AGND for programming the oscillator frequency.
10	FB3	Feedback input for OUTPUT3.
11	BD3	Negative linear regulator base driver.
12	EO2	Error amplifier output for compensation of OUTPUT2.
13	FB2	Feedback input for OUTPUT2.
14	ILIM2	Current limit threshold set for OUTPUT2. An external resistor adjusts the limit.
15	AGND	Analog signal ground.
16	AVCC	Supply voltage for analog circuitry.
17	BST2	Boost capacitor connection for the OUTPUT2 high side gate drive. Connect an external capacitor and a diode as shown in the Typical Application Circuit.
18	GD2H	Gate drive output for OUTPUT2. It is 180 degrees out of phase with GD1H.
19	PH2	Switching node for OUTPUT2 external inductor connection.
20	GD2L	Gate drive output for OUTPUT2, low side N-Channel MOSFET.
21	PGND	Power ground.
22	PVCC	Supply voltage for output drivers.
23	GD1L	Gate drive output for OUTPUT1, low side N-Channel MOSFET.
24	PH1	Switching node for OUTPUT1 external inductor connection.
25	GD1H	Gate drive output for OUTPUT1, high side N-Channel MOSFET.
26	BST1	Boost capacitor connection for the OUTPUT1 high side gate drive. Connect an external capacitor and a diode as shown in the Typical Application Circuit.
27	VIN	Input supply voltage.
28	BDI	Base drive for AVCC/PVCC regulator.

Block Diagram
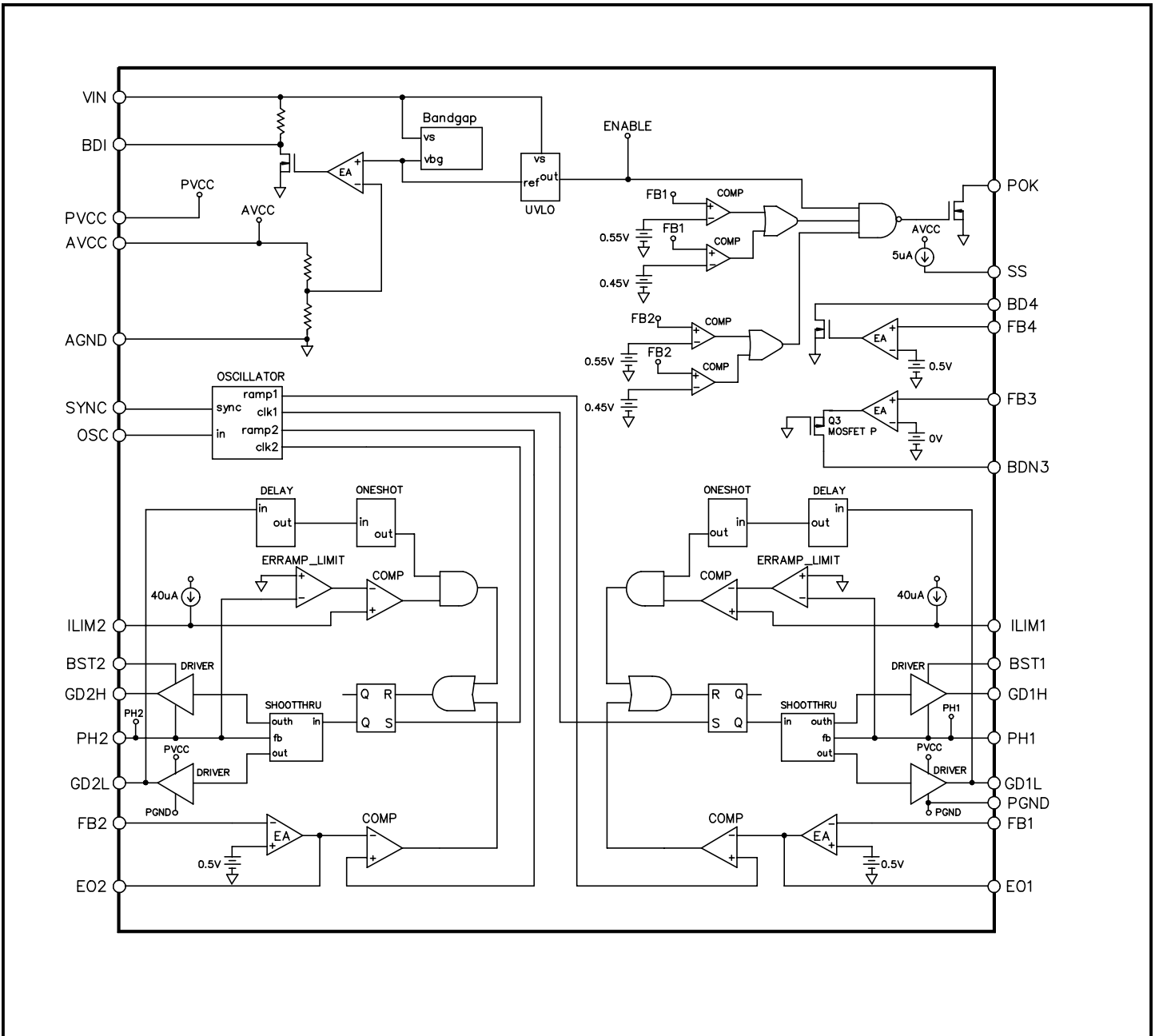
Applications Information

The SC2453 is designed to control and drive two N-Channel MOSFET synchronous rectified buck and two LDOs, one positive and the other negative. The two bucks are synchronized and out of phase operation for low input ripple and noise. The switching frequency is programmable to optimize design. The SC2453 switching regulator section features lossless current sensing while it provides a programmable cycle by cycle over current limit. The SC2453 linear sections are low dropout regulators. The voltage for the linear controllers LDO1 and LDO2 are programmable.

SUPPLIES

Supplies VIN, PVCC and AVCC from the input source are used to power the SC2353. An external PNP transistor as a linear regulator supplies AVCC and PVCC. The VIN supply provides the bias for the Internal Reference and UVLO circuitry. The AVCC supply provides the bias for the oscillator, the switchers, the LDO controllers, and the Power Good circuitry. PVCC is used to drive the low side MOSFET gate.

START UP SEQUENCE

A 5uA current source pulls up on the SS pin. When the SS pin reaches 0.5V, the first converter will start. The reference input of the error amplifier is ramped up with the soft-start signal. When the SS pin reaches 2V the SS pin is pulled down to approximately 0.7V and the second converter will begin to soft-start in an identical fashion to the first converter. When the SS pin reaches 2V for the second time, the SS pin is pulled to approximately 0.7V again and the LDOs are started. The reference of the positive LDO is ramped with the SS pin while the negative LDO should be soft-started externally by ramping the positive supply of the feedback resistors. The SS pin will then be pulled up to supply, i.e. AVCC. The SS time is controlled by the value of the SS cap. If the SS pin is pulled below 0.5V, the SC2453 is disabled.

The power-okay circuitry monitors the FB inputs of the converter error amplifiers. If the voltage on these inputs goes above 0.55V or below 0.45V then the POK pin is pulled low. The power-okay circuitry monitors the FB inputs of the converter error amplifiers. If the voltage on these inputs goes above 0.55V or below 0.45V then the POK pin is pulled low. The POK pin is held low until the end of the start-up sequence.

OSCILLATOR

The switching frequency of the SC2453 is set by an external resistor using the following formula:

$$R_{freq} = \frac{1}{10p \bullet 8.4 \bullet fs}$$

OVER CURRENT

SC2453 monitors any voltage drop in the lower MOSFETs Rdson voltage due to an over current condition. This method of current sensing minimizes any unnecessary losses due to external sense resistance.

The SC2453 utilizes an internal current source and an external resistor connected from the ILIM pins to the AGND pin to program a current limit level. This limit is programmable by choosing the resistor relative to the level required. The value of the resistor can be selected by the following formula:

$$Rilim = 2000/(Ilim * Rdson)$$

An internal comparator with a reference from the level set by the external resistor monitors the voltage drop across the lower MOSFET. Once the Vdson of the MOSFET exceeds this level, the low side gate is turned on and the upper MOSFET is turned off.

GATE DRIVERS

The low side gate driver is supplied from PVCC and provides a peak source/sink current of 1A. The high side gate drive is also capable of sourcing and sinking peak currents of 1A. The high side MOSFET gate drive can be provided by an external 12V supply that is connected from BST to GND. The actual gate to source voltage of the upper MOSFET will approximately equal 7V (12V-VCC). If the external 12V supply is not available, a classical bootstrap technique can be implemented from the PVCC supply. A bootstrap capacitor is connected from BST to Phase while PVCC is connected through a diode (Schottky or other fast low VF diode) to the BST. This will provide a gate to source voltage approximately equal to the VCC-Vdiode drop.

Shoot through control circuitry provides a 30ns dead time to ensure both the upper and lower MOSFET will not turn on simultaneously and cause a shoot through condition.

Applications Information (Cont.)

PWM CONTROLLER

SC2453 is a voltage mode buck controller that utilizes an externally compensated high bandwidth error amplifier to regulate output voltage. The power stage of the synchronous rectified buck converter control-to-output transfer function is as shown below:

$$G_{VD}(s) = V_{IN}\frac{1+sR_CC}{1+s\dfrac{L}{R}+s^2LC}$$

where,

$$\omega_O = \frac{1}{\sqrt{LC}}$$

L – Output inductance
C – Output capacitance
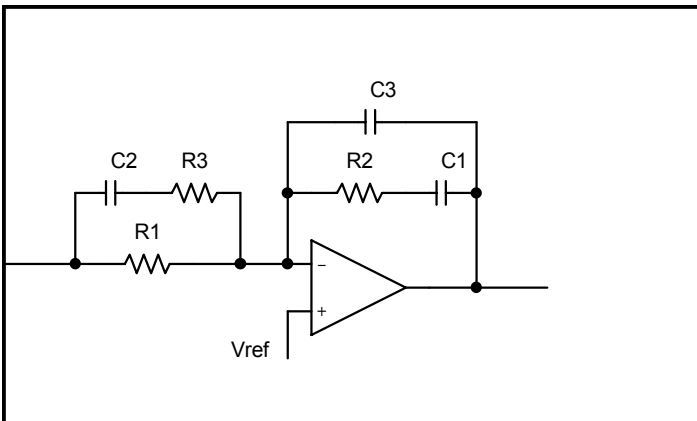R_C – Output capacitor ESR
V_{IN} – Input voltage

Figure 1. Voltage Mode Buck Converter Compensation Network

The transfer function of the compensation network is as follows:

$$G_{COMP}(s) = \frac{\omega_I}{s}\cdot\frac{(1+\dfrac{s}{\omega_{Z1}})(1+\dfrac{s}{\omega_{Z2}})}{(1+\dfrac{s}{\omega_{P1}})(1+\dfrac{s}{\omega_{P2}})}$$

where,

$$\omega_{Z1} = \frac{1}{R_2C_1}, \omega_{Z2} = \frac{1}{(R_1+R_3)C_2}$$

$$\omega_I = \frac{1}{R_1(C_1+C_3)}, \omega_{P1} = \frac{1}{R_3C_2}, \omega_{P2} = \frac{1}{R_2\dfrac{C_1C_3}{C_1+C_3}}$$

The design guidelines are as following:

1. Set the loop gain crossover frequency ω_c for given switching frequency.
2. Place an integrator in the origin to increase DC and low frequency gains.
3. Select ω_{Z1} and ω_{Z2} such that they are placed near ω_0 to dampen peaking; the loop gain has –20dB rate to go across the 0dB line for obtaining a wide bandwidth.
4. Cancel ω_{ESR} with compensation pole ω_{P1} ($\omega_{P1} = \omega_{ESR}$).
5. Place a high frequency compensation pole ω_{P2} at the half switching frequency to get the maximum attenuation of the switching ripple and the high frequency noise with the adequate phase lag at ω_c.
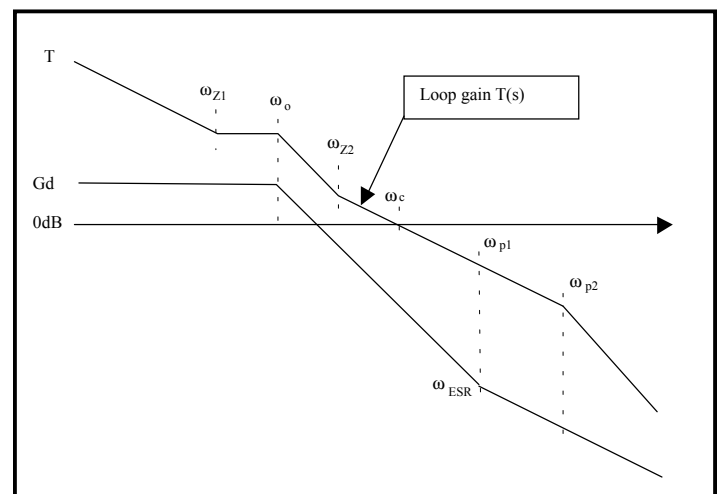

Figure 2. Asymptotic diagram of buck power stage and its compensated loop gain.

Applications Information (Cont.)

DUAL LDO CONTROLLERS

The SC2453 provides positive and negative adjustable linear regulator controllers. The positive linear regulator uses a PNP transistor to regulate output voltage. This is set by a voltage divider connected from the output to FB to AGND. Referring to the front page Application Circuit, select R8 in the 5KΩ to 20KΩ range. Calculate R7 with the following equation:

$$R_7 = R_8 \left(\frac{V_{OUT}}{0.5} - 1 \right)$$

The negative linear regulator uses a NPN transistor to regulate output voltage. This is set by a voltage divider connected from the output to FB to a positive reference. Referring to the front page Application Circuit, select R16 in the 5KΩ to 20KΩ range. Calculate R12 with the following equation:

$$R_{12} = R_{16} \left(\frac{V_{OUT}}{V_{REF}} \right)$$

where V_{REF} is the positive voltage reference.

LAYOUT GUIDELINES

Careful attention to layout requirements are necessary for successful implementation of the SC2453 PWM controller. High switching current is present in the application and their effect on ground plane voltage differentials must be understood and minimized.

1). The high power parts of the circuit should be laid out first. A ground plane should be used. The number and position of ground plane interruptions should be such as to not unnecessarily compromise ground plane integrity. Isolated or semi-isolated areas of the ground plane may be deliberately introduced to constrain ground currents to particular areas, such as the input capacitor or the bottom FET ground.

2). The loop formed by the Input Capacitor(s) (Cin), the Top FET (Q_T) and the Bottom FET (Q_B) must be kept as small as possible. This loop contains all the high current, fast transition switching. Connections should be as wide and as short as possible to minimize loop inductance. Minimizing this loop area will a) reduce EMI, b) lower ground injection currents, resulting in electrically "cleaner" grounds for the rest of the system and c) minimize source ringing, resulting in more reliable gate switching signals.

3). The connection between the junction of Q_T, Q_B and the output inductor should be a wide trace or copper region. It should be as short as practical. Since this connection has fast voltage transitions, keeping this connection short will minimize EMI. Also keep the Phase connection to the IC short. The top FET gate charge currents flow in this trace.

4) The Output Capacitor(s) (Cout) should be located as close to the load as possible. Fast transient load currents are supplied by Cout only and connections between Cout and the load must be short, wide copper areas to minimize inductance and resistance.

5) The SC2453 is best placed over a quiet ground plane area. Avoid pulse currents in the Cin, Q_T, Q_B loop flowing in this area. GND should be returned to the ground plane close to the package and close to the ground side of (one of) the output capacitor(s). If this is not possible, the GND pin may be connected to the ground path between the Output Capacitor(s) and the Cin, Q1, Q2 loop. Under no circumstances should GND be returned to a ground inside the Cin, Q1, Q2 loop.

6) A separate analog ground plane connects to the SC2453 AGND pin. All analog grounding paths including decoupling capacitors, feedback resistors, compensation components, and current-limit setting resistors should be connected to this plane.

7) Ideally, the grounds for the two LDO sections should be returned to the ground side of (one of) the output capacitor(s).
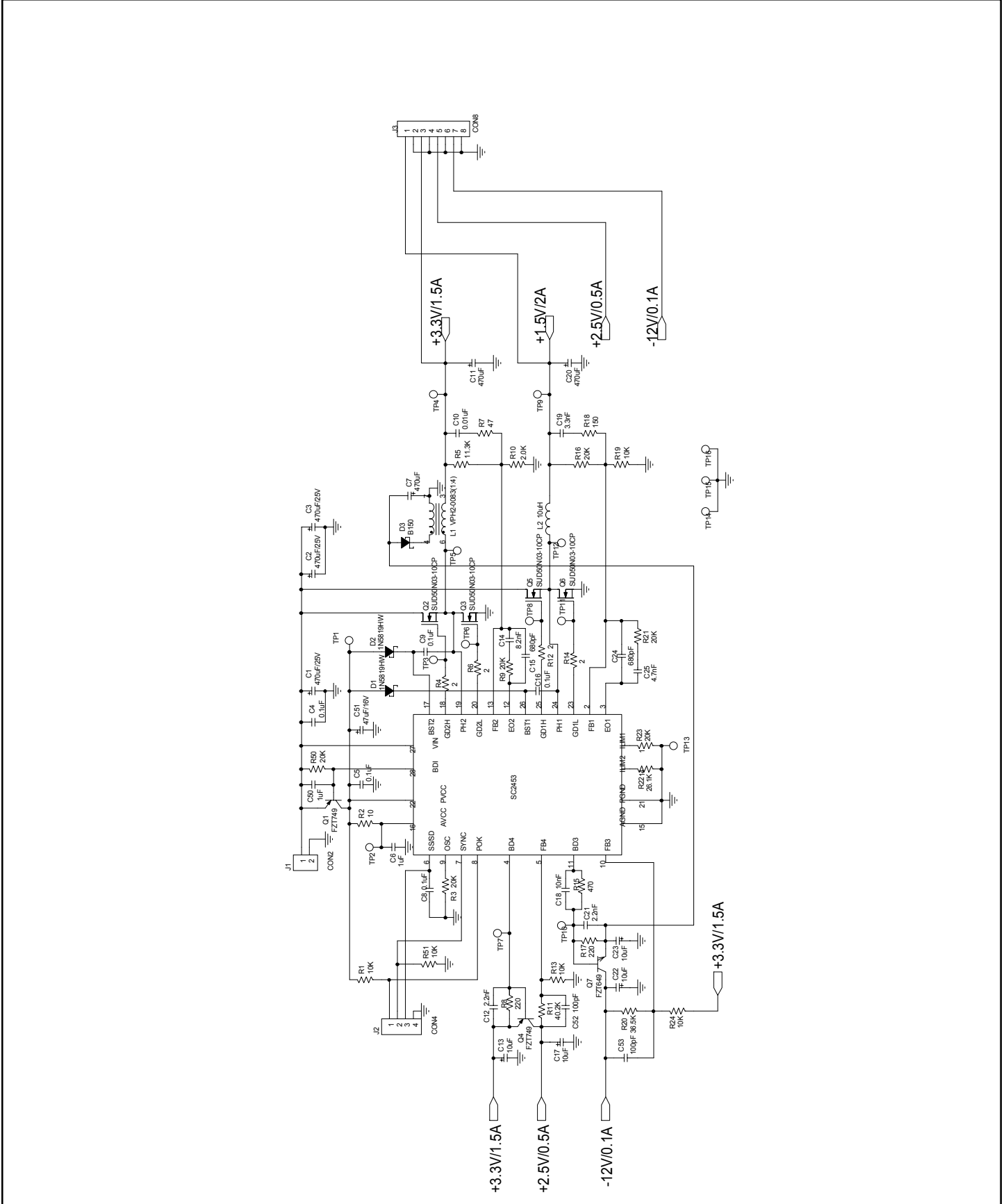
Bill of Materials - Evaluation Board

Item	Qty.	Reference	Value	Description/Part No.	Foot Print
1	3	C1,C2,C3	470uF/16V	Rubycon P/N: 16ZA470	CPCYL/D.400/LS.200/.034
2	4	C4,C5,C9,C16	0.1uF		1206
3	2	C6,C50	1uF		12.6
4	3	C7,C11,C20	470uF/16V	Panasonic P/N: ECA-1CHG471	CAP_RADIAL_V8X11P
5	1	C8	0.1uF		1206
6	1	C10	0.01uF		1206
7	2	C12,C21	2.2nF		1206
8	4	C13,C17,C22,C23	68uF/16V	Panasonic P/N: EEU-FC1C680	CPCYL/D.200/LS.100/.031
9	1	C14	8.2nF		1206
10	2	C15,C24	680pF		1206
11	1	C18	10nF		1206
12	1	C19	3.3nF		1206
13	1	C25	4.7nF		1206
14	1	C51	47uF/4V	Sanyo P/N: 4TPB330ML	7343
15	2	C52,C53	100pF		1206
16	2	D1,D2	1N5819HW	Diodes Inc. P/N: 1N5819HW-7	SOD-123
17	1	D3	B150	Diodes Inc. P/N: B150-13	SM/SMA
18	1	L1	VPH2-0083 (1:4)	Coiltronics P/N: VPH2-0083	VP2
19	1	L2	15uH	Coilcraft P/N: DO5022P-153	DO3316
20	2	Q1,Q2	FZT749	Zetex Inc. P/N: FZT749TA	SOT-223
21	4	Q2,Q3,Q5,Q7	SUD50N03-10CP	Vishay P/N: SUD50N03-10CP	SOT-223
22	1	Q7	FZT649	Zetex Inc. P/N: FZT649TA	SOT-223
23	5	R1,R13,R19,R24, R51	10K		1206
24	1	R2	10		1206
25	6	R3,R9,R16,R21,R23-R50	20K		1206
26	4	R4,R6,R12,R14	2		1206
27	1	R5	11.3K		1206
28	1	R7	47		1206
29	2	R8,R17	220		1206
30	1	R10	2.0K		1206
31	1	R11	40.2K		1206
32	1	R15	470		1206

Bill of Materials - Evaluation Board

Item	Qty.	Reference	Value	Description/Part No.	Foot Print
33	1	R18	150		1206
34	1	R20	36.5K		1206
35	1	R22	26.1K		1206
36	1	U1	SC2453	Semtech Corp. P/N: SC2453ITSTR	TSSOP-28

SC2453

POWER MANAGEMENT   PRELIMINARY

Outline Drawing - TSSOP-28

DIMENSIONS ①					
DIMᴺ	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	②
B	.169	.177	4.30	4.50	②
C	.252 BSC		6.40 BSC		–
D	.026 BSC		.65 BSC		–
E	.007	.012	.19	.30	–
F	.0020	.0060	.05	.15	–
G		.047		1.20	–
J	.0035	.0079	.09	.20	–
K	0°	8°	0°	8°	–
L	.018	.030	.45	.75	–

JEDEC MO−153AE

② DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.
① CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28

DIMENSIONS ①					
DIMᴺ	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.218	–	5.53	REF
D	–	.333	–	8.45	REF
E	–	.026	–	0.65	BSC
G	.155	–	3.947	–	–
X	–	.013	–	0.323	–
Y	–	.062	–	1.583	REF
Z	–	.280	–	7.113	–

② GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

① CONTROLLING DIMENSIONS: MILLIMETERS.

Contact Information

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