Si5322

PRELIMINARY DATA SHEET

PIN-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Description

The Si5322 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5322 accepts dual clock inputs ranging from 19.44 to 707 MHz and generates two equal frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. The Si5322 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5322 is ideal for providing clock multiplication in high performance timing applications.

Applications

- SONET/SDH OC-48/OC-192 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 line cards
- Optical modules
- Test and measurement

Features

- Selectable output frequencies ranging from 19.44 to 1050 MHz
- Low jitter clock outputs with jitter generation as low as 0.6 ps_{RMS} (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (30 kHz to 1.3 MHz)
- Dual clock inputs with manual or automatically controlled hitless switching
- Dual clock outputs with selectable signal format: LVPECL, LVDS, CML, CMOS
- Support for ITU G.709 FEC ratios (255/238, 255/237, 255/236)
- LOS alarm output
- Pin-controlled output phase adjust
- Pin-programmable settings
- On-chip voltage regulator for 1.8, 2.5, or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, RoHS compliant

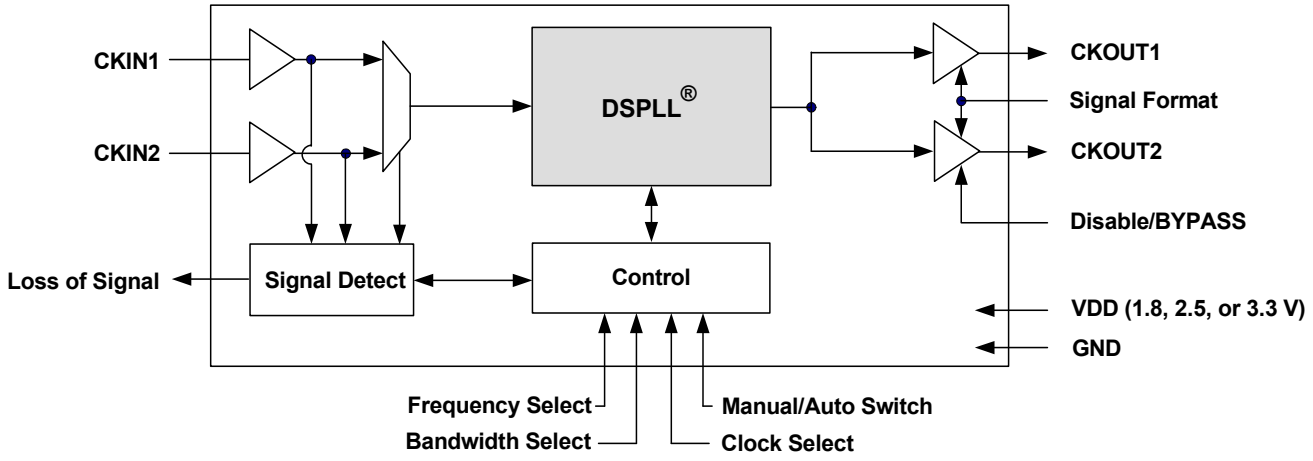


Table 1. Performance Specifications

(V_{DD} = 1.8, 2.5, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.62	1.8	1.98	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz Both CKOUTs enabled LVPECL format output	—	251	279	mA
		CKOUT2 disabled	—	217	243	mA
		f_{OUT} = 19.44 MHz Both CKOUTs enabled CMOS format output	—	204	234	mA
		CKOUT2 disabled	—	194	220	mA
		Tristate/Sleep Mode	—	TBD	TBD	mA
Input Clock Frequency (CKIN1, CKIN2)	CK_F	Input frequency and clock multiplication ratio pin-selectable from table of values using FRQSEL and FRQTBL settings. Consult Silicon Laboratories configuration software DSPLL*sim* or Any-Rate Precision Clock Family Reference Manual at www.silabs.com/clock for table selections.	19.44	—	707.35	MHz
Output Clock Frequency (CKOUT1, CKOUT2)	CK_{OF}		19.44	—	1049.76	MHz
Input Clocks (CKIN1, CKIN2)						
Differential Voltage Swing	CKN_{DPP}		0.25	—	1.9	V_{PP}
Common Mode Voltage	CKN_{VCM}	1.8 V ±10%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Rise/Fall Time	CKN_{TRF}	20–80%	—	—	11	ns
Duty Cycle	CKN_{DC}	Whichever is less	40	—	60	%
			50	—	—	ns
Output Clocks (CKOUT1, CKOUT2)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 1. Performance Specifications (Continued)
(V_{DD} = 1.8, 2.5, or 3.3 V ±10%, T_A = –40 to 85 ºC)

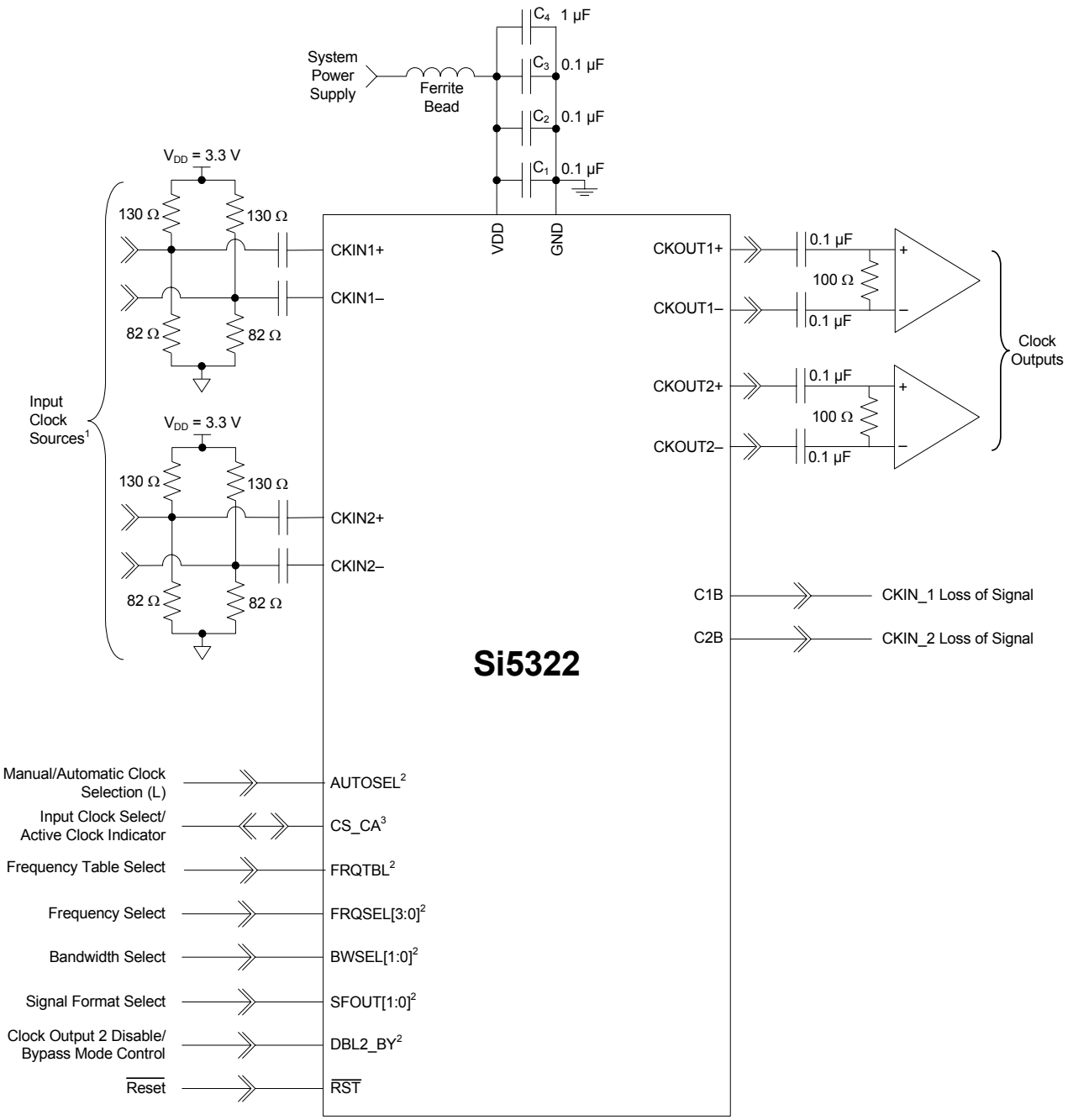
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps
Duty Cycle	CKO_{DC}		45	—	55	%
PLL Performance						
Jitter Generation	J_{GEN}	fo = 622.08 MHz, LVPECL output format 50 kHz – 80 MHz	—	0.6	TBD	ps rms
		12 kHz – 20 MHz	—	0.6	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
Phase Noise	CKO_{PN}	f_{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	38	—	ºC/W

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.6	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	ºC
Storage Temperature Range	T_{STG}	–55 to 150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ)		2	kV
ESD MM Tolerance		200	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.



Notes: 1. Assumes differential LVEPECL termination (3.3 V) on clock inputs.
2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).
3. Assumes manual input clock selection.

Figure 1. Si5322 Typical Application Circuit

1. Functional Description

The Si5322 is a low jitter, precision clock multiplier for high-speed communication systems, including SONET OC-48/OC-192, Ethernet, and Fibre Channel. The Si5322 accepts dual clock inputs ranging from 19.44 to 707 MHz and generates two frequency-multiplied clock outputs ranging from 19.44 to 1050 MHz. The two input clocks are at the same frequency and the two output clocks are at the same frequency. The input clock frequency and clock multiplication ratio are selectable from a table of popular SONET, Ethernet, and Fibre Channel rates. In addition to providing clock multiplication in SONET and datacom applications, the Si5322 supports SONET-to-datacom frequency translations. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to look up valid Si5322 frequency translations. This utility can be downloaded from www.silabs.com/timing. This information is also available in the Any-Rate Precision Clock Family Reference Manual, also available from www.silabs.com/timing.

The Si5322 is recommended for applications in which the input clock is relatively low jitter and only clock multiplication is required. The Si5322 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5322 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 30 kHz to 1.5 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio. The Si5322 monitors all input clocks for loss of signal and provides a LOS alarm when it detects a missing clock.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

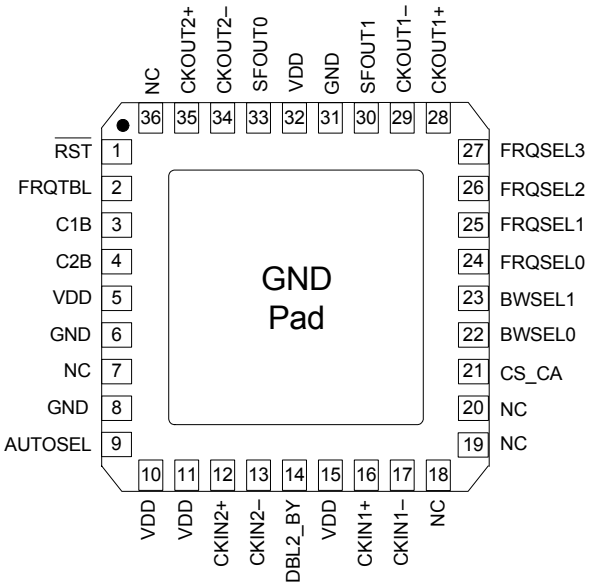
The Si5322 has two differential clock outputs. The electrical format of the clock outputs is programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. The phase difference between the selected input clock and the output clocks is adjustable in 200 ps increments for system skew control. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

1.1. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for more detailed information about the Si5322. The FRM can be downloaded from www.silabs.com/timing.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. This utility can be downloaded from www.silabs.com/timing.

2. Pin Descriptions: Si5322



Pin assignments are preliminary and subject to change.

Table 3. Si5322 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5322 will perform an internal self-calibration. This pin has a weak pull-up.
2	FRQTBL	I	3-Level	**Frequency Table Select.** Selects SONET/SDH, datacom, or SONET/SDH to datacom frequency table. L = SONET/SDH. M = Datacom. H = SONET/SDH to Datacom. This pin has a weak pull-down.
3	C1B	O	LVCMOS	**CKIN1 Loss of Signal.** Active high loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present. 1 = LOS on CKIN1.
4	C2B	O	LVCMOS	**CKIN2 Loss of Signal.** Active high loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present. 1 = LOS on CKIN2.

Table 3. Si5322 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
5, 10, 11, 15, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should be placed as close to device as is practical.
6, 8, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
9	AUTOSEL	I	3-Level	**Manual/Automatic Clock Selection.** Three level input that selects the method of input clock selection to be used. L = Manual. M = Automatic non-revertive. H = Automatic revertive.
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.
14	DBL2_BY	I	3-Level	**Output 2 Disable/Bypass Mode Control.** Controls enable of CKOUT2 divider/output buffer path and PLL bypass mode. L = CKOUT2 enabled. M = CKOUT2 disabled. H = Bypass mode with CKOUT2 enabled.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency selected from a table of values. The same frequency must be applied to CKIN1 and CKIN2.

Table 3. Si5322 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>21</td><td>CS_CA</td><td>I/O</td><td>LVCMOS</td><td>Input Clock Select/Active Clock Indicator.
If manual clock selection mode is chosen (AUTOSEL = L), this pin functions as the manual input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CS input state.
0 = Select CKIN1.
1 = Select CKIN2.
If automatic clock selection mode is chosen (AUTOSEL = M or H), this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both CKIN1 and CKIN2, indicating that the digital hold state has been entered, CA will indicate the last active clock that was used before entering the hold state.
0 = CKIN1 active input clock.
1 = CKIN2 active input clock.</td></tr>
<tr><td>23
22</td><td>BWSEL1
BWSEL0</td><td>I</td><td>3-Level</td><td>Bandwidth Select.
Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Rate Precision Clock Family Reference Manual.</td></tr>
<tr><td>27
26
25
24</td><td>FRQSEL3
FRQSEL2
FRQSEL1
FRQSEL0</td><td>I</td><td>3-Level</td><td>Multiplier Select.
Three level inputs that select the input clock and clock multiplication ratio, depending on the FRQTBL setting. Consult the Any-Rate Precision Clock Family Reference Manual or DSPLLsim configuration software for settings, both available for download at www.silabs.com/timing.</td></tr>
<tr><td>33
30</td><td>SFOUT0
SFOUT1</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for both CKOUT1 and CKOUT2. Valid settings include LVPECL, LVDS, and CML. Also includes selections for CMOS mode, tristate mode, and tristate/sleep mode.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>Reserved</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Tristate/Sleep</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 3. Si5322 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
34 35	CKOUT2– CKOUT2+	O	Multi	**Clock Output 2.** Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
29 28	CKOUT1– CKOUT1+	O	Multi	**Clock Output 1.** Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
7, 18, 19, 20, 36	NC	—	—	**No Connect.** These pins must be left unconnected for normal operation.
GND PAD	GND	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.

3. Ordering Guide

Ordering Part Number	Package	Temperature Range
Si5322-B-GM	36-Lead 6 x 6 mm QFN	–40 to 85 °C

4. Package Outline: 36-Lead QFN

Figure 2 illustrates the package details for the Si5322. Table 4 lists the values for the dimensions shown in the illustration.

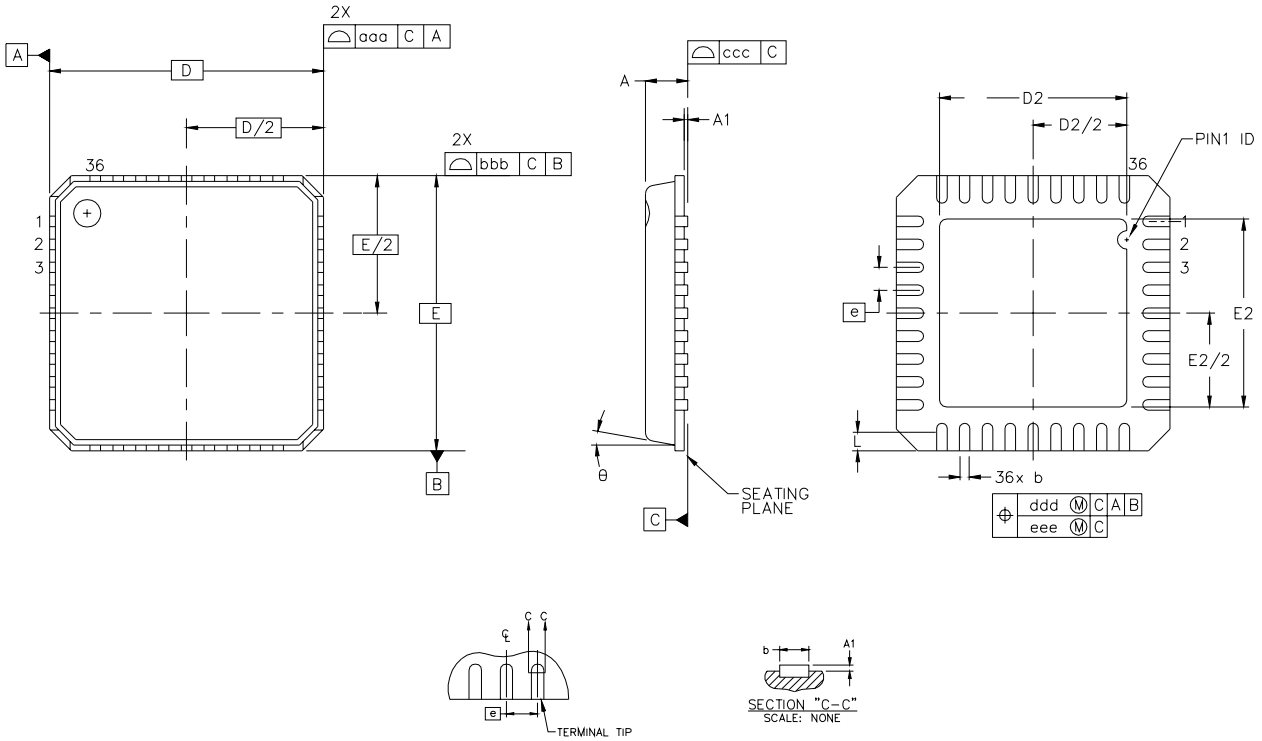


Figure 2. 36-Pin Quad Flat No-lead (QFN)

Table 4. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D		6.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		6.00 BSC	
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.75
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.05
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

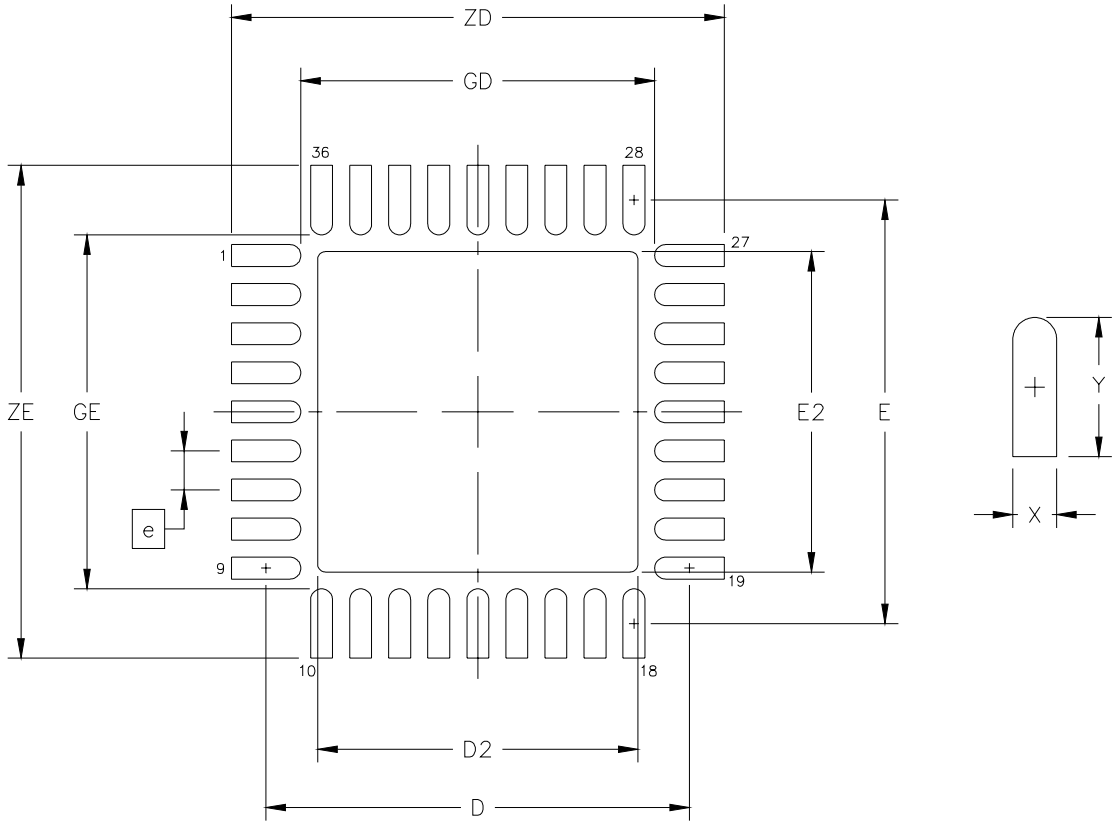


Figure 3. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.44 to Revision 0.45

- Condensed format.

Revision 0.45 to Revision 0.46

- Removed references to latency control, INC, and DEC in figures and text.
- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated “2. Pin Descriptions: Si5322”.
- Added “5. Recommended PCB Layout”.

Revision 0.46 to Revision 0.47

- Removed Figure 1. “Typical Phase Noise Plot.”
- Changed pins 11 and 15 from NC to VDD in “2. Pin Descriptions: Si5322”.

NOTES:

CONTACT INFORMATION

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