NIPPON PRECISION CIRCUITS INC.

SM6452AM/BM

Audio Variable Volume ICs

OVERVIEW

The SM6452AM/BM are serial-control electronic variable volume ICs for audio applications. They provide electronic volume control for 6 channels, with independent channel gain, attenuation and muting. They feature enhanced digital zip noise suppression. The serial control options are 3-wire interface (SM6452AM) and I^2C bus (SM6452BM). The SM6452AM/BM are available in 24-pin SSOP packages.

FEATURES

- 6-channel input/output (positive-phase-sequence output)
- Attenuation function
  - 6-channel independent control
  - +16 to 0 to –79dB variable range
  - 1.0 dB/step adjustment
  - Mute function
- Microcontroller interface
  - 3-wire serial data interface (SM6452AM)
  - I^2C bus format 2-wire control (SM6452BM) *1
  - I^2C address = 1000000
- Low noise
  - ≤ 0.002% THD + noise
  - ≤ 10µVrms residual noise
- $0.5AV_{DD}$ analog reference voltage source built-in
- Power supply
  - 7 to 13V analog supply
  - 2.7 to 5.5V digital supply
- Molybdenum-gate CMOS process
- 24-pin SSOP

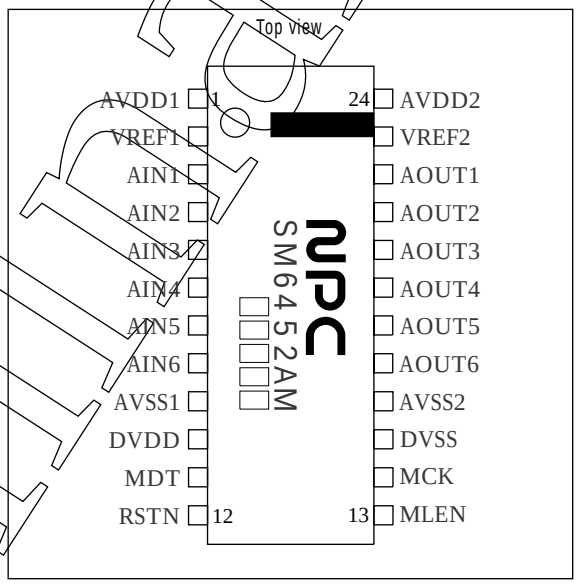
ORDERING INFORMATION

Device	Package
SM6452AM	24-pin SSOP
SM6452BM	24-pin SSOP

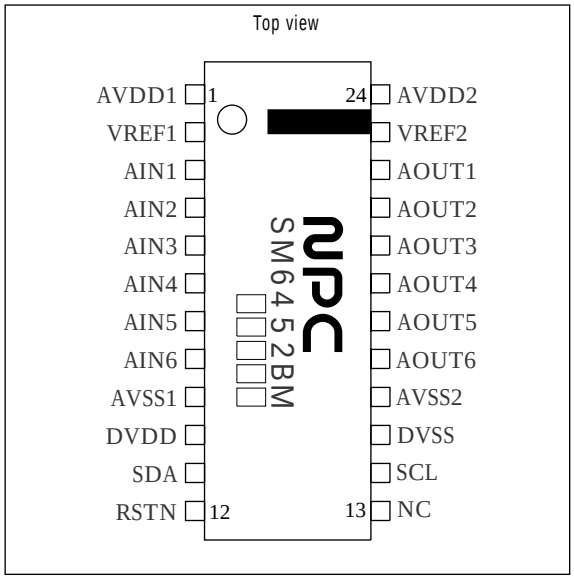
*1. I^2C bus is a registered trademark of Philips Electronics N.V.

PINOUT

SM6452AM

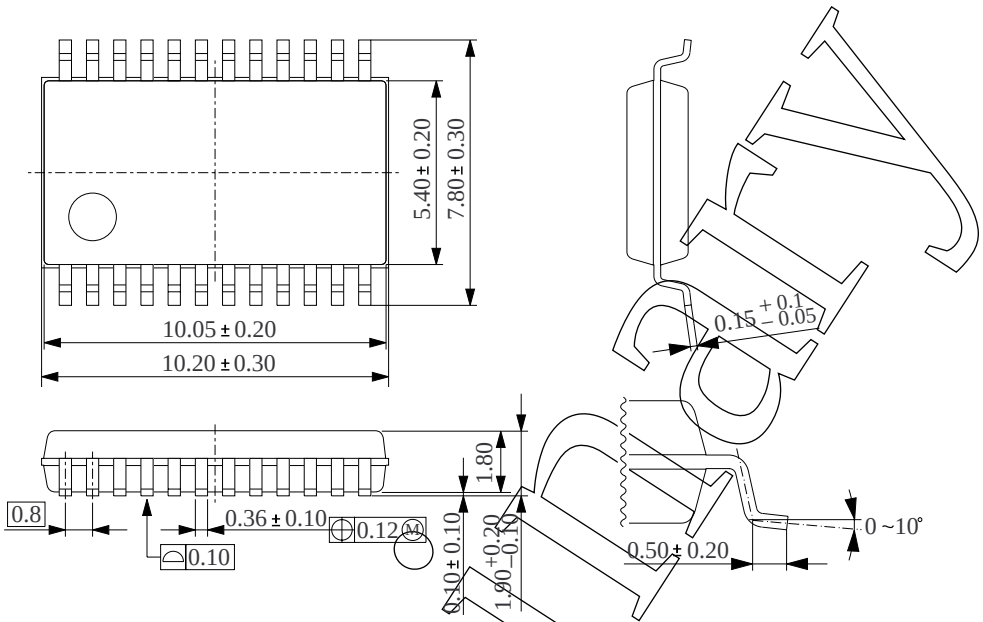


SM6452BM

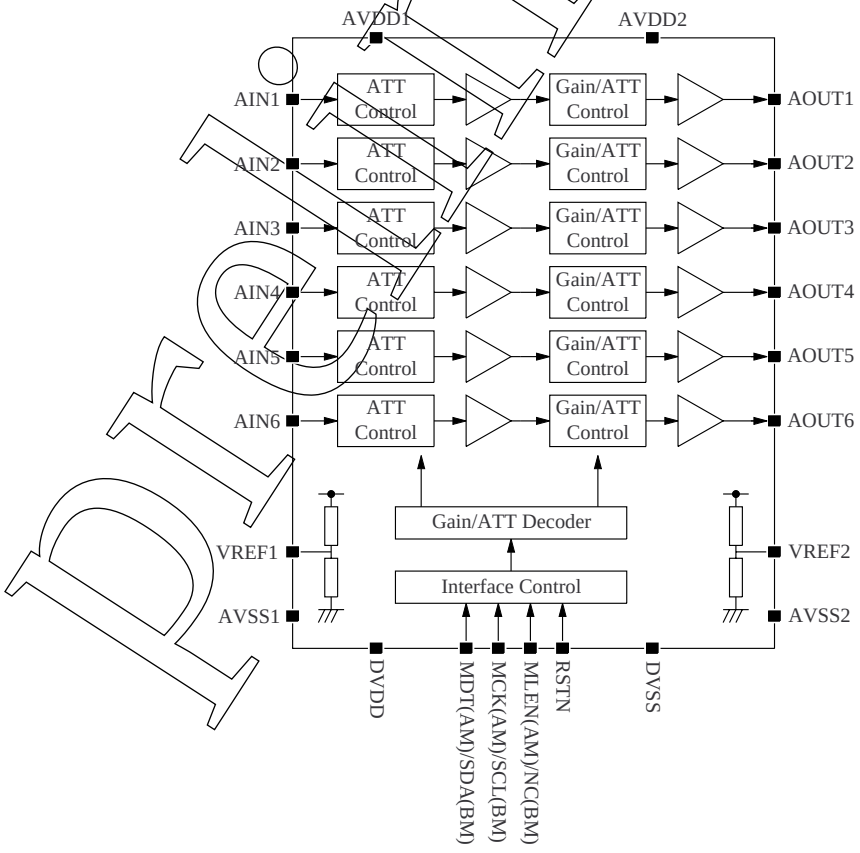


PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O[1]	A/D[2]	Description
1	AVDD1	–	A	Analog supply 1
2	VREF1	O	A	Reference voltage source capacitor connection (0.5AVDD1)
3	AIN1	I	A	Channel 1 audio input
4	AIN2	I	A	Channel 2 audio input
5	AIN3	I	A	Channel 3 audio input
6	AIN4	I	A	Channel 4 audio input
7	AIN5	I	A	Channel 5 audio input
8	AIN6	I	A	Channel 6 audio input
9	AVSS1	–	A	Analog ground 1
10	DVDD	–	D	Digital supply
11	MDT (AM)	I	D	Microcontroller data input
	SDA (BM)	I/O	D	I^2C bus serial data input and acknowledge (ACK) signal output
12	RSTN	Ip	D	System reset input (active LOW-level)
13	MLEN (AM)	Ip	D	Microcontroller latch enable input
	NC (BM)	–	–	No connection
14	MCK (AM)	I	D	Microcontroller clock input
	SCL (BM)	I	D	I^2C bus clock input
15	DVSS	–	D	Digital ground
16	AVSS2	–	A	Analog ground 2
17	AOUT6	O	A	Channel 6 audio output
18	AOUT5	O	A	Channel 5 audio output
19	AOUT4	O	A	Channel 4 audio output
20	AOUT3	O	A	Channel 3 audio output
21	AOUT2	O	A	Channel 2 audio output
22	AOUT1	O	A	Channel 1 audio output
23	VREF2	O	A	Reference voltage source capacitor connection (0.5AVDD2)
24	AVDD2	–	A	Analog supply 2

1. Ip = input pin with pull-up
2. A = analog, D= digital

SPECIFICATIONS

Absolute Maximum Ratings

AVSS1 = AVSS2 = DVSS = 0V, AVDD1 = AVDD2 = AV_{DD}, DVDD = DV_{DD}

Parameter	Symbol	Rating[1]	Unit
Analog supply voltage	AV_{DD}	–0.3 to 15.0	V
Digital supply voltage	DV_{DD}	–0.3 to 7.0	V
Analog input voltage	V_{INA}	V_{SS} – 0.3 to AV_{DD} + 0.3	V
Digital input voltage	V_{IND}	V_{SS} – 0.3 to DV_{DD} + 0.3	V
I^2C bus signal input voltage (SDA, SCL)	V_{IOPEN}	10	V
Storage temperature range	T_{stg}	–55 to 125	°C
Power dissipation	P_D	TBD	mW

1. Ratings also apply at supply switch ON and OFF.

Recommended Operating Conditions

AVSS1 = AVSS2 = DVSS = 0V

Parameter	Symbol	Rating	Unit
Analog supply voltage	AV_{DD}	7.0 to 13.0	V
Digital supply voltage	DV_{DD}	2.7 to 5.5	V
Supply voltage deviation	$AV_{DD1} - AV_{DD2}$, $AV_{SS1} - AV_{SS2}$, $AV_{SS1} - DV_{SS}$, $AV_{SS2} - DV_{SS}$	±0.1	V
Operating temperature	T_{opr}	–40 to 85	°C

DC Characteristics (SM6452AM)

AV_{DD} = 7 to 13V, DV_{DD} = 2.7 to 5.5V, V_{SS} = 0V, T_a = –40 to 85°C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD current consumption	I_{DDD1}	Data transfer stopped, MDT = MCK = MLEN = RSTN = DV_{DD} = 5V	–	TBD	TBD	µA
	I_{DDD2}	Data transfer in progress, DV_{DD} = 5V	–	TBD	TBD	mA
AVDD1, AVDD2 current consumption	I_{DDA}		–	TBD	TBD	mA
MDT, MCK, MLEN, RSTN HIGH-level input voltage	V_{IH}		$0.7DV_{DD}$	–	–	V
MDT, MCK, MLEN, RSTN LOW-level input voltage	V_{IL}		–	–	$0.3DV_{DD}$	V
RSTN, MLEN input current	I_{IL1}	V_{IN} = 0V	–	TBD	TBD	µA
MDT, MCK input leakage current	I_{LL1}	V_{IN} = 0V	–	–	TBD	µA
	I_{LH1}	$V_{IN} = DV_{DD}$	–	–	TBD	µA
RSTN, MLEN input leakage current	I_{LH2}	$V_{IN} = DV_{DD}$	–	–	TBD	µA

DC Characteristics (SM6452BM)

AV_{DD} = 7 to 13V, DV_{DD} = 2.7 to 5.5V, V_{SS} = 0V, T_a = –40 to 85°C

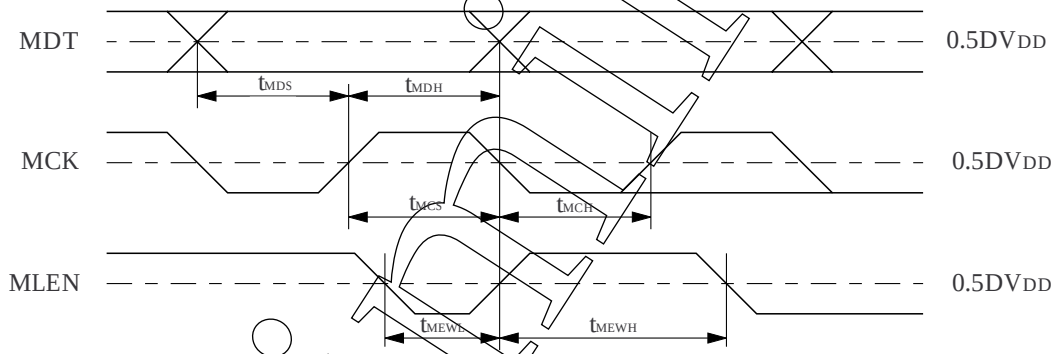
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD current consumption	I_{DDD1}	Data transfer stopped, SDA = SCL = RSTN = DV_{DD}	–	TBD	TBD	µA
	I_{DDD2}	Data transfer in progress	–	TBD	TBD	mA
AVDD1, AVDD2 current consumption	I_{DDA}		–	TBD	TBD	mA
SDA, SCL, RSTN HIGH-level input voltage	V_{IH}		$0.7DV_{DD}$	–	–	V
SDA, SCL, RSTN LOW-level input voltage	V_{IL}		–	–	$0.3DV_{DD}$	V
RSTN input current	I_{IL1}	V_{IN} = 0V	–	TBD	TBD	µA
SDA, SCL input current	I_{IL2}	V_{IN} = 0V	–	TBD	TBD	µA
RSTN input leakage current	I_{LH1}	$V_{IN} = DV_{DD}$	–	–	TBD	µA
SDA, SCL input leakage current	I_{LH2}	$V_{IN} = DV_{DD}$	–	–	TBD	µA
	I_{LH3}	V_{IN} = 10V	–	–	TBD	µA
SDA LOW-level output voltage	V_{OL}	ACK signal output, 3mA input current	TBD	–	TBD	V

AC Digital Characteristics (SM6452AM)

AV_{DD} = 7 to 13V, DV_{DD} = 2.7 to 5.5V, V_{SS} = 0V, T_a = –40 to 85°C

Serial inputs (MDT, MCK, MLEN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
MCK, MLEN rise time	t_r	–	–	100	ns
MCK, MLEN fall time	t_f	–	–	100	ns
MDT setup time	t_{MDS}	50	–	–	ns
MDT hold time	t_{MDH}	50	–	–	ns
MLEN setup time	t_{MCS}	50	–	–	ns
MLEN hold time	t_{MCH}	50	–	–	ns
MLEN LOW-level pulsewidth	t_{MEWL}	50	–	–	ns
MLEN HIGH-level pulsewidth	t_{MEWH}	50	–	–	ns



Reset input (RSTN)

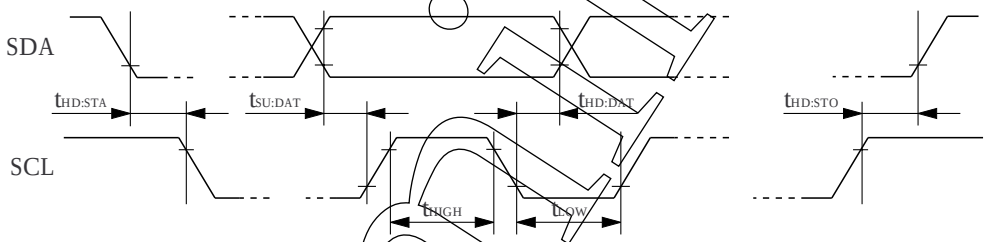
Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	100	–	–	ns

AC Digital Characteristics (SM6452BM)

AV_{DD} = 7 to 13V, DV_{DD} = 2.7 to 5.5V, V_{SS} = 0V, T_a = –40 to 85°C

Serial inputs (SDA, SCL)

Parameter	Symbol	Rating			Unit
		min	typ	max	
SCL hold time (start)	$t_{HD:STA}$	4.0	–	–	µs
SCL setup time (stop)	$t_{SU:STA}$	4.0	–	–	µs
SDA hold time	$t_{HD:DAT}$	5.0	–	–	µs
SDA setup time	$t_{SU:DAT}$	250	–	–	ns
SCL clock HIGH-level pulsewidth	t_{HIGH}	4.0	–	–	µs
SCL clock LOW-level pulsewidth	t_{LOW}	4.7	–	–	µs
SCL rise time	t_r	–	–	1000	ns
SCL fall time	t_f	–	–	300	ns



Reset input (RSTN)

Parameter	Symbol	Rating			Unit
		min	typ	max	
RSTN LOW-level pulsewidth	t_{RSTN}	100	–	–	ns

AC Analog Characteristics

AV_{DD} = 9V, DV_{DD} = 5V, (TBD)Vrms analog input amplitude, 1kHz analog input frequency, 100kΩ output load resistance, T_a = 25°C, AC-coupled inputs

Analog inputs (AIN1 to AIN6)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference input amplitude	V_{AI}		–	TBD	–	Vrms
Input resistance[1]	R_{IN}	ATT = 0dB	TBD	TBD	TBD	Ω
Input clipping voltage	V_{CLP}	THD + N = 1%, ATT = 0dB	–	TBD	–	Vrms

1. R_{IN} varies with the ATT setting. See figure 11 in the Analog Performance Characteristics section.

Analog outputs (AOUT1 to AOUT6)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Residual noise voltage	V_{NS}	Input signal: 0Vrms, A-weight filter, 0dBr = (TBD)Vrms, ATT = 0dB	–	TBD	TBD	μVrms
Signal-to-noise ratio	SNR		TBD	TBD	–	dBr
Total harmonic distortion + noise	THD + N	ATT = 0dB, 20kHz lowpass filter	–	TBD	TBD	%
Gain control range	R_{CNT}		–79	–	+16	dB
Step size	Step		0.8	1.0	1.5	dB
Attenuation error (1 to 20kHz)	ERR_1	+16 to –60dB	TBD	–	TBD	dB
	ERR_2	–61 to –79dB	TBD	–	TBD	dB
Absolute attenuation (1kHz)	AT_0	ATT = 16dB	–	TBD	–	dB
	AT_1	ATT = 0dB	–	TBD	–	dB
	AT_2	ATT = –20dB	–	TBD	–	dB
	AT_3	ATT = –40dB	–	TBD	–	dB
	AT_4	ATT = –60dB	–	TBD	–	dB
	AT_5	ATT = –79dB	–	TBD	–	dB
Mute attenuation (1kHz)	Mute	ATT = Mute	TBD	TBD	–	dB
Channel crosstalk[1]	CT	ATT = 0dB	TBD	TBD	–	dB
Frequency response	FR	ATT = 0dB, f = 200kHz	–	TBD	–	dB
Quiescent output zip noise voltage[2]	N_J	0Vrms input signal	–	–	TBD	mVp-p
Minimum driver load resistance	R_{ML}	ATT = 0dB, THD + N = 1%	TBD	TBD	–	Ω

1. Leakage to other channels when analog input is applied to one channel only.
2. Noise occurring when the ATT setting is changed (peak to peak)

Reference voltage (VREF1, VREF2)

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reference voltage output	V_{REF}		$0.45AV_{DD}$	$0.5AV_{DD}$	$0.55AV_{DD}$	V

MEASUREMENT CIRCUIT

TBD

MICROCONTROLLER INTERFACE

SM6452AM

Transfer format

The SM6452AM uses a 3-wire serial interface to select channels and set attenuation levels. The transfer format is shown in figure 1.

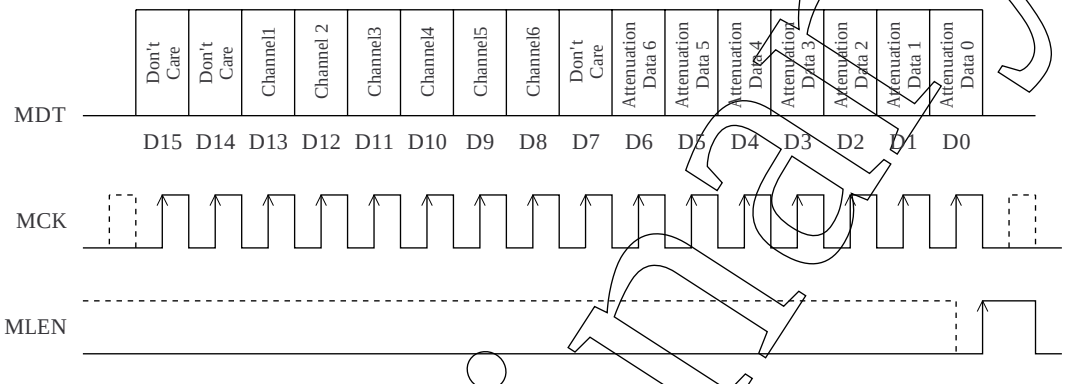


Figure 1. Microcontroller input data timing

Data is shifted into the internal shift register on the rising edge of MCK, and the attenuation value is loaded and changed on the rising edge of MLEN. Accordingly, data on MDT should be changed on the falling edge of MCK. The dotted lines for MCK and MLEN also indicate valid timing.

Data description (D15 to D0)

In the following description, LOW implies V_{IL} level and HIGH implies V_{IH} level.

- D15, D14
  Don't care.
- D13 to D8
  Chip address bits. Each of 6 channels is set when the corresponding bit is set HIGH.
  - D13: channel 1
  - D12: channel 2
  - D11: channel 3
  - D10: channel 4
  - D9: channel 5
  - D8: channel 6
- D7 to D0
  Gain/attenuation set bits. The gain/attenuation setting for ATT register settings are shown in table 1.

SM6452BM

Transfer format

The SM6452BM uses Philips I^2C interface to select channels and set attenuation levels. For details of the I^2C bus, refer to Philips "I^2C Bus Specification Description". Here, we describe only the aspects for controlling the SM6452BM. The transfer format is shown in figure 2.

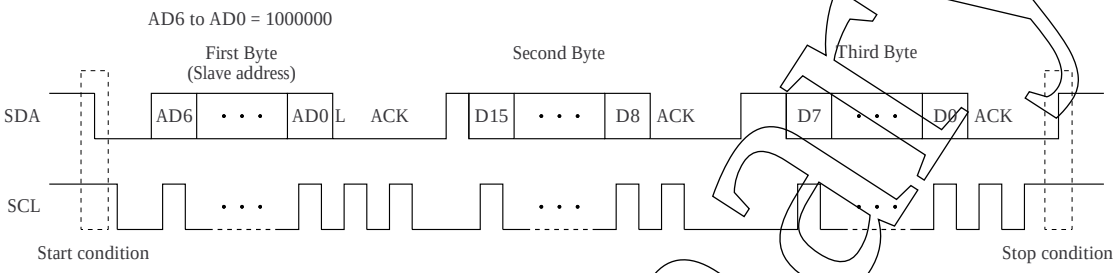


Figure 2. Microcontroller input data timing

As shown in figure 2, the data format comprises 3 bytes. After the SM6452BM receives 8 bits for each byte, an acknowledge signal (ACK) on SDA goes LOW to confirm the data transfer.

Data format

- Byte 1 (slave address)
  The first byte is slave address. The SM6452BM address (AD6 to AD0) is 1000000. The 8th bit indicates information write and should be set LOW.
- Bytes 2 and 3
  Bytes 2 and 3 are the channel select and gain/attenuation level set bits. Byte 2 represents data bits D15 to D8, and byte 3 represents data bits D7 to D0.

Data description (D15 to D0)

- D15, D14
  Don't care.
- D13 to D8
  Chip address bits. Each of 6 channels is set when the corresponding bit is set HIGH.
  - D13: channel 1
  - D12: channel 2
  - D11: channel 3
  - D10: channel 4
  - D9: channel 5
  - D8: channel 6
- D7 to D0
  Gain/attenuation set bits. The gain/attenuation setting for ATT register settings are shown in table 1.

Attenuation settings

Table 1. ATT settings

Attenuation[1]	ATT_H	D7	D6	D5	D4	D3	D2	D1	D0
16dB	00	×	LOW	LOW	LOW	LOW	LOW	LOW	LOW
15dB	01	×	LOW	LOW	LOW	LOW	LOW	LOW	HIGH
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
1dB	0F	×	LOW	LOW	LOW	HIGH	HIGH	HIGH	HIGH
0dB	10	×	LOW	LOW	HIGH	LOW	LOW	LOW	LOW
–1dB	11	×	LOW	LOW	HIGH	LOW	LOW	LOW	HIGH
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
–15dB	1F	×	LOW	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
–16dB	20	×	LOW	HIGH	LOW	LOW	LOW	LOW	LOW
–17dB	21	×	LOW	HIGH	LOW	LOW	LOW	LOW	HIGH
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
–78dB	5E	×	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	LOW
–79dB	5F	×	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	HIGH
Mute	6×	×	HIGH	HIGH	LOW	×	×	×	×
Mute	7×	×	HIGH	HIGH	HIGH	×	×	×	×

1. Outputs are muted after system reset. The ATT hex code is determined by D6 to D0 only.

ANALOG PERFORMANCE CHARACTERISTICS

AV_{DD} = 9V, DV_{DD} = 5V, 100kΩ output load resistance, T_a = 25°C

TBD

Figure 3. THD + N vs. input amplitude

TBD

Figure 4. THD + N vs. frequency

TBD

Figure 5. Gain/attenuation error

TBD

Figure 6. Residual noise vs. ATT

TBD

Figure 7. Frequency response

TBD

Figure 8. Crosstalk frequency response

TBD

Figure 9. FFT spectrum

TBD

Figure 10. THD + N vs. load resistance

TBD

Figure 11. Input resistance vs. ATT

TBD

Figure 12. Current consumption vs. supply voltage

TBD

Figure 13. Current consumption vs. temperature

TYPICAL APPLICATIONS

TBD

NPC
NIPPON PRECISION CIRCUITS INC.

NIPPON PRECISION CIRCUITS INC.

4-3, Fukuzumi 2-chome
Koto-ku, Tokyo 135-8430, Japan
Telephone: 03-3642-6661
Facsimile: 03-3642-6698

NP9917BE 2000.1