■ OVERVIEW

The SM8505 is an LSI designed specifically for infrared remote control receivers. This LSI demodulates the pulse position modulation signal received by the photodetector and converts it to 7-bit parallel data. Given an external synchronizing clock, the LSI can also output serial data. The SM8505 is function- and pin-compatible with Mitsubishi's M50117BP. The SM8505 is available in 18-pin plastic DIP.

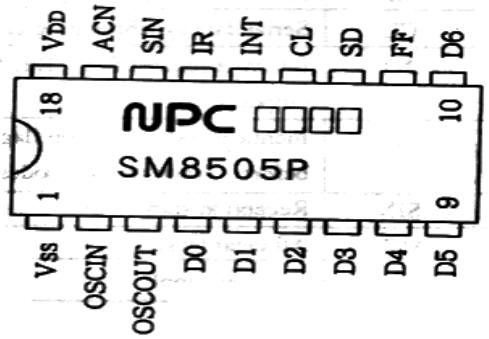
■ FEATURES

- Function- and pin-compatible with Mitsubishi's M50117BP
- Monolithic CMOS LSI
- Internal oscillation circuitry
- Demodulation of pulse position modulation signal
- 7-bit parallel data output
- Serial data output
- Single +5 V power supply
- CMOS construction
- 18-pin plastic DIP

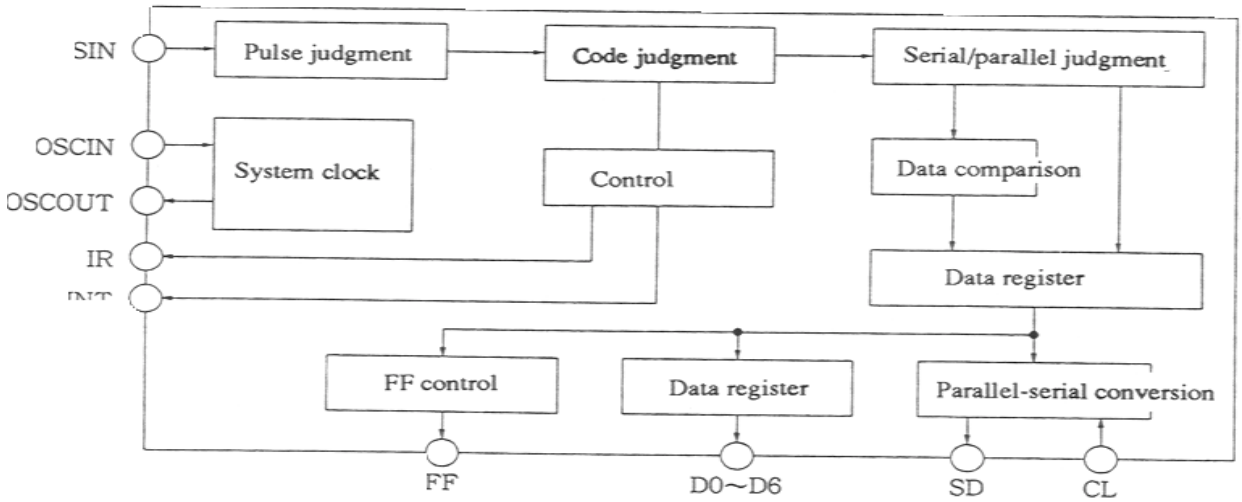
■ PINOUT

TOP VIEW

- 18-pin DIP



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

<table>
<tr><th>No.</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>Vss</td><td>GND</td></tr>
<tr><td>2</td><td>OSCIN</td><td>Oscillator circuit input</td></tr>
<tr><td>3</td><td>OSCOUT</td><td>Oscillator circuit output</td></tr>
<tr><td>4</td><td>D0</td><td>Data D0 output</td></tr>
<tr><td>5</td><td>D1</td><td>Data D1 output</td></tr>
<tr><td>6</td><td>D2</td><td>Data D2 output</td></tr>
<tr><td>7</td><td>D3</td><td>Data D3 output</td></tr>
<tr><td>8</td><td>D4</td><td>Data D4 output</td></tr>
<tr><td>9</td><td>D5</td><td>Data D5 output</td></tr>
<tr><td>10</td><td>D6</td><td>Data D6 output</td></tr>
<tr><td>11</td><td>FF</td><td>Flip-flop output. FF changes only when the specified codes are input. The table below shows the relation between FF and transmission codes.
<table>
<tr><th>D0</th><th>D1</th><th>D2</th><th>D3</th><th>D4</th><th>D5</th><th>D6</th><th></th></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>FF pin H</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>FF pin L</td></tr>
</table>
FF will not change when other codes are input.</td></tr>
<tr><td>12</td><td>SD</td><td>Serial data output. High impedance when no clock is input to the CL pin.</td></tr>
<tr><td>13</td><td>CL</td><td>Serial data synchronizing clock input</td></tr>
<tr><td>14</td><td>INT</td><td>Interrupt request flag. This flag indicates that sent data is stored correctly so that serial data can be output.</td></tr>
<tr><td>15</td><td>IR</td><td>Identical code reception flag. Received data is compared with the code received immediately before. When the two codes are identical, this flag goes "H".</td></tr>
<tr><td>16</td><td>SIN</td><td>Reception signal input</td></tr>
<tr><td>17</td><td>ACN</td><td>All clear (reset)</td></tr>
<tr><td>18</td><td>VDD</td><td>+ power supply</td></tr>
</table>

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply voltage	V_{DD} ~ V_{SS}	-0.3 to +7.0	V
Input voltage	V_{IN}	Vss-0.3 to V_{DD} +0.3	V
Output voltage	V_{OUT}	Vss-0.3 to V_{DD} +0.3	V
Storage temperature	T_{STG}	-40 to +125	°C
Power dissipation	P_W	250	mW
Soldering temperature	T_{SLD}	260	°C
Soldering time	t_{SLD}	10	Sec

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	4.5 to 5.5	V
Oscillation frequency	fosc	480 or 455	kHz
Operating temperature	t_{OPR}	-30 to +70	°C

■ ELECTRICAL CHARACTERISTICS

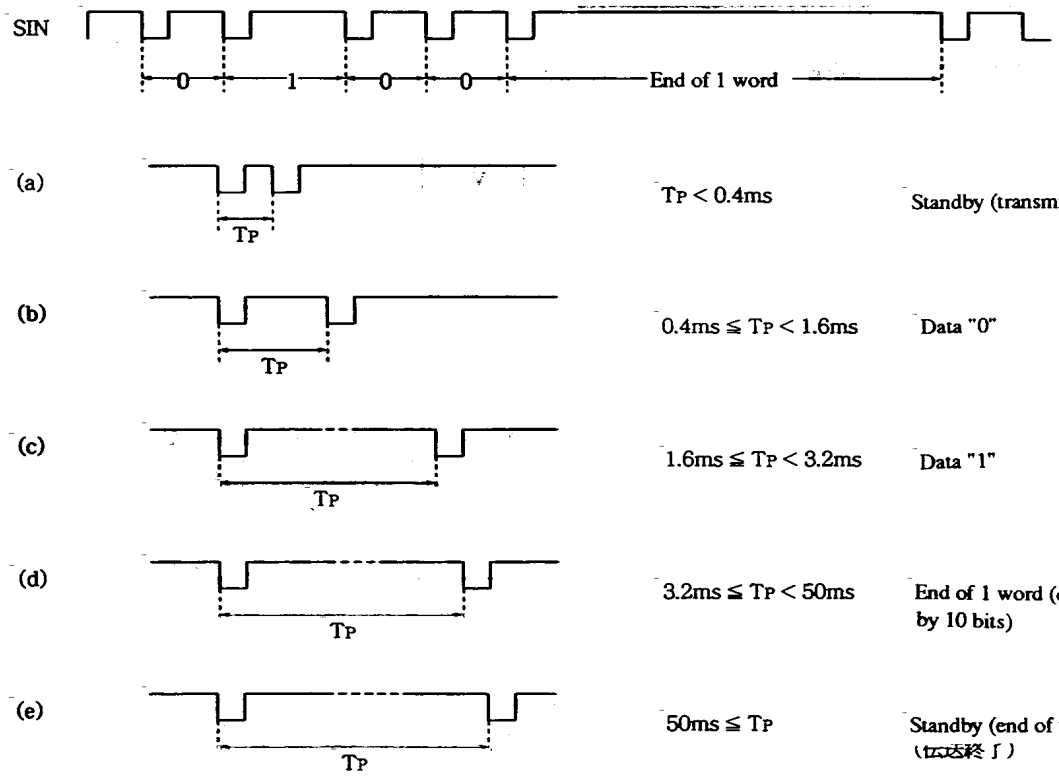
V_{DD} = 5V ± 10%, Ta=-30 to +70°C

ITEM	SYMBOL	SYMBOL	CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
Supply voltage	V_{DD}			4.5	5.0	5.5	V
Supply current	I_{DD}		fosc=455kHz		0.3	1.0	mA
H input voltage	V_{IH}	All input pins		$0.7V_{DD} \le V_{IH} \le V_{DD}$			V
L input voltage	V_{IL}	All output pins		$0 \le V_{IL} \le 0.3V_{DD}$			V
H output current 1	I_{OH1}	SD	V_{OH}=2.4H	-2.0	-6.0		mA
H output current 2	I_{OH2}	IR, INT	V_{OH}=2.4H	-1.0	-3.0		mA
H output current 3	I_{OH3}	D0 to D6, FF	V_{OH}=2.4H	-0.5	-1.5		mA
L output current	I_{OL}	All output pins	V_{OL}=0.4V	1.6	3.2		mA
Pull-up resistor 1	RI1	SIN			30		kΩ
Pull-up resistor 2	RI2	ACN			60		kΩ
Pull-down resistor	RI	CL			45		kΩ

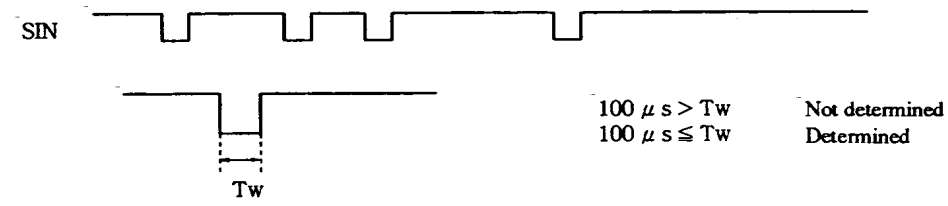
■ FUNCTIONAL DESCRIPTION

The SM8505 demodulates serial "pulse position modulation signals" into 7-bit parallel data (D0 - D6). When an external clock is input to the CL pin, the SD pin outputs serial data synchronized with the given clock.

1. Pulse position modulation data
   (1) Meaning and judgment of pulse position modulation data
   The pulse position modulation signal received with the photodetector (see the figure below) is input to the SIN pin of the SM8505.

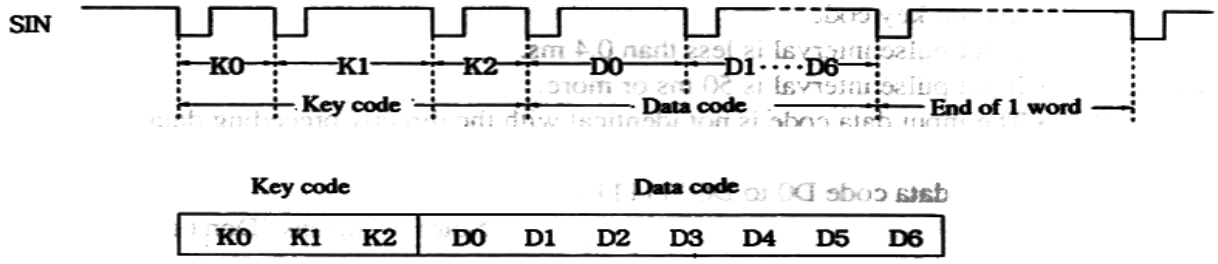


   (2) Pulse judgment



The pulse is not judged correctly unless its width Tw is 100 μs or longer. (When Tw is from 50 to 100 μs, the pulse may or may not be determined due to the relation with the internal clock positions.)

(3) Configuration of 1 word



Data starts from a 3-bit key code, which is followed by D0, D1, D2, to D6 (total 10 bits). After this data, an interval of 3.2 ms to50 ms follows. This interval indicates the end of one word.

(4) Key code

Key code has 3-bit code for identifying the type of remote controller. The SM8505 uses the following key code. Its code stands before 7-bit data code.

	K0	K1	K2
Key code	0	1	0

(5) Data code

Data code D0 to D6 are input following the key code. The data code shown below has a special meaning.

	D0	D1	D2	D3	D4	D5	D6		
Data code	0	0	0	0	0	–	–	Standby,	
	1	1	1		1	–	–	Standby,	
	1	0		0	0	0	0	FF pin	H
	0	1	0	1	0	0	0	FF pin	L

(Note) "-" means "Arbitrary".

2. SM8505 operation

(1) Initial state

State after ACN (reset). The initial state of each output pin is as follows:

- Data output D0 to D6 - L
- FF output FF - L
- Serial data output SD - high impedance
- Interrupt flag INT - L
- Identical code reception flag IR - L

(2) Standby state

Data input wait state. The standby state is set when the following pulse is input to the reception signal input SIN pin.

- Invalid key code
- Input pulse interval is less than 0.4 ms.
- Input pulse interval is 50 ms or more.
- The input data code is not identical with the directly preceding data.
- Input data code D0 to D6 "00000--"
- Input data code D0 to D6 "11111--"

Note) "-" means "Don't care."

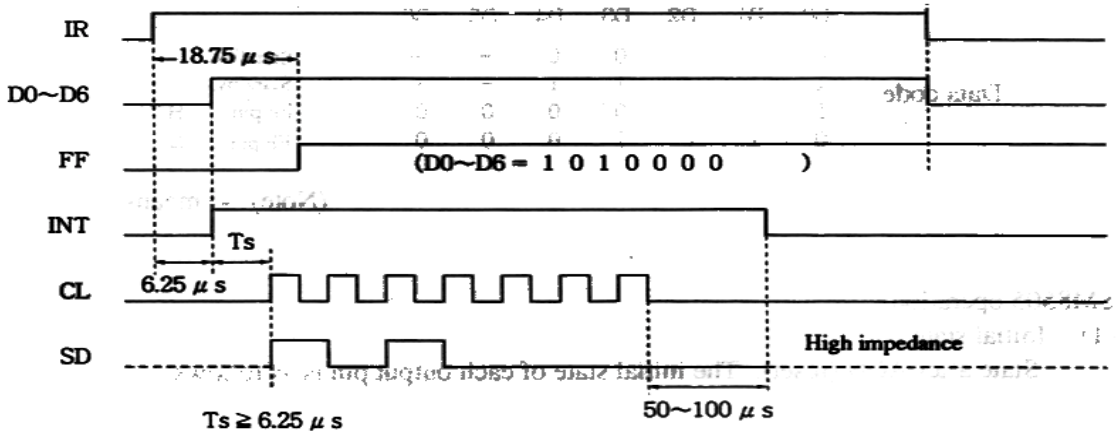
Each output pin is in the following state during standby:

• Data output	D0 to D6 L	
• FF output	FF .... retained	
• Serial data output	SD .... (high impedance)	Note)
• Interrupt flag	INT .... (L)	Note)
• Identical code reception flag	IR L	

Note) While data is being transferred, the serial data output SD and the interrupt flag INT do not enter this state until data transfer is completed. (See the TIME CHART.)

(3) Reception state

When data input from SIN matches the directly preceding data, IR and INT go "H", and output pins D0 to D6 become active. When INT is "H", inputting an external clock to the CL pin synchronizes the serial data output from the SD pin with the input clock. The timing chart is shown below.



The following explanation is in order of operation.

(a) After the same code is received, IR goes "H".

(b) D0 to D6 and INT go "H" 6.24 µs after IR goes "H".

(c) FF changes 18.75 µs after IR goes "H".

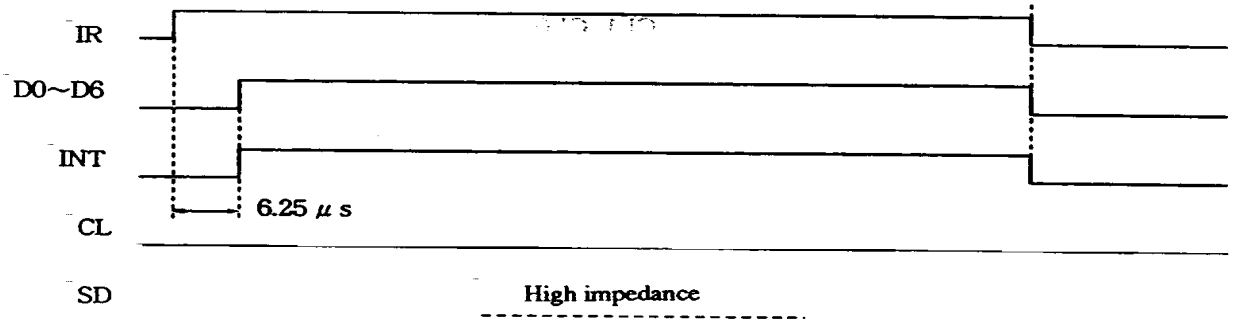
(d) The external clock CL input becomes valid 6.25 µs after INT goes "H". That is, Ts (period from INT's "H" to the rising edge of the clock) must be at least 6.25 µs.

(e) INT goes "L" and SD becomes a high impedance 50 to 100 µs after the 7th falling edge of the external clock.

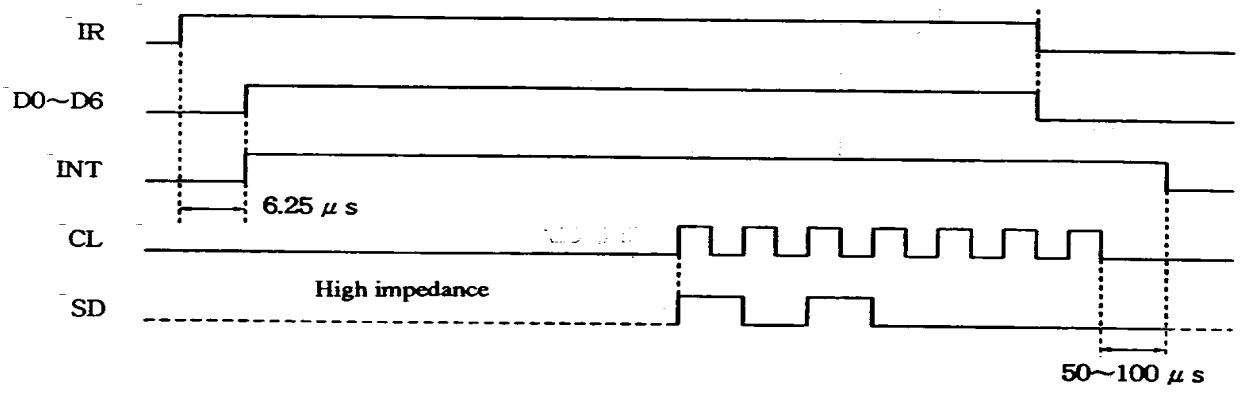
(f) When the standby state is set due to an invalid input code or other condition, IR and D0 to D6 simultaneously go "L". When no external clock is input after INT goes "H", INT goes "L" at the same time.

* SD output in (e): INT and SD outputs remain active until 7 clocks are input if even only one falling edge of CL is detected. In this period, serial data is not affected by any change in the data code.

(No clock is input to CL)



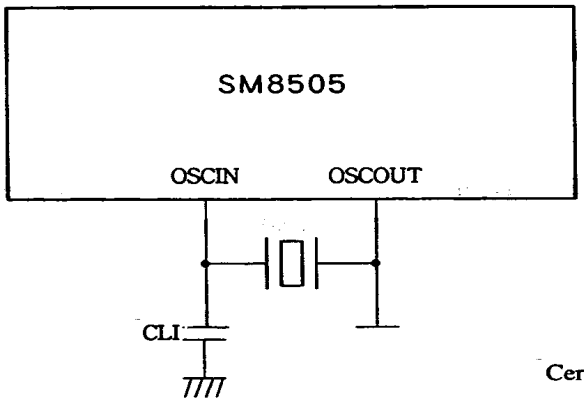
(IR goes "L" in the middle of serial data transfer.)



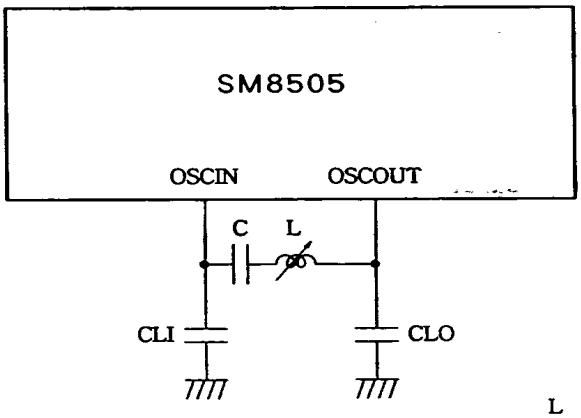
■ OSCILLATION CIRCUIT AND POWER-ON CLEAR CIRCUIT

1. Oscillation circuit example

The SM8505 incorporates an oscillation circuit. An internal clock can be generated by connecting an LC circuit or a ceramic oscillator between OSCIN and OSCOUT. Examples are shown below.



Ceramic oscillator: CSB455C
(Murata Manufacturing)
CL1, CL0: 50 to 100pF



L : 2.5mH
CLI, CLO : 90pF
C : 0.1 μF

2. Power-on clear circuit

The SM8505 can be made to reset at power-on by connecting a capacitor to the ACN pin . The graph below shows the qualitative relation between the supply voltage and the ACN pin voltage. The time from when the supply voltage VDD reaches 2.5 V until ACN rises to 0.3 VDD (i.e., time TACN) must be 1 ms or more. The external circuit shown below resets the SM8505 without fail each time the power is turned on. (Select the capacitance so that TACN ≥ 1 ms.)