-48V Programmable Hot Swap Sequencing Power Controller

FEATURES AND APPLICATIONS

Features:

- **Soft Starts Main Power Supply on Card Insertion or System Power Up**
- **In-Rush Current Limiting**
- **Master Enable to Allow System Control of Power Up or Down**
- **Programmable Independent Control of up to 4 DC/DC Converters via 4 Power Good Signals, PG[4:1]#**
- **Highly Programmable Circuit Breaker Level and Mode**
  - **Programmable Quick-Trip™ Value, Current Limiting, Duty Cycle Times, and Over-Current Filter**
- **Programmable Host Voltage Fault Monitoring**
  - **Programmable UV/OV Filter and UV Hysteresis**
- **Programmable Fault Mode: Latched or Duty Cycle**
- **Internal Shunt Regulator Allows for a Wide Supply Range (typically -32 to -72 Volts)**
- **I^2C 2-Wire Serial Bus Interface for Programming, Power On/Off and Operational Status**

Applications:

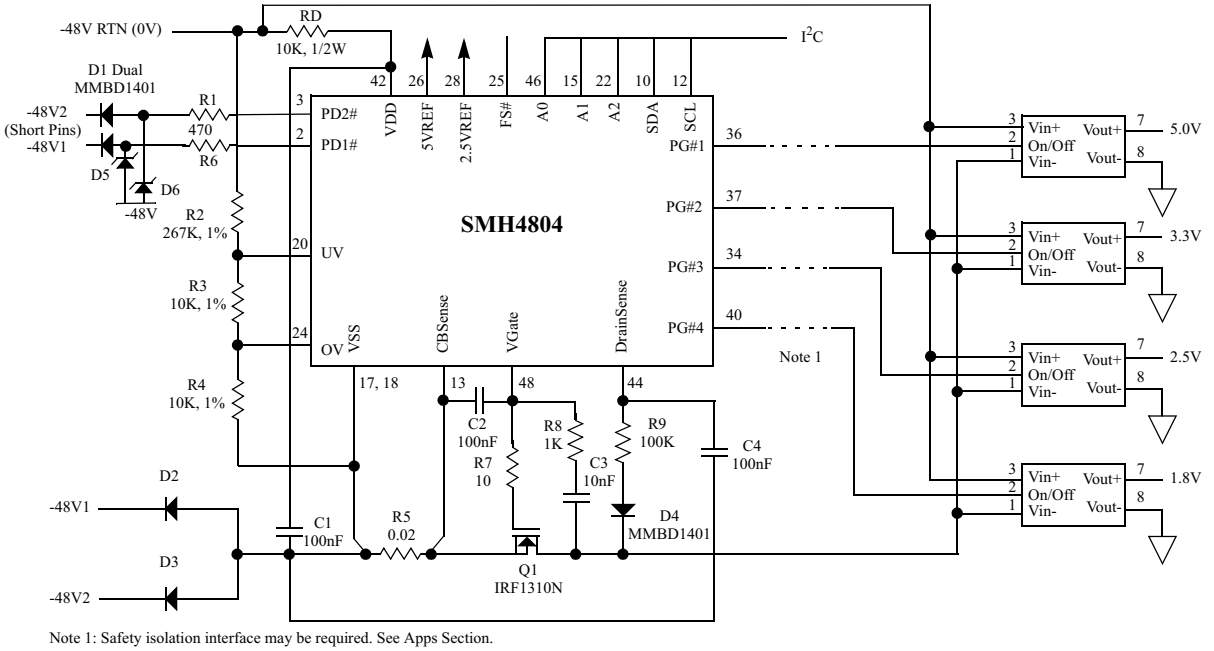
- **Telecom Hot-Swap Card**
- **Distributed Power Architectures**
- **Power-on LAN, IEEE 802.3**

INTRODUCTION

The SMH4804 is a user-programmable -48V power supply controller designed to control the hot-swapping of plug-in cards and to sequence supplies in a distributed power environment. The SMH4804 drives an external power MOSFET switch that connects the bus side supply to the card side load and controls in-rush current while providing both current regulation and over-current protection. When the source and drain voltages of the external MOSFET are within specification, the SMH4804 asserts four PG[4:1]# power-good logic outputs either simultaneously or sequenced at programmable intervals to enable DC-DC converters to distribute card side power.

Additional features of the device include: UV and OV monitor, master enable or temperature sense input (EN/TS), 2.5V and 5V reference outputs for expanding monitor functions, two Pin-Detect enable inputs (PD1# and PD2#) for card insertion verification, and duty-cycle or latched over-current protection modes. All features are programmed in nonvolatile registers through the I^2C interface which is simplified with the SMX3200 interface adapter and Windows GUI software available from Summit Microelectronics. Engineers can program the device directly in-circuit with units of voltage, current and time, allowing fast design cycles.

SIMPLIFIED APPLICATION DRAWING



Note 1: Safety isolation interface may be required. See Apps Section.

Figure 1. SMH4804 Simplified Application Diagram

FUNCTIONAL BLOCK DIAGRAM

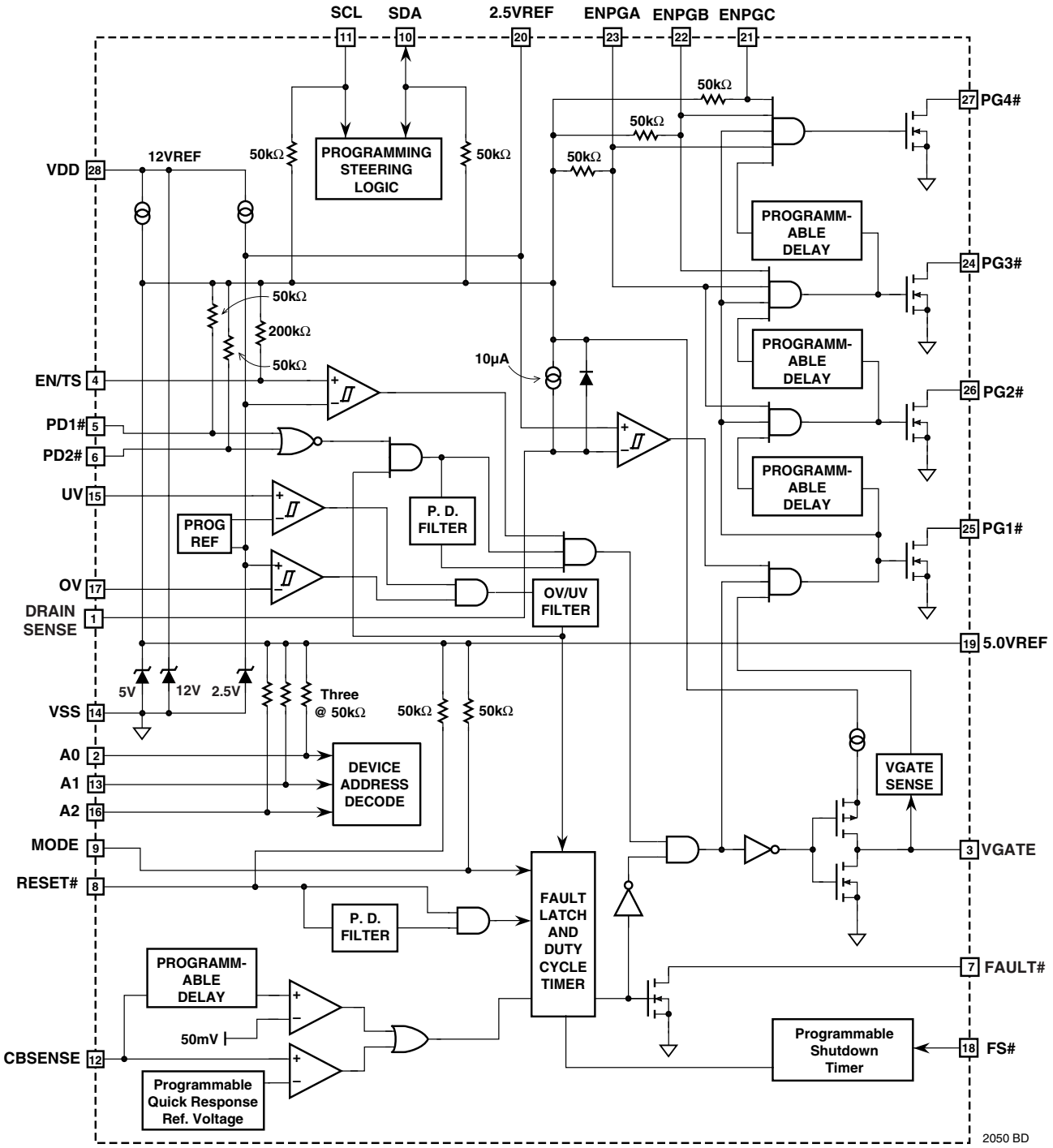


Figure 2. SMH4804 Block Diagram

FUNCTIONAL DESCRIPTION

The SMH4804 integrated hot swap power controller operates within a wide supply range, typically -32 to -72 volts, and generates the signals necessary to drive isolated-output DC/DC converters. The general start-up procedure is as follows:

- A physical connection must first be made with the chassis to discharge any electrostatic voltage potentials when a typical add-in board is inserted into the powered backplane.
- The board then contacts the long pins on the backplane that provide power and ground.
- As soon as power is applied the device starts up, but does not immediately apply power to the output load.
- Under-voltage and over-voltage circuits inside the controller verify that the input voltage is within a user-specified range.
- The SMH4804 senses the PD1# and PD2# pin detection signals to indicate the card is seated properly.

These requirements must be met for a Pin Detect Delay period of t_{PDD}. Once this time has elapsed, the hot-swap controller enables VGATE to turn on the external power MOSFET switch. The VGATE output is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. During the controlled turn-on period the V_{DS} of the MOSFET is monitored by the drain sense input. When DRAIN SENSE drops below 2.5V, and VGATE rises above $V_{DD} – V_{GT}$, the SMH4804 asserts the PG1# through PG4# power good outputs to enable the DC/DC controllers. The ENPGA, ENPGB, and ENPGC Power Good Enable inputs may be used to activate or deactivate specific output loads.

Steady-state operation is maintained as long as all conditions are normal. Any of the following events may cause the device to disable the DC/DC controllers by shutting down the power MOSFET:

- an under-voltage or over-voltage condition on the host power supply.
- an over-current event detected on the CBSENSE input
- a failure of the power MOSFET sensed via the DRAIN SENSE pin.
- the PD1#/PD2# pin detect signals becoming invalid.
- the master enable (EN/TS) falls below 2.5V.
- the FS# input is driven low by events on the secondary side of the DC/DC controllers.

The SMH4804 may be configured so that after any of these events occurs, the VGATE output shuts off and either latches into an off state, or recycles power after a cooling down period, t_{CYC}.

Powering V_{DD}

The SMH4804 contains an internal shunt regulator on the V_{DD} pin that prevents the voltage from exceeding 12V. It is necessary to use a dropper resistor (R_D) between the host power supply and the V_{DD} pin in order to limit current into the device and prevent possible damage. The dropper resistor allows the device to operate across a wide range of system supply voltages, typically -32 V to -72V, and also helps protect the device against common-mode power surges. Refer to the Applications Section for help on calculating the R_D resistance value.

Hot-Swap Verification

There are several enabling inputs that allow the host to control the SMH4804. The Pin Detect signals (PD1# and PD2#) are two active low enables that are generally used to indicate that the add-in circuit card is properly seated. These inputs must be held low for a pin-detect delay period of t_{PDD} before a power-up sequence may be initiated. This is typically done by clamping the inputs to V_{SS} through the implementation of an ejector switch, or alternatively through the use of staggered pins at the card-cage interface. The pin detect delay (t_{PDD}) timing parameter is controlled by bits 1:0 of register 9. Refer to Register 9 - Address 1001 on page 38 for more information.

Two shorter pins, arranged at opposite ends of the connector, force the card to be fully seated before both pin detects are enabled. Care must be taken not to exceed the maximum voltage rating of these pins during the insertion process. Refer to details in the Applications Section for proper circuit implementation. Note that the PD1# and PD2# inputs are enabled or disabled using bit 0 of Register 3. Refer to Register 3 - Address 0011 on page 32 for more information.

The EN/TS input provides an active high comparator input that may be used as a master enable or temperature sense input. This input signal must exceed 2.5V (nominal) for proper operation. Refer to the Pin Descriptions on page 10 for more information.

Under-/Over-Voltage Sensing

The Under-Voltage (UV) and Over-Voltage (OV) inputs provide a set of comparators that act in conjunction with an external resistive divider ladder to sense whether or not the host supply voltage is within the user-defined limits. The power-up sequence is initiated when the input to the UV pin rises above 2.5V and the input to the OV pin falls below

2.5V for a period of at least t_{PDD} (Pin Detect Delay time). The t_{PDD} filter helps prevent spurious start-up sequences while the card is being inserted. If UV falls below 2.5V or OV rises above 2.5V, the PG[4:1]# and VGATE outputs are disabled immediately.

Under-/Over-Voltage Filtering

The SMH4804 can be configured so that an out-of-tolerance condition on UV/OV does not shut off the output immediately. Instead, a filter delay may be inserted so that only sustained under-voltage or over-voltage conditions can shut off the output. An out-of-tolerance condition on UV/OV for longer than the filter delay time (t_{UOFLTR} in Figure 3) causes the VGATE and PG[4:1]# outputs to shut off when the UV/OV filter option is enabled using bits 2:1 of Register 4. The under-/over-voltage filtering feature is disabled (bits 2:1 = 00) in the default configuration. Refer to Register 4 - Address 0100 on page 33 for more information on the filter delay options. The UV and OV filters are enabled and disabled by programming bits 3 and 2 of Register 6 respectively. Refer to Register 6 - Address 0110 on page 36 for more information. Note that the delay values in Register 4 are only valid if the corresponding over or under voltage filtering is enabled using bits 3:2 of Register 6.

Figure 3 shows the timing for the under-/over-voltage filter.

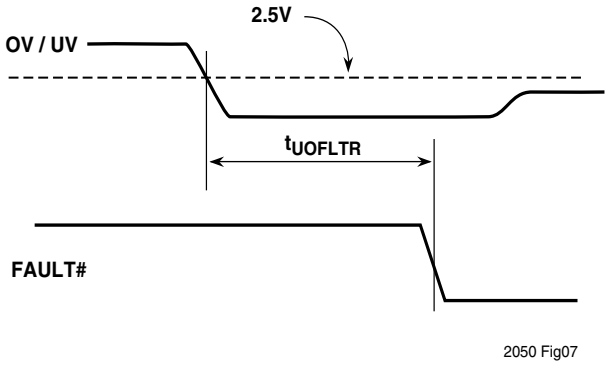


Figure 3. Under-/Over-Voltage Filter Timing

Under-/Over-Voltage Latching

An additional option for an out-of-tolerance condition on UV/OV is to latch the VGATE and PG[4:1]# outputs off such that a return to normal UV/OV operation does not turn them back on. In this case the FAULT# output is asserted.

Under-Voltage Hysteresis

The Under-Voltage comparator input may be configured with a programmable level of hysteresis using Register 7. The falling voltage compare level may be set in steps of 62.5mV below 2.5V. The rising voltage compare level is fixed at 2.5V. The default under-voltage hysteresis level is set to 62.5mV. In default conditions the SMH4804 is not in an under-voltage state once the UV voltage rises above 2.5V; and after that an under-voltage occurrence is not recognized until the UV voltage falls below 2.4375V (2.5V – 62.5mV).

Soft Start Slew Rate Control

Once all of the preconditions for powering up the DC/DC controllers have been met as explained in the previous sections, the SMH4804 provides a means to soft start the external power MOSFET. It is important to limit in-rush current to prevent damage to the add-in card or disruptions to the host power supply. For example, charging the filter capacitance too quickly (normally required at the input of the DC/DC controllers) may generate very high current. The VGATE output of the SMH4804 is current limited to I_{VGATE}, allowing the slew rate to be easily modified using external passive components. The slew rate may be found by dividing I_{VGATE} by the gate-to-drain capacitance placed on the external FET.

Load Control — Sequencing the Secondary Supplies

The PG1# through PG4# output pins are used to enable the external DC/DC controllers. Once the card is inserted, the SMH4804 samples the PD1# and PD2# pin detect input pins to determine if the card as been inserted properly. It then monitors the state of the UV and OV input pins to assure there is no under-voltage or over-voltage condition present. Once these conditions are met, and the EN/TS pin is greater than 2.5V, the SMH4804 asserts the VGATE output to turn on the external MOSFET.

During the time it takes to turn the MOSFET on, the SMH4804 monitors the system for an over-current condition via the CBSENSE input pin. In addition, the device internally monitors the voltage level on the VGATE output pin. This is shown by the ‘VGATE Sense’ block in Figure 2.

Once power has been ramped to the DC/DC controllers, two conditions must be met before the PG[4:1]# outputs can be enabled:

- the DRAIN SENSE input voltage must be below 2.5V.
- the VGATE voltage must be greater than $V_{DD} – V_{GT}$, where V_{GT} is the gate threshold.

The DRAIN SENSE input helps ensure that the power MOSFET is not absorbing too much steady state power from operating at a high V_{DS}. This sensor remains active at all times (except when current regulation is enabled). The

VGATE sensor makes sure that the power MOSFET is operating well into its saturation region before allowing the loads to be switched on. Once VGATE reaches $V_{DD} - V_{GT}$ this sensor is latched.

When the external MOSFET is properly switched on the PG[4:1]# outputs may be enabled. Output PG1# is activated first, followed by PG2# after a delay of t_{PGD}, PG3# after another t_{PGD} delay, and PG4# after a final t_{PGD} delay. The delays built into the SMH4804 allow timed sequencing of power to the loads. The delay times are programmable from 50µs to 160ms using bits 3:2 of Register 3 and bit 3 of Register 9. Refer to Register 3 - Address 0011 on page 32 and Register 9 - Address 1001 on page 38 for more information.

The ENPGA, ENPGB, and ENPGC input pins in Figure 5 are used to enabled the PG[4:1]# outputs. The ENPGA pin controls the PG[4:2]# outputs. If ENPGA is deasserted by external logic, the SMH4804 disables the PG[4:2]# outputs and they enter the high-impedance state. The ENPGA input must be asserted in order for PG[4:2]# to be driven by the SMH4804.

The ENPGB pin controls the PG[4:3]# outputs. If ENPGB is deasserted by external logic, the SMH4804 disables the PG[4:3]# outputs and they enter the high-impedance state. The ENPGB input must be asserted in order for PG[4:3]# to be driven by the SMH4804.

The ENPGC pin controls the PG[4]# output. If ENPGC is deasserted by external logic, the SMH4804 disables the PG[4]# outputs and the output enters the high-impedance state. The ENPGC input must be asserted in order for PG[4]# to be driven by the SMH4804.

This cascaded control mechanism is useful for enabling supplies that have dependencies based on the other voltages in the system.

The PG[4:1]# outputs have a 12V withstand capability, so high voltages must not be connected to these pins. Bipolar transistors or opto-isolators can be used to boost the withstand voltage to that of the host supply. Refer to Figure 18 for connectivity information.

Figure 5 shows the relationship between the PG[4:1]# and the ENPG[C:A] signals.

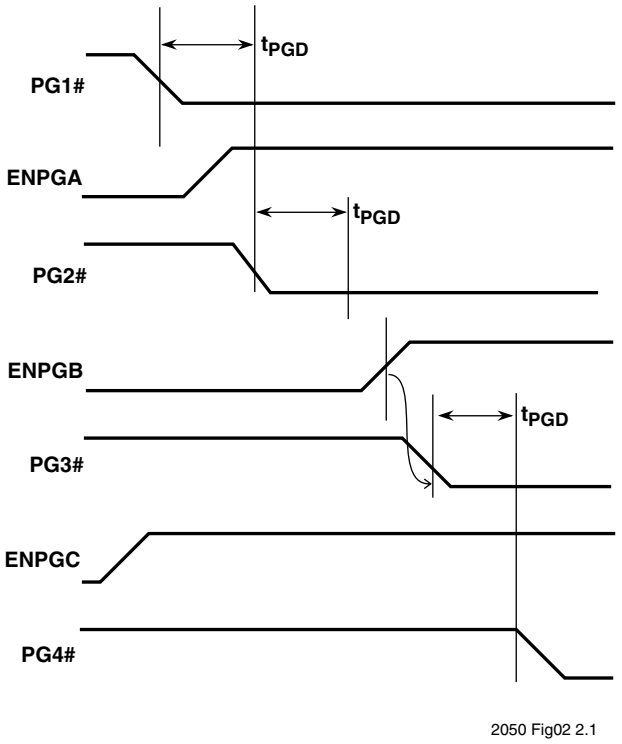


Figure 4. PG Output and ENPG Input Relationship

Forced Shutdown — Secondary Feedback

The Forced Shutdown signal (FS#) is an active low input that provides a method of receiving feedback from the secondary side of the DC/DC controllers. A built-in shutdown timer allows the SMH4804 to ignore the state of the FS# input until the timer period expires. The timer period is defined in bits 2:0 of Register 5. The FS# input must be driven high by the end of this timer period. A low level on this input causes a Fault condition, driving the FAULT# pin low and shutting off the VGATE and PG[4:1]# outputs.

The purpose of the shutdown timer is to allow enough time for devices on the secondary side of the DC/DC controllers to power up and stabilize. This feature allows supervisory circuits such as an SMS44 to control the shutdown of the primary side soft start circuit, even though the secondary side initially has no power.

Alternatively, the FS# input can be programmed to act as a fourth ENPG input controlling the PG1# output. This is combined with an option to independently enable PG1# with no affect on the other PG[4:2]# outputs, or it can be programmed so PG1# is the enabling output for the other outputs.

Circuit Breaker Operation

The SMH4804 provides a number of circuit breaker functions to protect against over-current conditions. A sustained over-current event could damage the host supply and/or the load circuitry. The board's load current passes through a series resistor (R_S) connected between the MOSFET source (which is tied to CBSENSE) and V_{SS}. The breaker trips whenever the voltage drop across R_S is greater than 50mV for more than t_{CBD} (a programmable filter delay ranging from 10µs to 500µs).

The circuit breaker cycle time is controlled via bit 0 of Register 4.

Figure 5 shows the circuit breaker duty cycle operation with RESET# high.

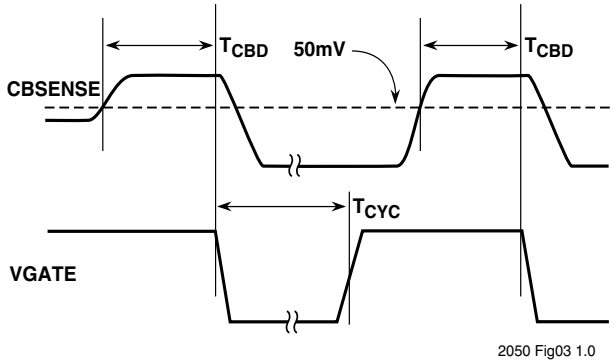


Figure 5. Circuit Breaker Duty Cycle Operation with RESET# High

Figure 6 shows the behavior of VGATE and CBSENSE immediately after RESET# is deasserted.

The circuit breaker cycle time can be programmed to a value of either 2.5 seconds of 5 seconds depending on the system configuration. Refer to bit 0 of Register 4 - Address 0100 on page 33 for more information on selecting the circuit breaker cycle time.

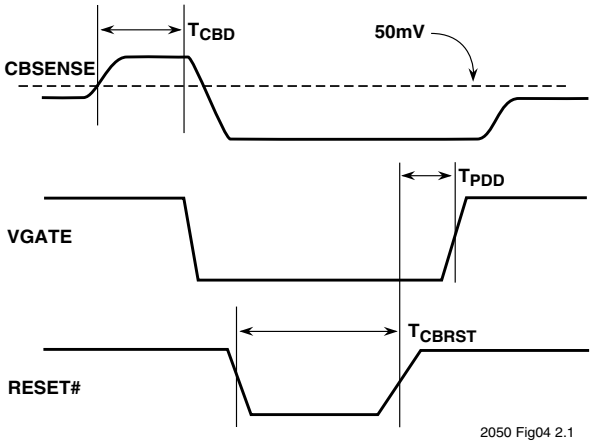


Figure 6. Circuit Breaker Reset with RESET# Low

Quick-Trip™ Circuit Breaker

The SMH4804 provides a Quick-Trip™ feature that causes the circuit breaker to trip immediately if the voltage drop across R_S exceeds V_{QCB}. The Quick-Trip level may be set to 60mV, 100mV (default), 200mV, or the feature may be disabled. Refer to bits 1:0 of Register 2 - Address 0010 on page 31 for more information.

Figure 7 shows the circuit breaker 'Quick Trip' response.In this figure, the voltage rises above V_{QCB}, causing VGATE to be deasserted.

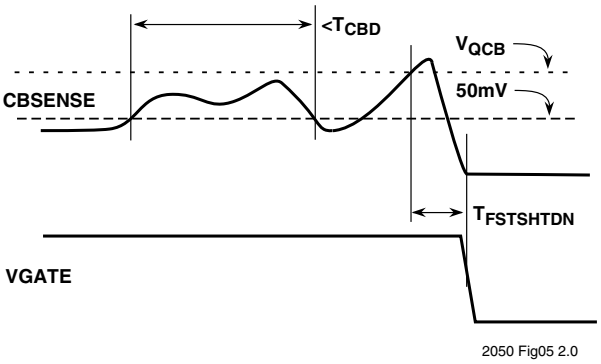


Figure 7. Circuit Breaker Quick Trip Response

Current Regulation

The current regulation mode is an optional feature that provides a means to regulate current through the MOSFET for a programmable period of time using bits 1:0 of Register 6.

Current regulation is generally enabled in applications that have switched dual (A and B) distributed power sources. By using the current regulation function, unwarranted shutdowns can be avoided if one of the dual supplies is switched in when it is at a more negative potential the currently operating supply.

When current regulation is selected by programming bits 1:0 of Register 6 to a binary value of 01 (5 ms), 10 (80 ms), or 11 (160 ms), it is enabled during a soft-start (power on period) and during normal operation after the PG[4:1]# outputs are enabled. If the voltage monitored at the CBSENSE pin is greater than 50mV, but less than 60mV, the SMH4804 reduces the VGATE voltage in order to maintain a CBSENSE potential less than 60mV, effectively regulating the current through the MOSFET.

Figure 8 and Figure 9 illustrate the current regulation function. The time period t_{PCR} — selectable at 5, 80, or 160 ms — is the maximum time during which regulation is enforced. If either V_{QCB} or t_{PCR} are exceeded the VGATE and PG[4:1]# outputs are immediately deasserted.

However, if CBSENSE drops below 50mV before the timer period ends, the timer is reset and VGATE resumes normal operation (see Current Regulation With Recovery on page 7). If the Quick-Trip level is exceeded, the device bypasses the current regulation timer and shuts down immediately. The current regulation feature is disabled in the default configuration.

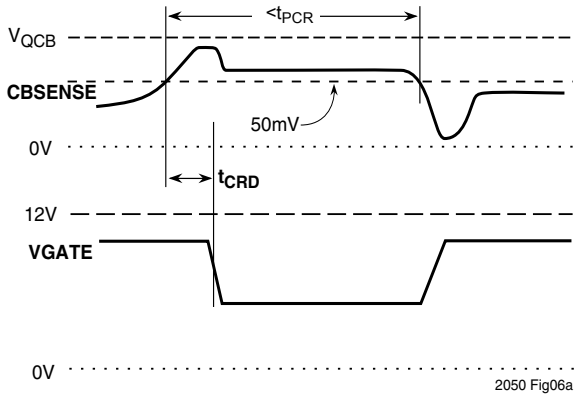


Figure 8. Current Regulation With Recovery

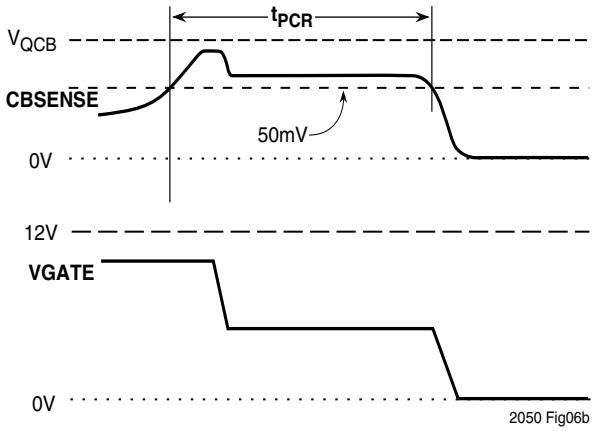


Figure 9. Current Regulation Without Recovery

Nonvolatile Fault Latch

The SMH4804 provides an optional nonvolatile fault latch (NVFL) circuit breaker feature. The nonvolatile fault latch essentially provides a programmable fuse on the circuit breaker. When the latch is enabled by setting bit 5 of Register 5, the nonvolatile fault latch is set whenever the circuit breaker trips. Once set, it cannot be reset by cycling power or through the use of the RESET# pin.

Note: The device remains disabled until Register C is reprogrammed. Refer to Register C - Address 1100 on page 38 for more information.

As long as the NVFL is set, the FAULT# output remains asserted. The Nonvolatile Fault Latch feature is disabled in the default configuration.

Resetting FAULT#

When the circuit breaker trips, the VGATE output is turned off and the SMH4804 drives FAULT# low. There are two methods to reset the circuit breaker which are selectable with the MODE pin:

- When the MODE is held high or left floating, the circuit breaker is in the duty-cycle mode. In this case the breaker resets automatically after a time of t_{CYC}.
- When the MODE pin is held low (or disabled in the Configuration Register) FAULT# can be reset by bringing RESET# low. The VGATE output attempts to restart the MOSFET slew control circuitry t_{PDD} after bringing RESET# back high again.

In either case, cycling power to the board resets the circuit breaker. If the over current condition still exists after the MOSFET switches back on, the circuit breaker will re-trip.

Serial Interface

The SMT4804 uses the industry standard I^2C, 2-wire serial data interface. This interface provides access to the configuration registers and the nonvolatile fault latch. The interface has three address inputs (A0 - A2) allowing up to eight devices on the same bus. This allows multiple devices on the same board or multiple boards in a system to be controlled with two signals; SDA and SCL.

Device configuration utilizing the Windows based SMT4804 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3200) is available from Summit to communicate with the SMT4804. The Dongle connects directly to the parallel port of a PC and programs the device through a cable using the I^2C bus protocol.

PACKAGE AND PIN CONFIGURATIONS

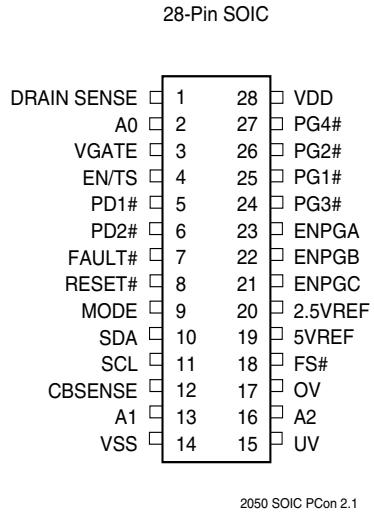


Figure 10. 28-Pin SOIC Package Pinout

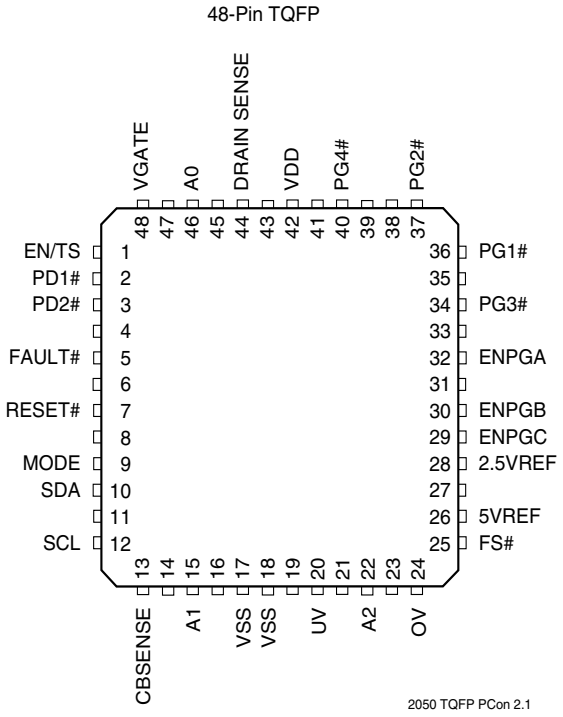


Figure 11. 48-Pin TQFP Package Pinout[1]

1. All unnamed pins on this package are no-connects.

PIN DESCRIPTIONS

Table 1 provides the type, name, and description of the SMH4804 pins. Pin numbers are provided for both the 28-pin SOIC and 48-pin TQFP packages.

Pin Number (28-Pin SOIC)	Pin Number (48-Pin TQFP)	Pin Type (I/O)	Pin Name	Description
1	44	I	DRAIN SENSE	The DRAIN SENSE input monitors the voltage at the drain of the external power MOSFET switch with respect to VSS. An internal 10µA source pulls the DRAIN SENSE signal towards the 5V reference level. DRAIN SENSE must be held below 2.5V to enable the PG[4:1] outputs.
2	46	I	A0	The A0 input works in conjunction with the A1 and A2 inputs. Together these inputs are used for decoding multiple devices on the serial bus. The A0 input has an internal 50KΩ pull-up to 5V.
3	48	O	VGATE	The VGATE output activates an external power MOSFET switch. This signal supplies a constant current output (100µA typical), which allows easy adjustment of the MOSFET to turn on slew rate.
4	1	I	EN/TS	The Enable/Temperature Sense input is the master enable input. If EN/TS is less than 2.5V, VGATE is disabled. This pin has an internal 200KΩ pull-up to 5V.
5	2	I	PD1#	The PD1# pin works in conjunction with the PD2# pin to optionally enable VGATE and the PG[4:1]outputs when they are at V_{SS}. This pin has an internal 50KΩ pull-up to 5V.
6	3	I	PD2#	The PD2# pin works in conjunction with the PD1# pin to optionally enable VGATE and the PG[4:1]# outputs when they are at V_{SS}. This pin has an internal 50KΩ pull-up to 5V.
7	5	O	FAULT#	FAULT# is an open-drain, active-low output that indicates the fault status of the device.
8	7	I	RESET#	The RESET# pin is used to clear latched fault conditions. When this pin is asserted, the VGATE and PG[4:1]# outputs are disabled. Refer to the section on Circuit Breaker Operation for more information. This pin has an internal 50KΩ pull-up to 5V.
9	9	I/O	SDA	SDA is the bidirectional serial data I/O port. This pin has an internal 50KΩ pull-up to 5V.

Table 1. SMH4804 Pin Descriptions

Pin Number (28-Pin SOIC)	Pin Number (48-Pin TQFP)	Pin Type (I/O)	Pin Name	Description
10	10	I	MODE	The state of the MODE signal determines how fault conditions are cleared. The device is in latched mode when this pin is low, and in cycle mode when the pin is high or floating.
11	12	I	SCL	SCL is the serial clock input. This pin has an internal 50KΩ pull-up to 5V.
12	13	I	CBSENSE	The circuit breaker sense input is used to detect over-current conditions across an external, low value sense resistor (R_S) tied in series with the Power MOSFET. A voltage drop of greater than 50mV across the resistor for longer than t_{CBD} trips the circuit breaker. A programmable Quick-Trip™ sense point is also available.
13	15	I	A1	The A1 input works in conjunction with the A0 and A2 inputs. Together these inputs are used for decoding multiple devices on the serial bus. The A1 input has an internal 50KΩ pull-up to 5V.
14	17	I	VSS	This is connected to the negative side of the supply.
15	20	I	UV	The UV pin is used as an under-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE is disabled if UV is less than 2.5V. Programmable internal hysteresis is available on the UV input, adjustable in increments of 62.5mV. Also available is a filter delay on the UV input.
16	22	I	A2	The A2 input works in conjunction with the A0 and A1 inputs. Together these inputs are used for decoding multiple devices on the serial bus. The A2 input has an internal 50KΩ pull-up to 5V.
17	24	I	OV	The OV pin is used as an over-voltage supply monitor, typically in conjunction with an external resistor ladder. VGATE is disabled if OV is greater than 2.5V. A filter delay is available on the OV input.
18	25	I	FS#	The Forced Shutdown (FS#) pin is an active low input that causes VGATE and the PG[4:1]# outputs to be shut down at any time after an internal shutdown timer has expired. The shutdown timer allows supervisory circuits on the secondary side (which are not powered up initially) to control shut down of the SMH4804 via an opto-isolator. This input has no pull-up resistor.
19	26	O	5VREF	This is a precision 5V output reference voltage that may be used to expand the logic input functions on the SMH4804. The output reference voltage is with respect to V_{SS}.

Table 1. SMH4804 Pin Descriptions (Continued)

Pin Number (28-Pin SOIC)	Pin Number (48-Pin TQFP)	Pin Type (I/O)	Pin Name	Description
20	28	O	2.5VREF	This is a precision 2.5V output reference voltage that may be used to expand the logic input functions on the SMH4804. The output reference voltage is with respect to V_{SS}.
21	29	I	ENPGC	The active-high ENPGC input controls the PG4# output. When ENPGC is low, the PG4# output is immediately placed in a high-impedance state. When ENPGC is high, or left floating, PG4# is driven low at a time period of t_{PGD} after PG3# is asserted. This pin has an internal 50kΩ pull-up to 5V.
22	30	I	ENPGB	The active-high ENPGB input controls the PG3# and PG4# outputs. When ENPGB is low, the PG3#, and PG4# outputs are immediately placed in a high-impedance state. When ENPGB is high, or left floating, PG3# is driven low at a time period of tPGD after PG2# is asserted. This pin has an internal 50kΩ pull-up to 5V.
23	32	I	ENPGA	The active-high ENPGA input controls the PG2#, PG3#, and PG4# outputs. When ENPGA is low, the PG2#, PG3#, and PG4# outputs are immediately placed in a high-impedance state. When ENPGA is high, or left floating, PG2# is driven low at a time period of tPGD after PG1# is asserted. This pin has an internal 50kΩ pull-up to 5V.
24	34	O	PG3#	The PG3# output is an open-drain, active low signal with no internal pull-up resistor. This pin can be used to switch a load or enable a DC/DC converter. PG1# is enabled immediately after VGATE reaches V_{DD} - V_{GT} and the DRAIN SENSE voltage is less than 2.5V. Each successive PGn# output (PG2# → PG3# → PG4#) is enabled t_{PGD} after its predecessor, provided that the ENPGx inputs are high. The voltage on this pin cannot exceed 12V relative to V_{SS}. ENPGx refers to the ENPGA, ENPGB, and ENPGC inputs.
25	36	O	PG1#	The PG1# output is an open-drain, active low signal with no internal pull-up resistor. This pin can be used to switch a load or enable a DC/DC converter. PG1# is enabled immediately after VGATE reaches V_{DD} - V_{GT} and the DRAIN SENSE voltage is less than 2.5V. Each successive PGn# output (PG2# → PG3# → PG4#) is enabled t_{PGD} after its predecessor, provided that the ENPGx inputs are high. The voltage on this pin cannot exceed 12V relative to V_{SS}. ENPGx refers to the ENPGA, ENPGB, and ENPGC inputs.

Table 1. SMH4804 Pin Descriptions (Continued)

Pin Number (28-Pin SOIC)	Pin Number (48-Pin TQFP)	Pin Type (I/O)	Pin Name	Description
26	37	O	PG2#	The PG2# output is an open-drain, active low signal with no internal pull-up resistor. This pin can be used to switch a load or enable a DC/DC converter. PG1# is enabled immediately after VGATE reaches V_{DD} - V_{GT} and the DRAIN SENSE voltage is less than 2.5V. Each successive PGn# output (PG2# → PG3# → PG4#) is enabled t_{PGD} after its predecessor, provided that the ENPGx inputs are high. The voltage on this pin cannot exceed 12V relative to V_{SS}. ENPGx refers to the ENPGA, ENPGB, and ENPGC inputs.
27	40	O	PG4#	The PG4# output is an open-drain, active low signal with no internal pull-up resistor. This pin can be used to switch a load or enable a DC/DC converter. PG1# is enabled immediately after VGATE reaches V_{DD} - V_{GT} and the DRAIN SENSE voltage is less than 2.5V. Each successive PGn# output (PG2# → PG3# → PG4#) is enabled t_{PGD} after its predecessor, provided that the ENPGx inputs are high. The voltage on this pin cannot exceed 12V relative to V_{SS}. ENPGx refers to the ENPGA, ENPGB, and ENPGC inputs.
28	42	I	VDD	This is the positive supply input. An internal shunt regulator limits the voltage on this pin to approximately 12V with respect to V_{SS}. A resistor must be placed in series with the V_{DD} pin to limit the regulator current (R_D in the application illustrations).

Table 1. SMH4804 Pin Descriptions (Continued)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... –55°C to 125°C

Power Supply Current (I_{DD}) ..... 15 mA

Storage Temperature ..... –65°C to 150°C

Lead Solder Temperature (10 seconds) ..... 300 °C

Terminal Voltage with Respect to V_{SS}:

VGATE ..... VDD + 0.3V

A0, A1, A2, MODE, RESET, ENPGA, ENPGB, ENPGC, FS#, SDA, and SCL..... -0.3 to +7V

PD1#, PD2#, VDD, UV, OV, CBSENSE, DRAIN SENSE, EN/TS, FAULT#, PG1#, PG2#, PG3#, and PG4# ..... -0.3 to +15V

Open Drain Output Short Circuit Current..... 100 mA

Junction Temperature ..... 150^{o} C

ESD Rating per JEDEC 2000V

Latch-Up testing per JEDEC..... ± 100mA

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature Range (Ambient) ..... -40^{o} C to +85^{o} C

Supply Voltage(V_{DD}) (I_{DD} = 5 mA)..... 11V to 13V

Package Thermal Resistance (θ_{JA}) 28-pin SOIC ... 79^{o}C/W

Package Thermal Resistance (θ_{JA}) 48-pin TQFP... 80^{o}C/W

Moisture Classification Level 3 (MSL 3) per J-STD-020

Reliability Characteristics

Data Retention..... 100 Years

Endurance[1] ..... 100,000 Cycles

1. Guaranteed by Design

DC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise notes. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Supply voltage	IDD = 3 mA	11	12	13	V
$5V_{REF}$	5V reference output voltage	IDD = 3 mA	4.8	5.00	5.25	V
I_{LOAD5}	5V reference output current	IDD = 3 mA	-1		1	mA
$2.5V_{REF}$	2.5V reference output voltage	IDD = 3 mA	2.45	2.50	2.55	V
$I_{LOAD2.5}$	2.5V reference output current	IDD = 3 mA	-0.5		0.5	mA
I_{DD}[1]	Power supply current		2		13	mA
V_{UV}	Under-voltage threshold	IDD = 3 mA	2.45	2.50	2.55	V
V_{UVHYST}	Under-voltage hysteresis	IDD = 3 mA		63[2]		mV
V_{OV}	Over-voltage threshold	IDD = 3 mA	2.45	2.50	2.55	V
V_{OVHYST}	Over-voltage hysteresis	IDD = 3 mA		10		mV
V_{GATE}	VGATE output voltage	I_{GATE} = 80 µA	V_{DD} - V_{GT}		V_{DD}	V
I_{GATE}	VGATE output current	V_{GATE} = 5 V	80	85	90	µA
V_{SENSE}	DRAIN SENSE threshold	V_{SENSE} = V_{SS}	2.45	2.50	2.55	V
I_{SENSE}	DRAIN SENSE current output	I_{DD} = 3 mA	9	10	11	µA
V_{CB}	Circuit breaker threshold	I_{DD} = 3 mA	45	50	55	mV
V_{QCB}	Programmable Quick Trip circuit breaker threshold voltage	QT = 200 mV	180	200	220	mV
		QT = 100 mV	90	100	110	mV
		QT = 60 mV	54	60	66	mV
V_{ENTS}	EN/TS threshold voltage	I_{DD} = 3 mA	2.40	2.45	2.50	V
$V_{ENTSHYST}$	EN/TS threshold hysteresis voltage	I_{DD} = 3 mA		10		mV
V_{IH}	Input voltages: ENPGA/B/C, MODE, RESET#, PD1#, PD2#		3		$5V_{REF}$	V
V_{IL}			-0.1		2	V
V_{OL}	Output low voltage: FAULT#	I_{OL} = 3 mA	0		0.4	V
	Output low voltage: PG1#/2#/3#/4#	I_{OL} = 3 mA	0		0.4	V
I_{IL}	Input current: PD1#, PD2#, EN/TS	V_{IL} = V_{SS}		100		µA
V_{GT}	Gate threshold		0.7	1.8	3.0	V

1. This value is set by the R_D resistor.
2. See Table 8 for a listing of programmable under-voltage hysteresis settings.

AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise notes. All voltages are relative to GND.)

Symbol	Description	Conditions	Min	Typ	Max	Unit	Comment
t_{CBD}	Programmable Over-Current Filter	t_{CBD} = 5 µs	-25	t_{CBD}	+25	µs	See Figure 5, Figure 6, Figure 7, and Figure 13
		t_{CBD} = 50 µs[1]				µs	
		t_{CBD} = 150 µs				µs	
		t_{CBD} = 400 µs				µs	
t_{PGD}	Programmable power good delay (PG1 → PG2, PG2 → PG3, PG3 → PG4)	t_{PGD} = 50 µs	-25	t_{PGD}	+25	%	See Figure 4
		t_{PGD} = 250 µs				%	
		t_{PGD} = 500 µs				%	
		t_{PGD} = 1000 µs				%	
		t_{PGD} = 5 ms[1]				%	
		t_{PGD} = 20 ms				%	
		t_{PGD} = 80 ms				%	
		t_{PGD} = 160 ms				%	
t_{QTSD}	Quick-Trip shutdown			200		ns	See Figure 7
t_{CYC}	Circuit breaker cycle mode cycle time	t_{CYC} = 2.5 s[1]	-25	t_{CYC}	+25	%	See Figure 5
		t_{CYC} = 5 s					
t_{CBRST}	CB_{RESET} pulse width		200			ns	See Figure 6
t_{PUVF}	Programmable under-voltage filter	t_{PUVF} = Off[1]	-25	t_{PUVF}	+25	%	
		t_{PUVF} = 5 ms					
		t_{PUVF} = 80 ms					
		t_{PUVF} = 160 ms					
t_{PDD}	Programmable pin detect	t_{PDD} = 0.5 ms	-25	t_{PDD}	+25	%	See Figure 6 and Figure 13
		t_{PDD} = 5 ms					
		t_{PDD} = 80 ms[1]					
		t_{PDD} = 160 ms					

1. Indicates default value

I²C 2-WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS

(Over recommended operating conditions, unless otherwise notes. All voltages are relative to GND.)

Symbol	Parameter	Conditions	Min	Max	Units
f_{SCL}	SCL clock frequency		0	100	kHz
t_{LOW}	Clock period low		4.7		µs
t_{HIGH}	Clock period high		4.0		µs
t_{BUF}	Bus free time[1]	Before new transmission	4.7		µs
$t_{SU:STA}$	Start condition setup time		4.7		µs
$t_{HD:STA}$	Start condition hold time		4.0		µs
$t_{SU:STO}$	Stop condition setup time		4.7		µs
t_{AA}	Clock edge to valid output	SCL low to valid SDA (cycle n)	0.2	3.5	µs
t_{DH}	Data out hold time	SCL low (cycle n+1) to SDA change	0.2		µs
t_R	SCL and SDA rise time[1]			1000	ns
t_F	SCL and SDA fall time[1]			300	ns
$t_{SU:DAT}$	Data in setup time		250		ns
$t_{HD:DAT}$	Data in hold time		0		ns
t_I	Noise filter SCL and SDA[1]	Noise suppression		100	ns
t_{WR}	Write cycle time			5	ms

1. Values are guaranteed by the design.

TIMING DIAGRAM

Figure 12 shows a timing diagram for the Bus Interface Memory timing. The table above lists the AC timing parameters for Figure 12. One bit of data is transferred during each clock pulse. Note that data must remain stable when the clock is high.

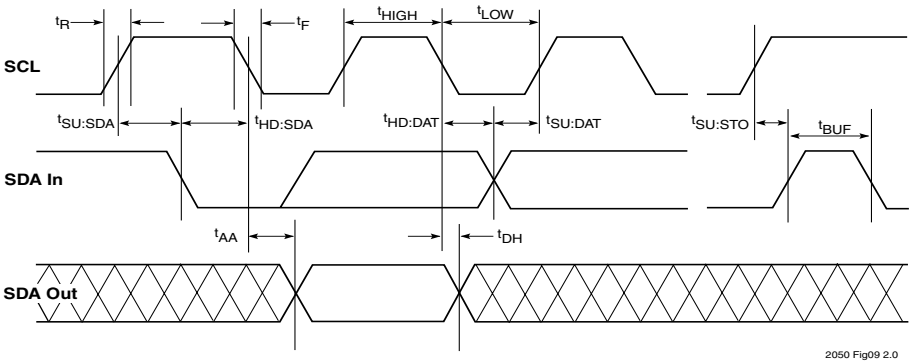


Figure 12. Bus Interface Memory Timing

Power-on Timing

Figure 13 illustrates some power on sequences, including the UV and OV differentials to their reference, and Power Good cascading. Refer to the table on page 17 for more information on the t_{PDD} and t_{CBD} timings.

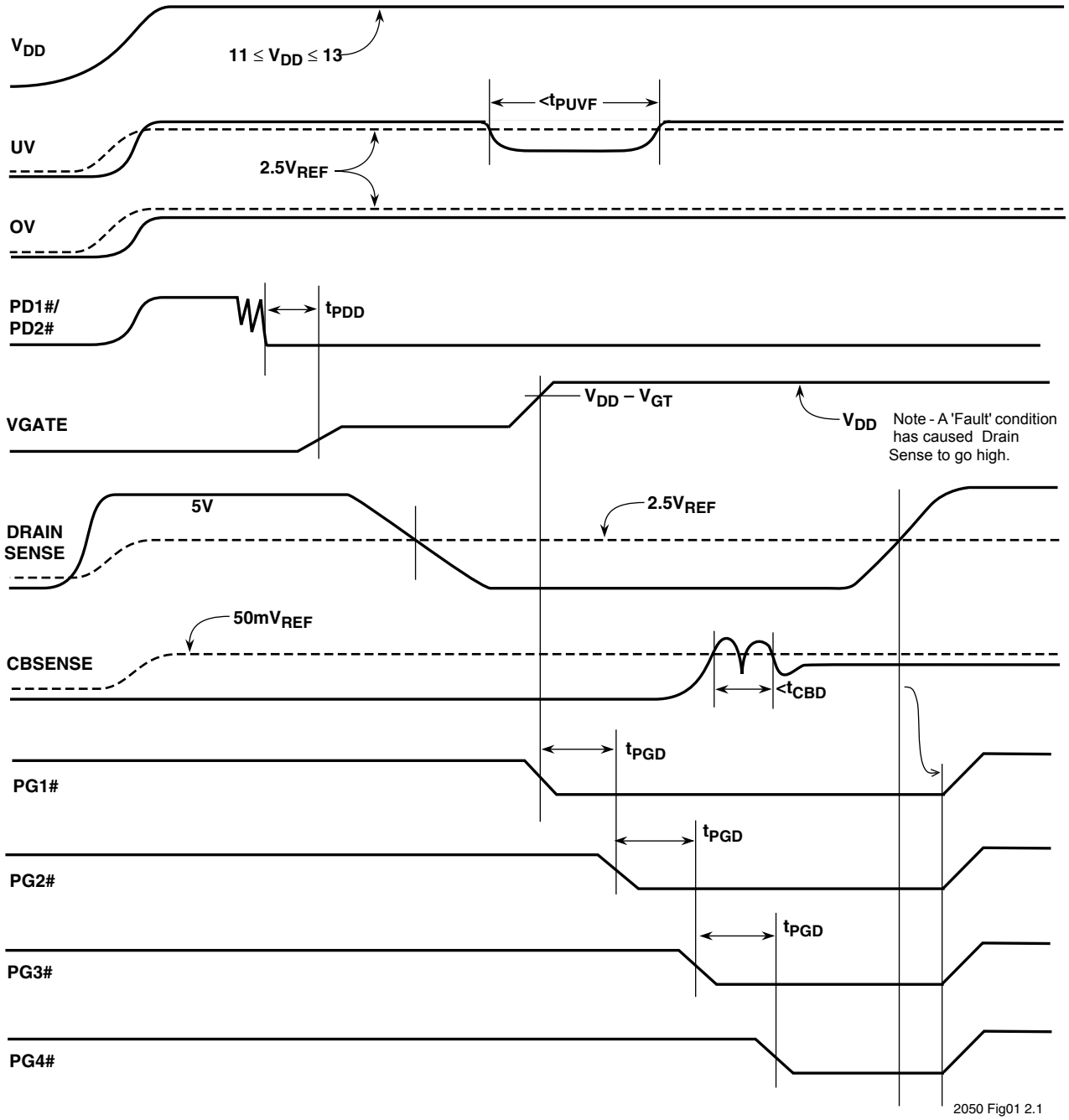
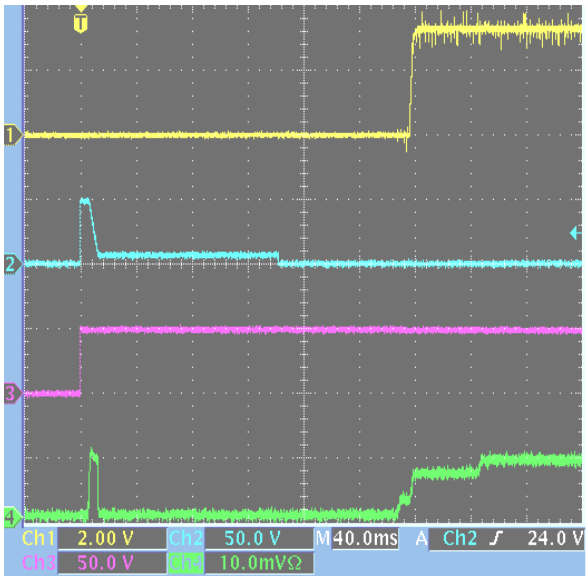


Figure 13. SMH4804 Power-On Sequences



SMH4804 Power-On Waveforms - Ref to -48V

Tektronix TDS3054: Time/Horizontal division = 40mS

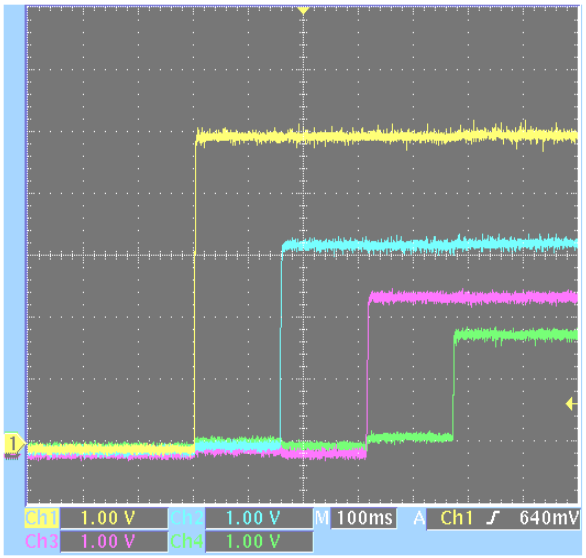
Ch 1 (2V/Div) = 3.3V DC-DC converter output (Yellow trace)

Ch 2 (50V/Div) = PG#2 output (Blue trace) - Note 1

Ch 3 (50V/Div) = Switched 48V supply voltage (Purple trace)

Ch 4 (2A/Div) = Inrush input current (Green)

Note 1 – After initial hot swap conditions are met, he PG# outputs first drop to –43V until ready to sequence the DC-DC converter. When ready to sequence, the PG# outputs then drop an additional 5V to enable the converters.



SMH4804 Sequencing waveforms - Ref to GND

Four DC/DC converters sequenced on at 160ms intervals

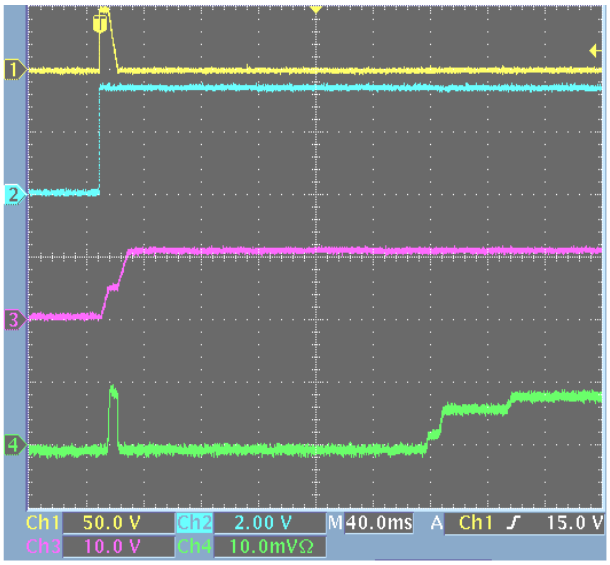
Tektronix TDS3054: Time/Horizontal division = 100mS

Ch 1 (1V/Div) = 5.0V DC-DC converter output (Yellow trace)

Ch 2 (1V/Div) = 3.3V DC-DC converter output (Yellow trace)

Ch 3 (1V/Div) = 2.5V DC-DC converter output (Yellow trace)

Ch 4 (1V/Div) = 1.8V DC-DC converter output (Yellow trace)



SMH4804 with 0.1uF and 0.01uF Soft-Start Capacitors

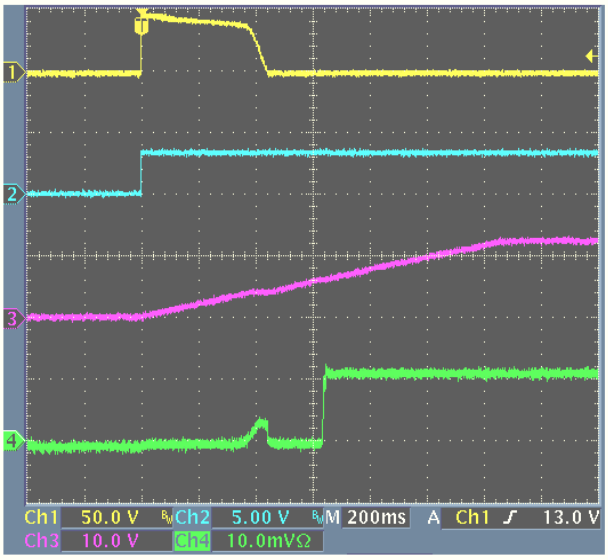
Tektronix TDS3054: Time/Horizontal division = 40mS

Ch 1 (50V/Div) = MOSFET Drain (Yellow trace)

Ch 2 (5V/Div) = SMH4804 UV pin (Blue trace)

Ch 3 (10V/Div) = MOSFET Gate (Purple trace)

Ch 4 (2A/Div) = -48V Inrush input current (Green)



SMH4804 with 1uF and 0.1uF Soft-Start Capacitors

Tektronix TDS3054: Time/Horizontal division = 200mS

Ch 1 (50V/Div) = MOSFET Drain (Yellow trace)

Ch 2 (5V/Div) = SMH4804 UV pin (Blue trace)

Ch 3 (10V/Div) = MOSFET Gate (Purple trace)

Ch 4 (2A/Div) = -48V Inrush input current (Green)

Operating at High Voltages

The breakdown voltage of the external active and passive components limits the maximum operating voltage of the SMH4804 hot-swap controller. Components that must be able to withstand the full supply voltage are: the input and output decoupling capacitors, the protection diode in series with the DRAIN SENSE pin, the power MOSFET switch and the capacitor connected between its drain and gate, the high-voltage transistors connected to the power good outputs, and the dropper resistor connected to the controller's V_{DD} pin.

Over-Voltage and Under-Voltage Resistors

In Figures 21, 22, and 23, the three resistors (R1, R2, and R3) connected to the OV and UV inputs must be capable of withstanding the maximum supply voltage of several hundred volts. The trip voltage of the UV and OV inputs is 2.5V relative to V_{SS}. As the input impedance of UV and OV is very high, large value resistors can be used in the resistive divider. The divider resistors should be high stability, 1% metal-film resistors to keep the under-voltage and over-voltage trip points accurate.

Telecom Design Example

A hot-swap telecom application may use a 48V power supply with a –25% to +50% tolerance (i.e., the 48V supply can vary from 36V to 72V). The formula for calculating R1, R2, and R3 are as follows.

First, a peak current, ID_{MAX}, must be specified for the resistive network. The value of the current is arbitrary, but it cannot be too high (self-heating in R3 becomes a problem), or too low (the value of R3 becomes very large, and leakage currents can reduce the accuracy of the OV and UV trip points). The value of IDMAX should be ≥200µA for the best accuracy at the OV and UV trip points. A value of 250µA for IDMAX is used to illustrate the following calculations.

With V_{OV} (2.5V) being the over-voltage trip point, R1 is calculated by the formula:

$$R1 = \frac{V_{OV}}{ID_{MAX}}$$

Substituting:

$$R1 = \frac{2.5V}{250\mu A} = 10\ K\Omega$$

Next the minimum current that flows through the resistive divider, ID_{MIN}, is calculated from the ratio of minimum and maximum supply voltage levels:

$$ID_{MIN} = \frac{ID_{MAX} \times VS_{MIN}}{VS_{MAX}}$$

Substituting:

$$ID_{MIN} = \frac{250\mu A \times 36V}{2.5\ V} = 125\ \mu A$$

Now the value of R3 is calculated from ID_{MIN}:

$$R3 = \frac{VS_{MIN} \times V_{UV}}{ID_{MIN}}$$

V_{UV} is the under-voltage trip point, also 2.5V. Substituting:

$$R3 = \frac{36V \times 2.5V}{125\ \mu A} = 286\ k\Omega$$

The closest standard 1% resistor value is 267 kΩ

Then R2 is calculated:

$$(R1 + R2) = \frac{V_{UV}}{ID_{MIN}}$$

or

$$R2 = \frac{V_{UV}}{ID_{MIN}} - R1$$

Substituting:

$$R2 = \frac{2.5V}{125\ \mu A} - 10\ k\Omega = 20\ k\Omega - 10\ k\Omega = 10\ k\Omega$$

An Excel spread sheet is available on Summit's website (***www.summitmicro.com)*** to simplify the resistor value calculations and tolerance analysis for R1, R2, and R3.

Dropper Resistor Selection

The SMH4804 is powered from the high-voltage supply via a dropper resistor, R_D. The dropper resistor must provide the SMH4804 (and its loads) with sufficient operating current under minimum supply voltage conditions, but must

not allow the maximum supply current to be exceeded under maximum supply voltage conditions.

The dropper resistor value is calculated from:

$$R_D = \frac{VS_{MIN} - VDD_{MAX}}{I_{DD} - I_{LOAD}}$$

where VS_{MIN} is the lowest operating supply voltage, V_{DDMAX} is the upper limit of the SMH4804 supply voltage, I_{DD} is minimum current required for the SMH4804 to operate, and I_{LOAD} is any additional load current from the 2.5V and 5V outputs and between V_{DD} and V_{SS}.

Calculate the minimum wattage required for RD from:

$$P_{R0} \geq \frac{(VS_{MAX} - VDD_{MIN})^2}{R_D}$$

where V_{DDMIN} is the lower limit of the SMH4804 supply voltage, and VS_{MAX} is the highest operating supply voltage.

In circumstances where the input voltage may swing over a wide range (*e.g., from 20V to 100V)* the maximum current may be exceeded. In these circumstances it may be necessary to add an 11V Zener diode between V_{DD} and V_{SS} to handle the wide current range. The Zener voltage should be below the nominal regulation voltage of the SMH4803A so that it becomes the primary regulator.

MOSFET V_{DS}(ON) Threshold

The drain sense input on the SMH4804 monitors the voltage at the drain of the external power MOSFET switch with respect to V_{SS}. When the MOSFET's V_{DS} is below the user-defined threshold the MOSFET switch is considered to be ON. The $V_{DS}(ON)_{THRESHOLD}$ is adjusted using the resistor, R_T, in series with the drain sense protection diode. This protection, or blocking, diode prevents high voltage breakdown of the drain sense input when the MOSFET switch is OFF. A low leakage MMBD1401 diode offers protection up to 100V. For high voltage applications (up to 500V) the Central Semiconductor CMR1F-10M diode should be used. The $V_{DS}(ON)_{THRESHOLD}$ is calculated from:

$$V_{DS}(ON)_{THRESHOLD} = V_{SENSE} - (I_{SENSE} \times R_{T)} - V_{DIODE}$$

where VDIODE is the forward voltage drop of the protection diode. The $V_{DS}(ON)_{THRESHOLD}$ varies over temperature due to the temperature dependence of V_{DIODE} and I_{SENSE}. The calculation below gives the $V_{DS}(ON)_{THRESHOLD}$ under the worst case condition of 85°C ambient. Using a 68 kΩ resistor for R_T gives:

$$V_{DS}(ON)_{THRESHOLD} = 2.5V - (15\mu A \times 68k\Omega) - 0.5V = 1V$$

The voltage drop across the MOSFET switch and sense resistor, V_{DSS}, is calculated from:

$$V_{DSS} = I_D (R_S \times R_{ON})$$

where I_D is the MOSFET drain current, RS is the circuit breaker sense resistor and R_{ON} is the MOSFET on resistance.

The dropper resistor value should be chosen such that the minimum and maximum I_{DD} and V_{DD} specifications of the SMH4804 are maintained across the host supply's valid operating voltage range. First, subtract the minimum V_{DD} of the SMH4804 from the low end of the voltage, and divide by the minimum I_{DD} value. Using this value of resistance as R_D find the operating current that would result from running at the high end of the supply voltage to verify that the resulting current is less than the maximum I_{DD} current allowed. If some range of supply voltage is chosen that would cause the maximum I_{DD} specification to be violated, then an external zener diode with a breakdown voltage of ~12V should be used across V_{DD}.

As an example of choosing the proper R_D value, assume the host supply voltage ranges from 36 to 72V. The largest dropper resistor that can be used is: (36V-11V)/3mA = 8.3kΩ. Next, confirm that this value of R_D also works at the high end: (72V-13V)/8.3kΩ = 7.08mA, which is less than 8mA.

The FS# input can also be used in conjunction with a secondary-side supervisory circuit providing a positive feedback loop during the power up sequence. As an example, assume the SMH4804 is configured to turn on –48V to three DC/DC converters and then sequentially turn on the converters with a 1.6ms delay. Further assume all of the enable inputs are true and PG4# has just been sequenced on. If FS# option 4 (100_{BIN} in register 5) has been selected, then FS# must be driven high within 1.6ms after PG4# goes low, otherwise all of the PG[4:1]# outputs are disabled.

Ideally, there would be a secondary-side supervisor similar to the SMS44 that would have its reset time-out period programmed to be less than 1.6ms. After the last supply turns on the RESET# output of the SMS44 would be released and FS# pulled high. However, if for any reason

not all of the supplies turn on, RESET# is not released and the SMH4804 disables the PG[4:1]# outputs. This termination timer function can be programmed to abort the sequence after PG1#, PG2#, PG3# or PG4#.

Soft Start Slew Rate Control

The –48V turn on time is controlled by the SMH4804 and by the values of R4, C1 and C2 in Figures 21, 22, and 23. The turn on time is approximately 10ms with the component values shown in Figure 15. Increasing the capacitance reduces the output slew rate and increases the turn on time. The capacitors prevent the MOSFET from turning on simultaneously with the application of –48V. Resistor R4 is specified to limit the current into and the rate of charge of C1. The ratio of C1 to C2 (10:1) limits the MOSFET's V_{GS} to approximately 5V once the –48V supply is connected and C1 is fully charged.

Configuring the SMH4804 for Independent Control of DC-DC Converters for Power-on-LAN IEEE 802.3

Certain systems employing live card insertion or 'hot-swapping' require independent control of the individual secondary-side voltages. The SMH4804 Quad Hot Swap Controller is easily configured for independent on/off control of up to 4 individual DC-DC converters. A simplified schematic displaying the SMH4804 enable pins together with their respective output enabling pins is shown in Figure 14.

The SMH4804 asserts each of its output enabling pins (PG[4:1]#) independently of one another as shown in Figure 14. Applying a logic high (3.5V - 5V) to any of the 'ENABLE_PGx#' nodes forces the corresponding output to a logic low.

For example, to turn on the first DC-DC converter (assuming its Enable pin requires a low to turn it on), 'ENABLE_PG1#' must be high. Taking this node low forces the SMH4804 output to a high impedance (open-drain) state. Please refer to Application Brief AB-01 for more details.

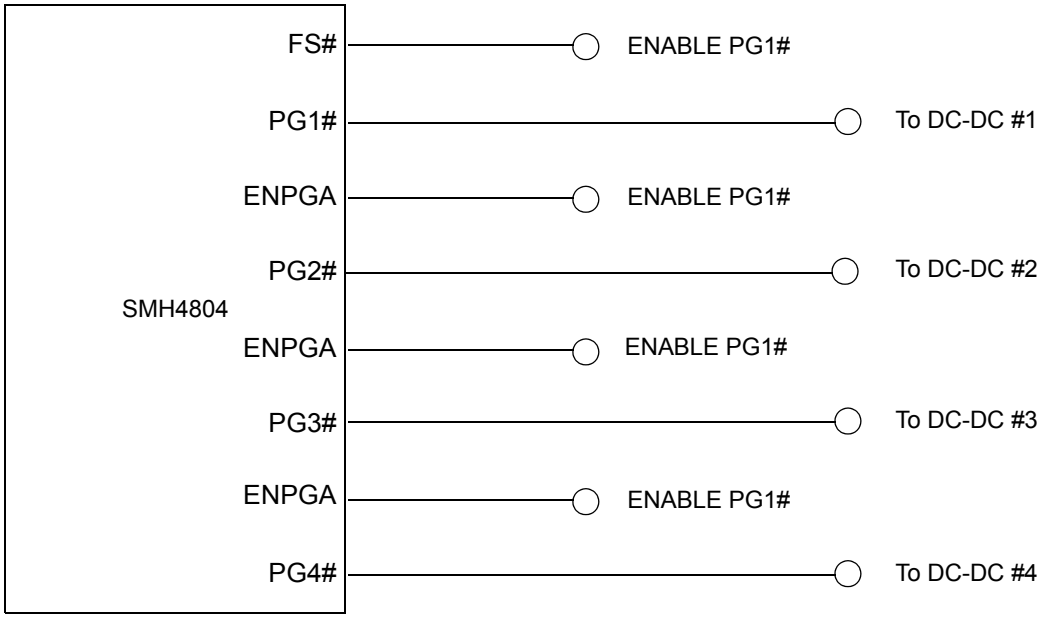


Figure 14. Configuring the SMH4804 as a Quad Independent Hot-Swap Controller.

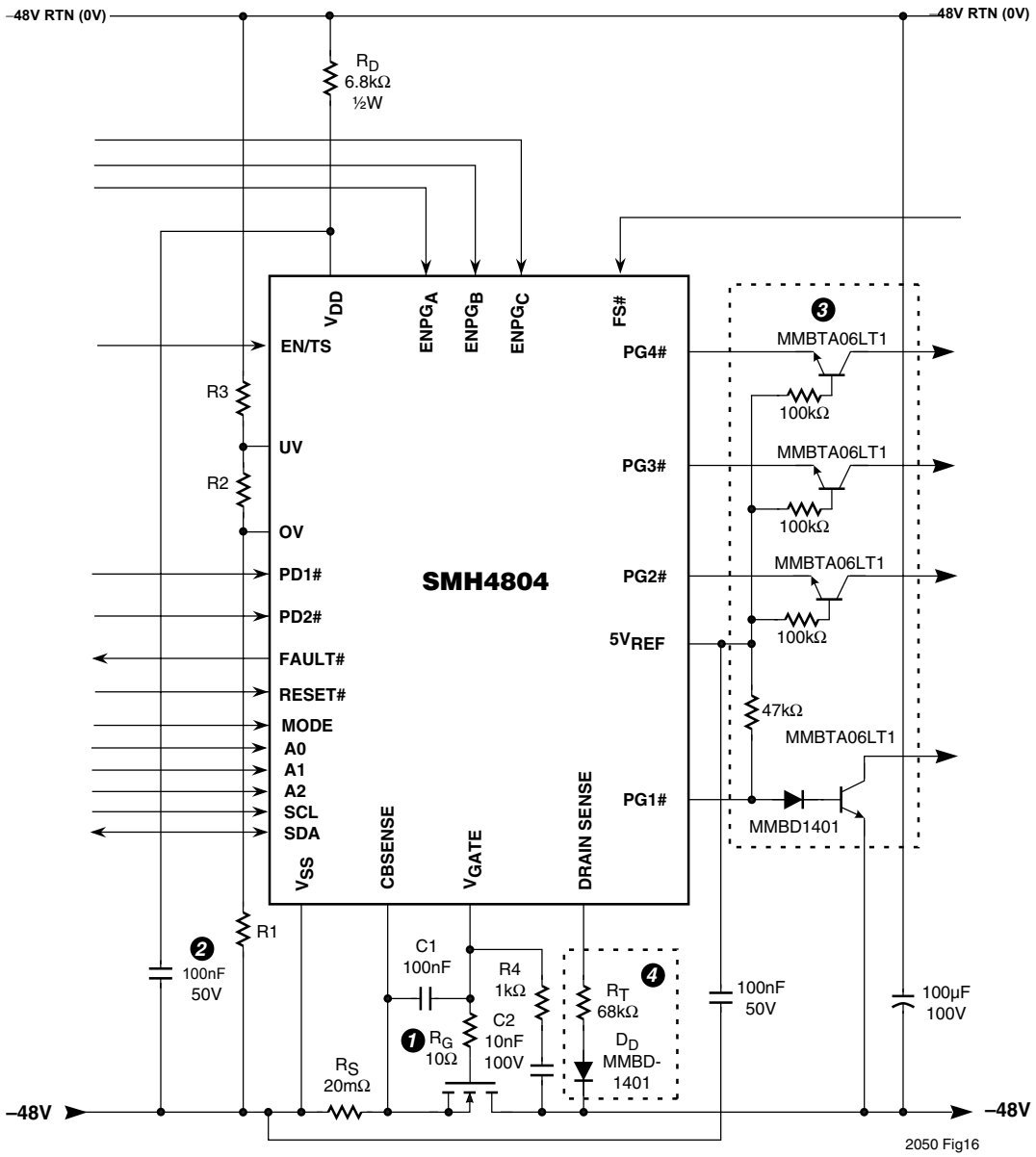


Figure 15. Changing Polarity of Power Good Output PG1#

Notes:

❶ The 10Ω resistor (R_G) must be located as close as possible to the MOSFET.

❷ Optional bypass capacitor. If a larger value is required an 11V zener must be connected in parallel.

❸ Optional interface circuit. The PG[4:1]# outputs can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG[4:1]# outputs doesn't exceed 15V.

❹ The DRAIN Sense function may cause nuisance tripping due to voltage transients on the –48V line or when using multiple lines. This may be avoided by one of the following methods:

A. Disable the function by connecting the DRAIN Sense pin to V_{SS} directly. The components R_T and D_D are eliminated.

B. Add a capacitor from DRAIN Sense to V_{SS}. The exact capacitance value depends upon the magnitude and duration of the voltage transient appearing at the drain of the MOSFET.

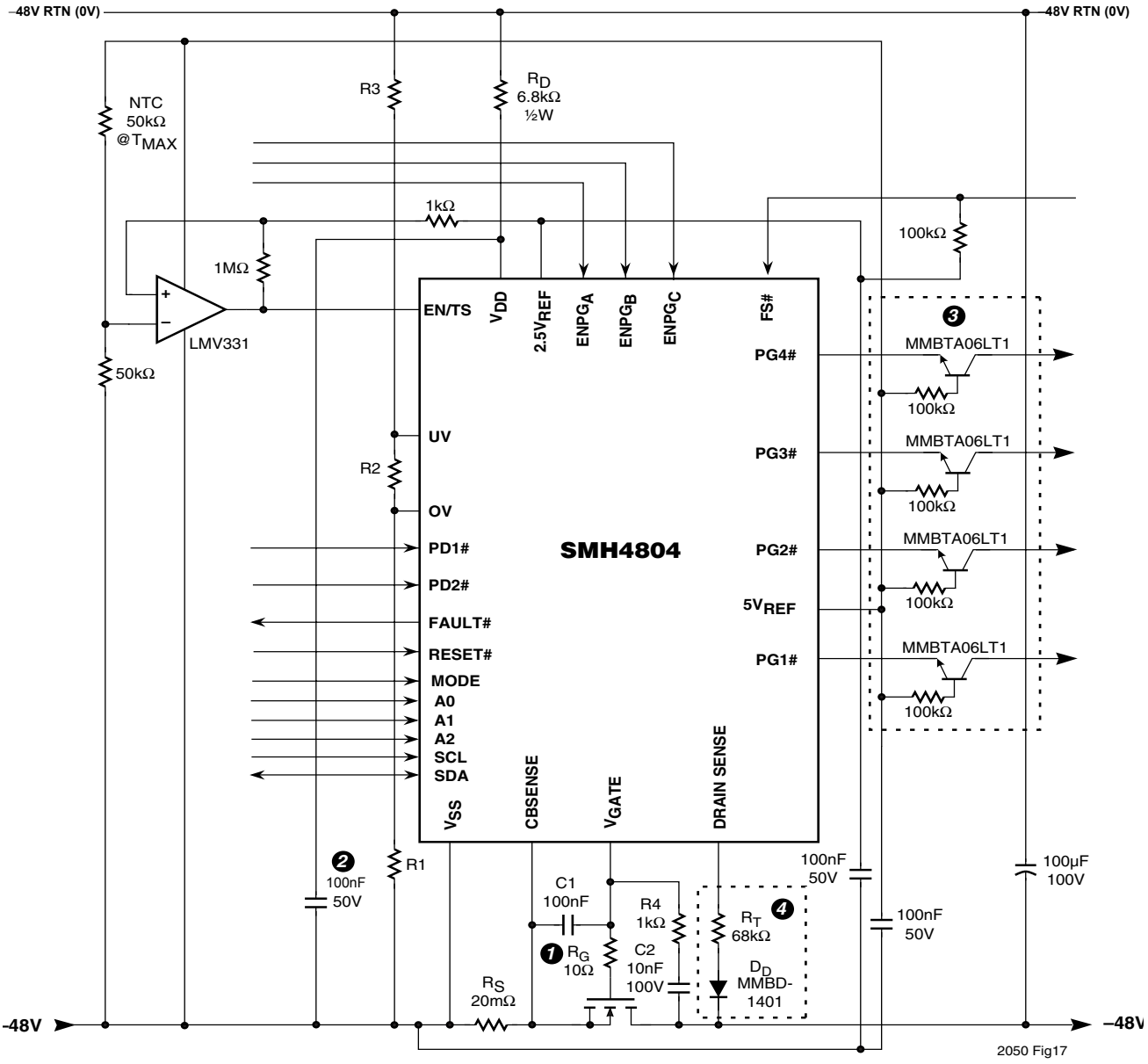


Figure 16. Over-temperature Shutdown

Notes:

❶ The 10Ω resistor (R_G) must be located as close as possible to the MOSFET.

❷ Optional bypass capacitor. If a larger value is required an 11V Zener must be connected in parallel.

❸ Optional interface circuit. The PG[4:1]# outputs can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG[4:1]# outputs doesn't exceed 15V.

❹ The DRAIN Sense function may cause nuisance tripping due to voltage transients on the –48V line or when using multiple lines. This may be avoided by one of the following methods:

A. Disable the function by connecting the DRAIN Sense pin to V_{SS} directly. The components RT and DD are eliminated.

B. Add a capacitor from Drain Sense to V_{SS}. The exact capacitance value depends upon the magnitude and duration of the voltage transient appearing at the drain of the MOSFET.

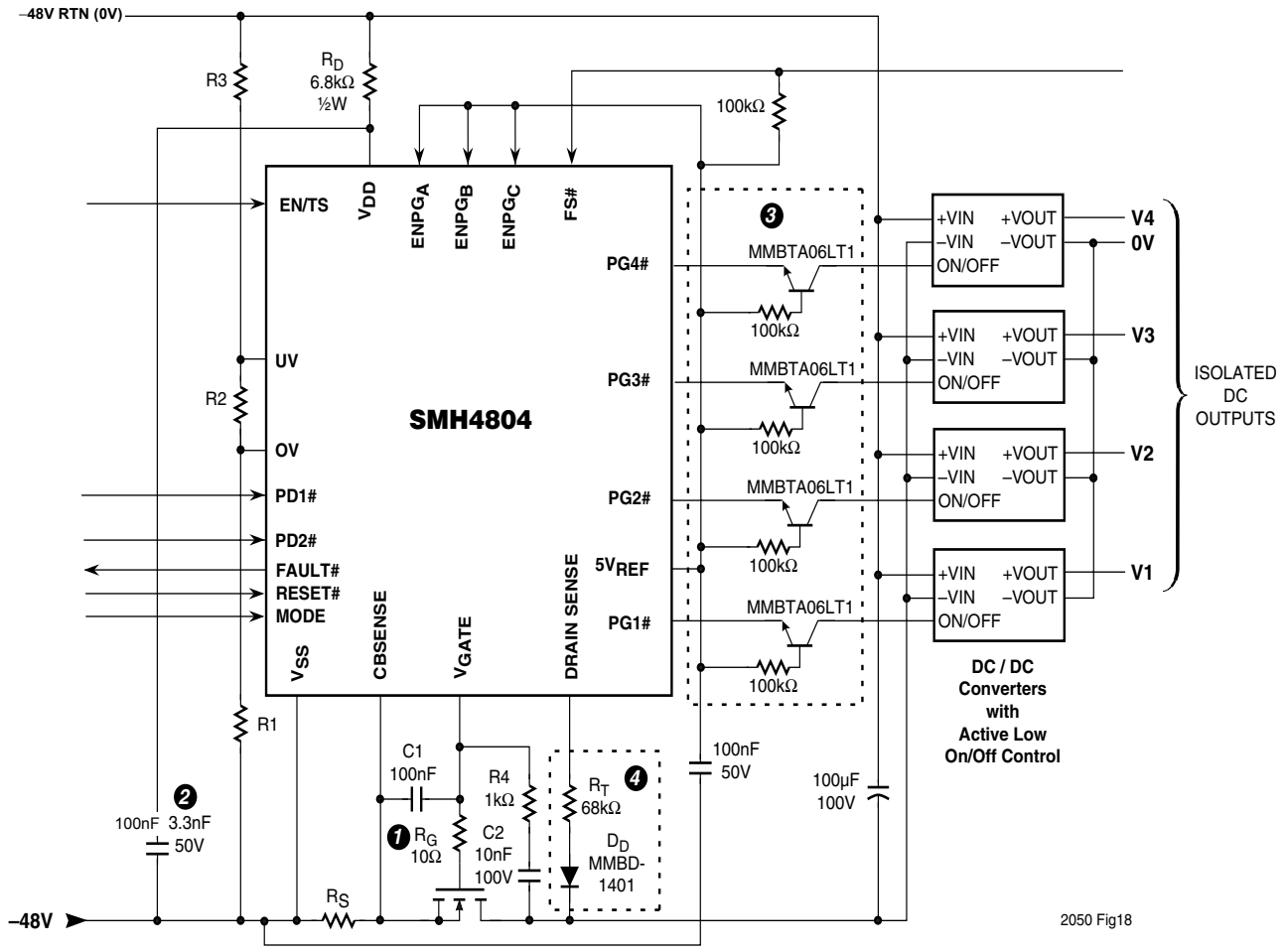


Figure 17. Typical Application Sequencing Four DC/DC Converter

Notes:

❶ The 10Ω resistor (R_G) must be located as close as possible to the MOSFET.

❷ Optional bypass capacitor. If a larger value is required an 11V Zener must be connected in parallel.

❸ Optional interface circuit. The PG[4:1]# outputs can be directly connected to the power module if the input voltage to the module is within tolerance and the voltage on the PG[4:1]# outputs doesn't exceed 15V.

❹ The DRAIN Sense function may cause nuisance tripping due to voltage transients on the –48V line or when using multiple lines. This may be avoided by one of the following methods:

A. Disable the function by connecting the DRAIN Sense pin to V_{SS} directly. The components R_T and D_D are eliminated.

B. Add a capacitor from DRAIN Sense to V_{SS}. The exact capacitance value depends upon the magnitude and duration of the voltage transient appearing at the drain of the MOSFET.

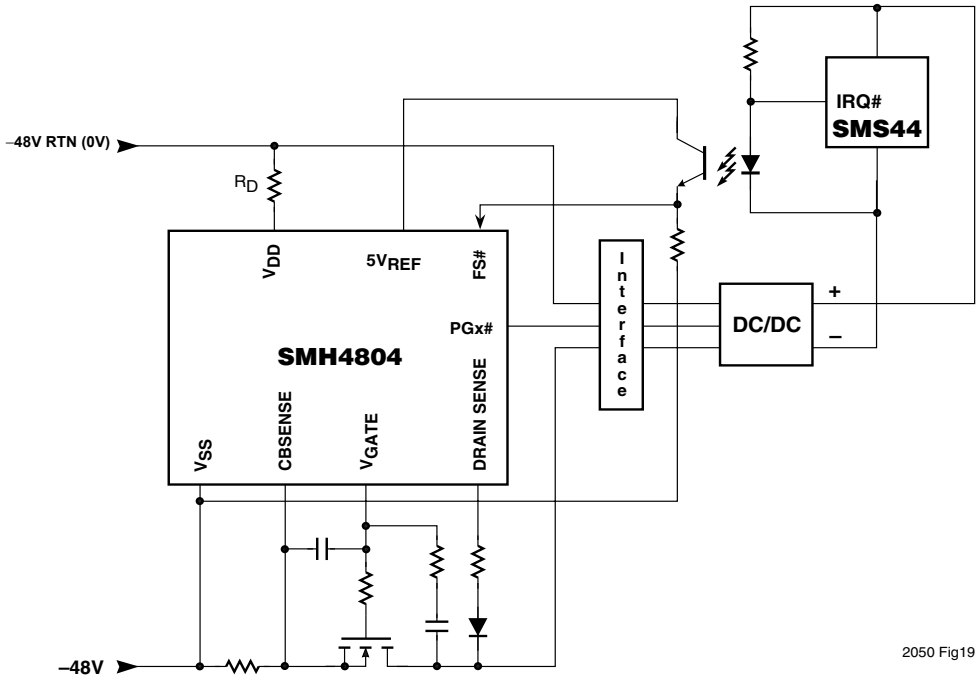


Figure 18. Controlling FS# with Secondary Feedback

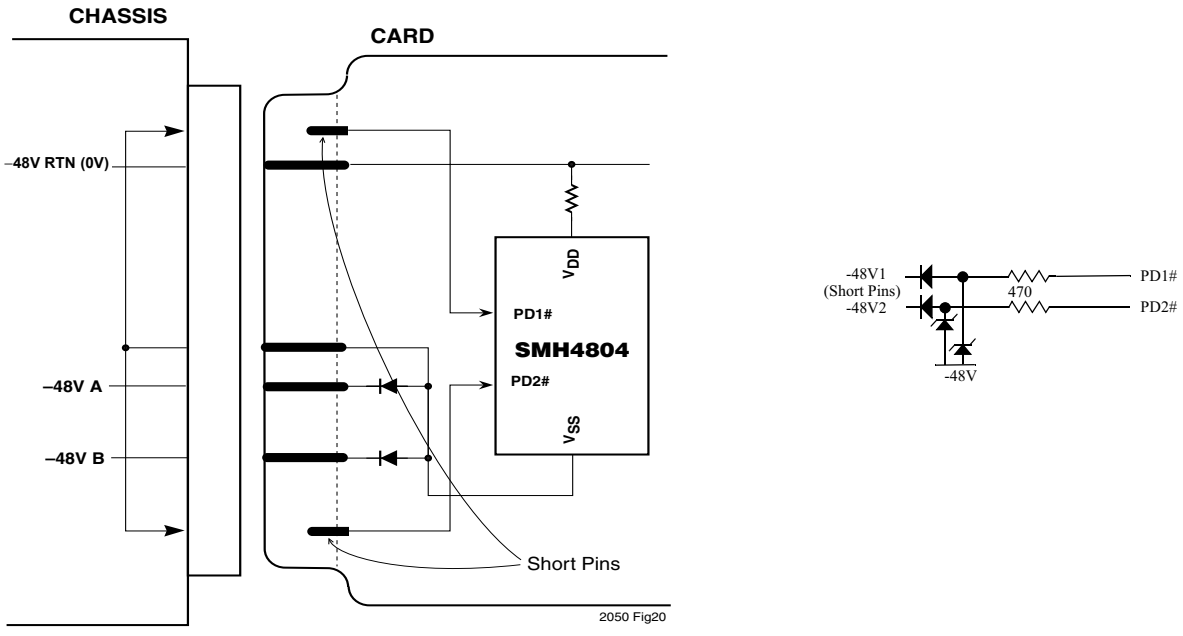


Figure 19. PD1# and PD2# Inputs, Physical Offset

PROGRAMMING INFORMATION

I²CBus Interface

The I²C bus is a two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA) and a serial clock line (SCL). The SMH4804 supports a 100 kHz clock rate.

The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. The SMH4804 contains a Schmitt input on both the SDA and SCL signals.

Start and Stop Conditions

Both the SDA and SCL pins remain high when the bus is not busy. Data transfers between devices may be initiated with a Start condition only when SCL and SDA are high. A high-to-low transition of the SDA while the SCL pin is high is defined as a Start condition. A low-to-high transition SDA while SCL is high is defined as a Stop condition. Figure 20 shows a timing diagram of the start and stop conditions.

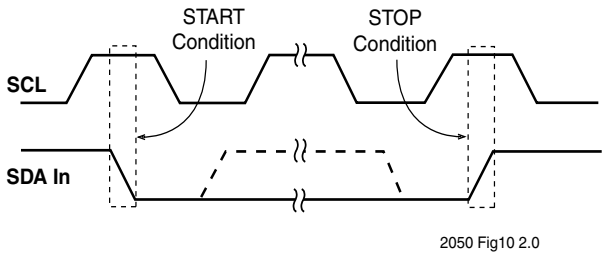


Figure 20. Start and Stop Conditions

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter, and any device that receives data as a receiver. The device controlling data transmission is called the Master, and the controlled device is called the Slave. In all cases the SMH4804 is referred to as a Slave device since it never initiates any data transfers.

Acknowledge

Data is always transferred in bytes. Acknowledge (ACK) is used to indicate a successful data transfer. The transmitting device releases the bus after transmitting eight bits. During the ninth clock cycle the Receiver pulls the SDA line low to acknowledge that it received the eight bits of data. This is shown by the ACK callout in Figure 21.

When the last byte has been transferred to the Master during a read of the SMH4804, the Master leaves SDA high for a Not Acknowledge (NACK) cycle. This causes the SMH4804 part to stop sending data, and the Master issues a Stop on the clock pulse following the NACK.

Figure 21 shows the Acknowledge timing.

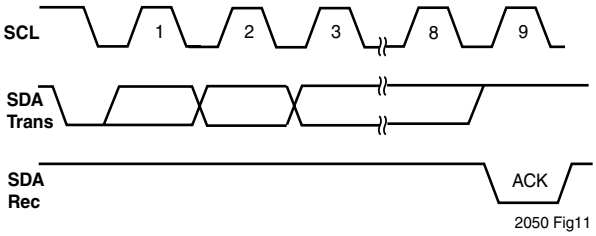


Figure 21. Acknowledge Timing

Read and Write

The first byte from a Master is always made up of a 7-bit Slave address and the Read/Write (R/W) bit. The R/W bit tells the Slave whether the Master is reading data from the bus or writing data to the bus (1 = Read, 0 = Write). The first four of the seven address bits are called the Device Type Identifier (DTI). The DTI for the SMH4804 is 1010_{BIN}. The next three bits are Address values for A2, A1, and A0 (if multiple devices are used). The SMH4804 issues an Acknowledge after recognizing a Start condition and its DTI. Figure 22 shows an example of a typical master address byte transmission.

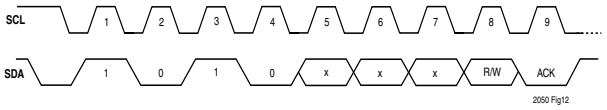


Figure 22. Typical Master Address Byte Transmission

During a read by the Master device, the SMH4804 transmits eight bits of data, then releases the SDA line, and monitors the line for an Acknowledge signal. If an Acknowledge is detected, and no Stop condition is generated by the Master, the SMH4804 continues to transmit data. If an Acknowledge is not detected (NACK), the SMH4804 terminates any subsequent data transmission. The read transfer protocol on SDA is shown in Figure 23.

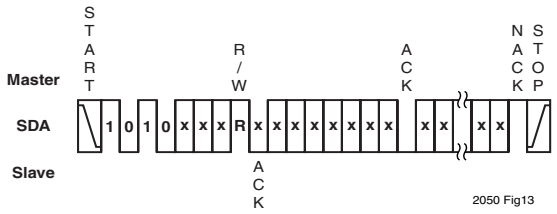


Figure 23. Read Protocol

During a Master write, the SMH4804 receives eight bits of data, then generates an Acknowledge signal. It device continues to generate the ACK condition on SDA until a Stop condition is generated by the Master. The write transfer protocol on SDA is shown in Figure 24.

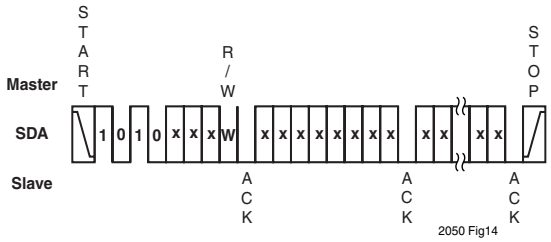


Figure 24. Write Protocol

Random Access Read

Random address read operations allow the Master to access any memory location in a random fashion. This operation involves a two-step process. First, the Master issues a Write command which includes the Start condition and the Slave address field (with the R/W bit set to Write) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMH4804 to the desired address.

After the word address Acknowledge is received by the Master, it immediately reissues a Start condition followed by another Slave address field with the R/W bit set to Read. The SMH4804 responds with an Acknowledge and then transmits the 8 data bits stored at the addressed location. At this point, the Master sets the SDA line to NACK and generates a Stop condition. The SMH4804 discontinues data transmission and reverts to its standby power mode.

Sequential Reads

Sequential reads can be initiated as either a current address read or a random access read. The first word is transmitted as with the other byte Read modes (current address byte Read or random address byte Read). However, the Master now responds with an Acknowledge, indicating that it requires additional data from the SMH4804.

The SMH4804 continues to output data for each Acknowledge received. The Master sets the SDA line to NACK and generates a Stop condition. During a sequential Read operation the internal address counter is automatically incremented with each Acknowledge signal.

For Read operations all address bits are incremented, allowing the entire array to be read using a single Read command. After a count of the last memory address the address counter rolls over and the memory continues to output data.

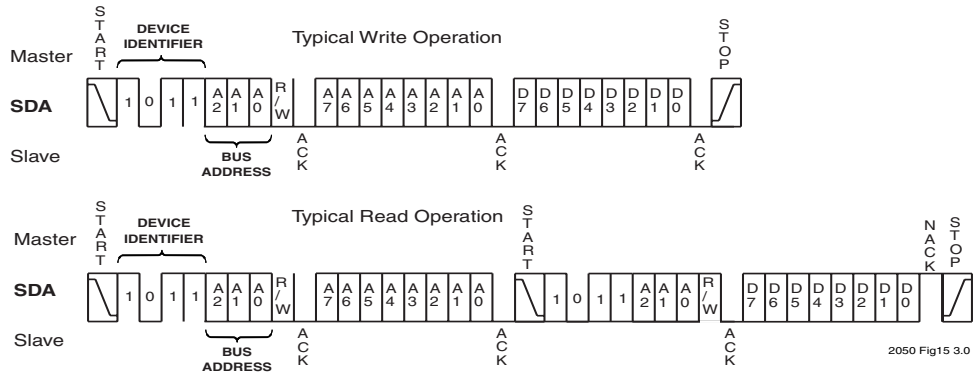


Figure 25. Sequential Bus Cycles

Register Access

The SMH4804 contains a 2-wire bus interface for register access as explained in the previous section. This bus is highly configurable, while maintaining the industry standard protocol. The SMH4804 responds to one of two selectable Device Type Addresses: $1010_{BIN,}$ generally assigned to NV-memories, or 1011_{BIN}, which is the default address for the SMH4804. The Device Type Address is assigned by programming bit 3 of Register 8.

Register accesses are also programmable using bits 2:1 of Register 8. Accesses can be denied (no reads or writes), read only, or read/write (default state).

The SMH4804 has three address pins, A[2:0], associated with the 2-wire bus. The SMH4804 can be configured to respond to:

- only to the proper serial data string of the Device Type Address and specific bus addresses (Register 8, bit 0 set).
- the Device Type Address and any bus address (Register 8, bit 0 cleared).

Development Hardware and Software

The end user can use the Summit SMX3200 programming cable and software to connect the board containing the SMH4804 to the personal computer. See Figure 26 for board connections. The programming cable interfaces directly between a PC's parallel port and the and the 10-pin connector shown in Figure 26. The application's values are entered via an intuitive graphical user interface employing drop-down menus.

After the desired settings for the application are determined the software generates a hex file that can be written to the SMH4804. This file contains the customer part number and is used to customize the devices during the final electrical test operations.

Figure 26 shows a diagram of the SMH4804 programming connections.

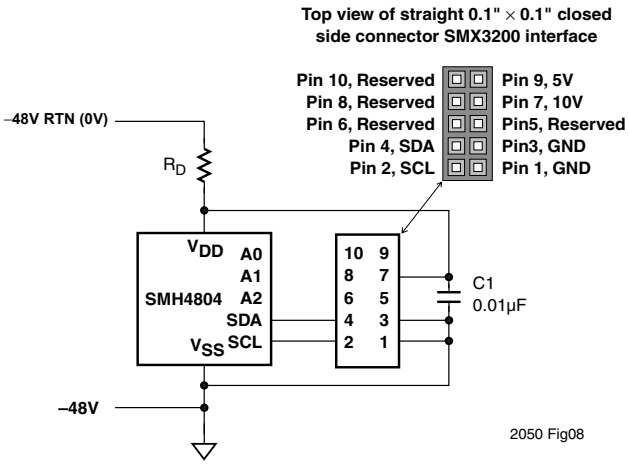


Figure 26. SMH4804 Programming Connection

Caution: Damage may occur when connecting the dongle to a system utilizing an earth-connected positive terminal.

Master/Slave Protocol

The master/slave protocol defines any device that sends data onto the bus as a transmitter and any device that receives data as a receiver. The device controlling data transmission is called the Master and the controlled device is called the Slave. The SMH4804 is always a Slave device, since it never initiates any data transfers. One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock high time, because a change on the data line while SCL is high is interpreted as either a Start or a Stop condition.

Register Bit Maps

The SMH4804 has eight user programmable, nonvolatile, configuration registers. Although 8-bit data transfers are used for reading and writing the registers, only the 4 lease significant bits of each register are utilized by the device. Therefore, in each of the following registers, bits 7:4 are left blank. Bits 3:0 are used as shown for each register.

DEFAULT CONFIGURATION REGISTER SETTINGS — SMH4804F-019

Register	Hex Contents	Description
R02	9	Over-current delay and Quick-Trip over-current reference level.
R03	2	Power-good sequencing delay, CB mode enable, and PD[2:1]# pin-detect enable.
R04	8	PG[4:1]# Power-good sequence enable, over/under voltage filter delay, circuit breaker cycle time.
R05	C	Non-volatile fault latch enable, FS# forced shutdown function control.
R06	C	Under-voltage filter enable, over-voltage filter enable, VGATE current regulation control.
R07	9	Under-voltage hysteresis control.
R08	1	I2C control, including device type address, configuration register R/W status, and slave address response control.
R09	9	Power-good sequence speed, PD[2:1]# pin detect delay time.
R0C	0	Non-volatile fault latch. Set by hardware when a fault is detected.

Table 2. SMH4804 Default Register Settings

REGISTERS

Register 2 - Address 0010

This register is used to select both the over-current delay and the quick trip threshold for the electronic circuit breaker.

Bits				Default	R/W	Description
3	2	1	0			
0	0			0b10	R/W	Set Over-current delay to 400 µs.
0	1				R/W	Set Over-current delay to 150 µs.
1	0				R/W	Set Over-current delay to 50 µs.
1	1				R/W	Set Over-current delay to 5 µs.
		0	0	0b01	R/W	Set Quick Trip reference voltage to 200 mV.
		0	1		R/W	Set Quick Trip reference voltage to 100 mV.
		1	0		R/W	Set Quick Trip reference voltage to 60 mV.
		1	1		R/W	Set Quick Trip reference voltage off.

Table 3. Register 2 Bitmap

Register 3 - Address 0011

This register is used to control the sequencing delays from PG1# to PG2#, PG2# to PG3#, and PG3# to PG4#. The SMH4804 provides two levels of sequencing delay: fast and slow, which is selected by programming bit 3 of Register 9. These two bits are effectively concatenated with R9 bit 3, providing 8 programmable delay periods. Refer to Register 9 for more information.

NOTE - Bit 1 controls the effect of the MODE pin. When set (high) the pin functions as described in the pin descriptions. If the bit is cleared (low) the state of the pin is ignored and the circuit breaker enters latch mode.

Bit 0 enables or disables the function of the PD[4:1]# inputs.

Bits				Default	R/W	Description
3	2	1	0			
Register 9, bit 3 = 0						
0	0			0b00	R/W	PG[4:1]# Sequencing delay: 1500 µs.
0	1					PG[4:1]# Sequencing delay: 50 µs.
1	0					PG[4:1]# Sequencing delay: 250 µs.
1	1					PG[4:1]# Sequencing delay: 500 µs.
Register 9, bit 3 = 1						
0	0			0b00	R/W	PG[4:1]# Sequencing delay: 5 ms.
0	1					PG[4:1]# Sequencing delay: 20 ms.
1	0					PG[4:1]# Sequencing delay: 80 ms.
1	1					PG[4:1]# Sequencing delay: 160 ms.
Register 9, bit 3 = 1 or 0						
		0		0b1	R/W	When bit 1 is cleared (0), the CB MODE MODE is disabled (see NOTE above).
		1				When bit 1 is set (1), the CB MODE is enabled (see NOTE above).
			0	0b0		When bit 0 is cleared, the PD1# and PD2# signals are disabled.
			1			When bit 0 is set, the PD1# and PD2# signals are enabled.

Table 4. Register 3 Bitmap

Register 4 - Address 0100

Register 4 enables PG[4:1]# signal sequencing, sets the O/U voltage filter timing, and selects the circuit breaker cycle time.

Bit 3 of this register enables or disables the PG[4:1]# sequence delays. When set, the delays are defined in registers 3 and 9. If bit 3 is cleared, no delay is incurred and sequencing is based solely on the state of the ENPGA#, ENPGB#, and ENPGC# inputs. If the ENPGx# inputs are tied high, the PG[4:1]# outputs turn on simultaneously.

Bits				Default	R/W	Description
3	2	1	0			
0				0b1	R/W	When bit 3 is cleared, PG[4:1]# signal sequencing is simultaneous.
1						When bit 3 is set, PG[4:1]# signal sequencing is enabled.
	0	0		0b00	R/W	When bits 2:1 are set to 0b00, the over/under voltage filter is off.
	0	1				When bits 2:1 are set to 0b01, the over/under voltage delay is 5 ms.
	1	0				When bits 2:1 are set to 0b10, the over/under voltage delay is 80 ms.
	1	1				When bits 2:1 are set to 0b11, the over/under voltage delay is 160 ms.
			0	0b0	R/W	When bit 0 is cleared, the circuit breaker cycle time is 2.5 sec.
			1			When bit 0 is set, the circuit breaker cycle time is 5 sec.

Table 5. Register 4 Bitmap

Register 5 - Address 0101

Register 5 controls the function of the nonvolatile fault latch and provides general control for the FS# input. Bit 3 controls the enabling of the non-volatile latch. Bits 2:0 configure the FS# input.

The FS# pin has two basic functions: it can be programmed to act as an auxiliary enable input controlling the PG1# output, or it can be programmed to be an event monitor during the power-up sequence.

These bits also control the interrelationship of the PG[4:1]# outputs. In a cascade operating mode PG1# must be true before PG2# can be true, etc. This interrelationship can be disabled so that each PG[4:1]# output is effectively controlled by its corresponding ENGPx# input, as long as the primary supply, VGATE and DRAIN SENSE pins are within their operating limits.

When programmed as an enable to PG1# there are two options: 010_{BIN} disables the cascade mode (the PG[4:1]# outputs can act independently) and FS# effectively becomes the enable input for PG1#; 011_{BIN} enables the cascade mode and makes FS# the enable input for PG1#. In this mode, PG1# must be active before PG2# can be activated, followed by PG3#, then PG4#.

The event monitor mode is generally implemented in conjunction with a monitoring device on the secondary side of the DC/DC converters, such as the SMS44, SMT4004 or SMS64. If FS# is not pulled high before the programmed condition then the PG[4:1]# and VGATE outputs are shut down. As an example, if the binary value is 111_{BIN}, VGATE and PG1# are shut down if FS# is not pulled high before t_{PGD} has elapsed after PG1# is true. None of the other PG[4:1]# outputs are activated. If a failure occurs due to the lapse of the event monitor timer, cycling the power resets the device.

Bits				Default	R/W	Description
3	2	1	0			
0				0b1	R/W	When bit 3 is cleared, the non-volatile latch is enabled.
1						When bit 3 is set, the non-volatile latch is disabled.
	0	0	0	0b100	R/W	When bits 2:0 are 0b000, the FS function: PG4 + t_{PGD} cascade is disabled for simultaneous assertion of the PG[4:1]# pins.
	0	0	1			When bits 2:0 are 0b001, the FS function is disabled (=1).
	0	1	0			When bits 2:0 are 0b010, the FS function is active (=1) before PG1 enabled. Cascade disabled for simultaneous assertion of the PG[4:1]# pins.
	0	1	1			When bits 2:0 are 0b011, the FS function must be high (de-asserted) before PG1 is enabled.
	1	0	0			FS function: PG4 + t_{PGD} (PG Delay)
	1	0	1			FS function: PG3 + t_{PGD} (PG Delay)
	1	1	0			FS function: PG2 + t_{PGD} (PG Delay)
	1	1	1			FS function: PG1 + t_{PGD} (PG Delay)

Table 6. Register 5 Bitmap

One last event mode, $000_{BIN,}$ disables the cascade effect and sets up PG4# going true as the trigger event. FS# must be pulled high before t_{PGD} elapses, or VGATE and all of the PG[4:1]# outputs are disabled.

Cascade enabled:

ENPGA enables PG2#, PG3# and PG4#;

ENPGB enables PG3# and PG4#;

ENPGC enables PG4#.

Cascade disabled:

ENPGA enables PG2#;

ENPGB enables PG3#;

ENPGC enables PG4#.

Simultaneous:

PG1#, PG2#, PG3# and PG4# operate independently from one another.

Sequenced:

PG1#, PG2#, PG3# and PG4# are dependent upon activation of PG(N–1) — for N = 2, 3, and 4 — plus a programmable PG delay.p=On

Register 6 - Address 0110

This register enables what events are recorded in the nonvolatile fault latch if bit 3 of R5 is cleared. The high order bits of this register control whether the under and over voltage pins are filtered, and the two low order bits program the current regulation time period.

Bits				Default	R/W	Description
3	2	1	0			
0				0b1	R/W	When bit 3 is cleared, the under voltage is filtered.
1						When bit 3 is set, the under voltage is not filtered.
	0			0b1	R/W	When bit 2 is cleared, the over voltage is filtered.
	1					When bit 2 is set, the over voltage is not filtered.
		0	0	0b00	R/W	When bits 1:0 are set to 0b00, the current regulation is turned off.
		0	1			When bits 1:0 are set to 0b01, the current regulation is 5 ms.
		1	0			When bits 1:0 are set to 0b10, the current regulation is 80 ms.
		1	1			When bits 1:0 are set to 0b11, the current regulation is 160 ms.

Table 7. Register 6 Bitmap

Register 7 - Address 0111

This register controls the UV hysteresis. The values shown are with respect to V_{SS}.

Bits				Default	R/W	Description
3	2	1	0			
1				0b1	R/W	In this register, bit 3 is always set.
1	0	0	0	0b001	R/W	When bits 2:0 are 0b000, the UV hysteresis = 0.0 volts.
	0	0	1			When bits 2:0 are 0b001, the UV hysteresis = 0.0625 volts.
	0	1	0			When bits 2:0 are 0b010, the UV hysteresis = 0.125 volts.
	0	1	1			When bits 2:0 are 0b011, the UV hysteresis = 0.1785 volts.
	1	0	0			When bits 2:0 are 0b100, the UV hysteresis = 0.250 volts.
	1	0	0			When bits 2:0 are 0b101, the UV hysteresis = 0.3125 volts.
	1	1	0			When bits 2:0 are 0b110, the UV hysteresis = 0.375 volts.
	1	1	1			When bits 2:0 are 0b111, the UV hysteresis = 0.4375 volts.

Table 8. Register 7 Bitmap

Register 8 - Address 1000

This register is used to control the I^2C bus interface activity. Bit 3 determines the Device Type Address, bits 2 and 1 select the register access capability, and bit 0 determines whether the device must receive a bus address that corresponds to the biasing of the address pins.

Note: If the fault latch option is selected and write access is denied the SMH4804 cannot be cleared of a fault condition.

Bits				Default	R/W	Description
3	2	1	0			
0				0b0	R/W	When bit 3 is cleared, the device type address is 1011.
1						When bit 3 is set, the device type address is 1010.
	0	0		0b00	R/W	When bits 2:1 are set to 0b00, the Configuration registers are read/write (R/W).
	0	1				When bits 2:1 are set to 0b01, the Configuration registers are read-only (RO).
	1	0				When bits 2:1 are set to 0b10 or 0b11, I^2C access to the Configuration registers is disabled.
	1	1				
			0	0b1	R/W	When bit 0 is cleared, the SMH4804 responds to all address pins.
			1			When bit 0 is set, the SMH4804 responds to the address set by the address pin pin polarities (A0,A1 and A2).

Table 9. Register 8 Bitmap

Register 9 - Address 1001

In this register, bit 3 works in conjunction with Register 3, bits 2 and 3. Refer to the Register 3 description for details. Bit 2 sets UV/OV conditions to be either latched or not latched. Bits 1 and 0 select the delay from the point where both PD[2:1]# inputs are low (or initial power up conditions) to when sequencing can commence.

Bits				Default	R/W	Description
3	2	1	0			
0	0			0b1	R/W	When bit 3 is cleared, the power good sequence is set to Fast.
1						When bit 3 is set, the power good sequence is set to Slow.
	0			0b0	R/W	When bit 2 is cleared, UV/OV conditions are not latched.
	1					When bit 2 is set, UV/OV conditions are latched.
		0	0	0b01	R/W	When bits 1:0 are set to 0b00, the PD delay is 0.5 ms.
		0	1			When bits 1:0 are set to 0b01, the PD delay is 80 ms.
		1	0			When bits 1:0 are set to 0b10, the PD delay is 160 ms.
		1	1			When bits 1:0 are set to 0b11, the PD delay is 320 ms.

Table 10. Register 9 Bitmap

Register C - Address 1100

This register is not a configuration register, but rather a nonvolatile fault latch (NVFL). If a circuit breaker fault condition is detected and the NVFL is enabled (Register 5, Bit 3 cleared), bit 0 of Register C is automatically set (written with a logic ‘1’) when the circuit breaker trips. So long as the bit remains set, the SMH4804 is not able to drive VGATE or the PG[4:1]# outputs. The host or service center must access the register and clear the bit (write a ‘0’) once the fault condition has been resolved. The bit can also be used as a nonvolatile Power on/off control to power the SMH4804 and system through the I^2C bus.

Bits				Default	R/W	Description
3	2	1	0			
			0	0b0	R/W	When bit 0 is cleared, the NV fault latch is cleared. This bit is cleared by software once the fault condition is resolved. When cleared by an I^2C command, the VGATE and PG[4:1]# outputs will power the system on.
			1			When bit 0 is set, the NV fault latch is set. This bit is set automatically by hardware when a fault is detected. When set by an I^2C command, the VGATE and PG[4:1]# outputs will power the system off.

Table 11. Register 9 Bitmap

PACKAGING

Figure 27 shows the package dimensions for the 28-pin SOIC package.

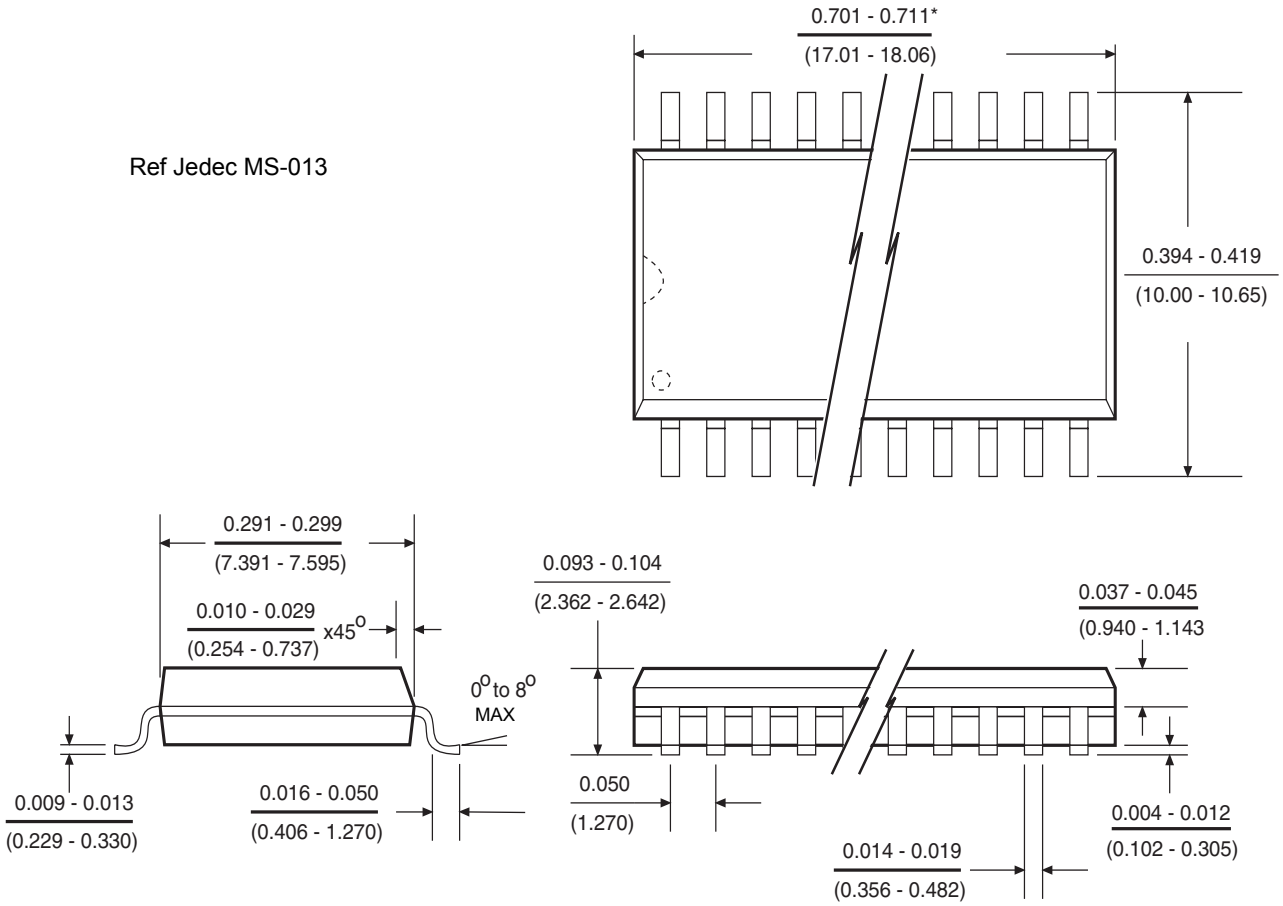


Figure 27. 28-Pin SOIC Package

Figure 28 shows the package dimensions for the 48-pin TQFP package.

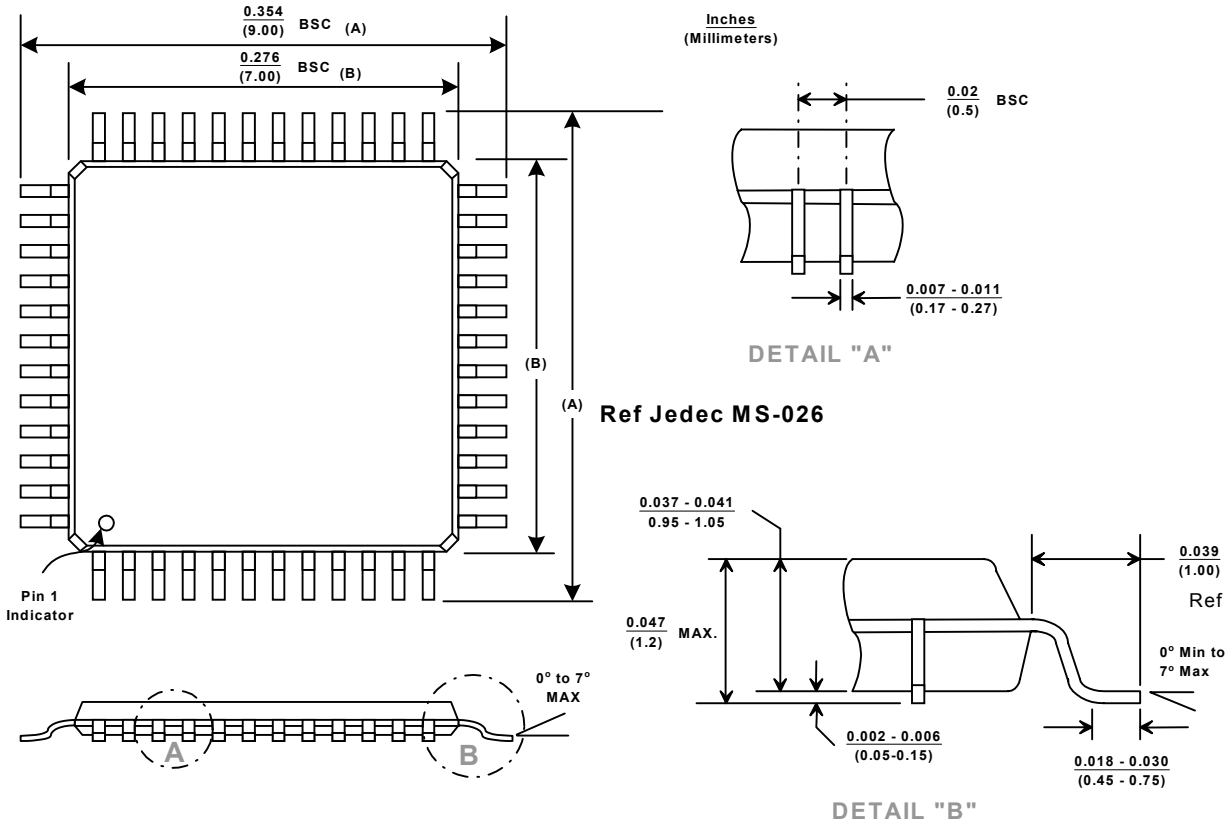
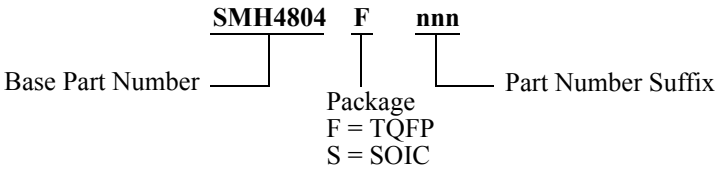
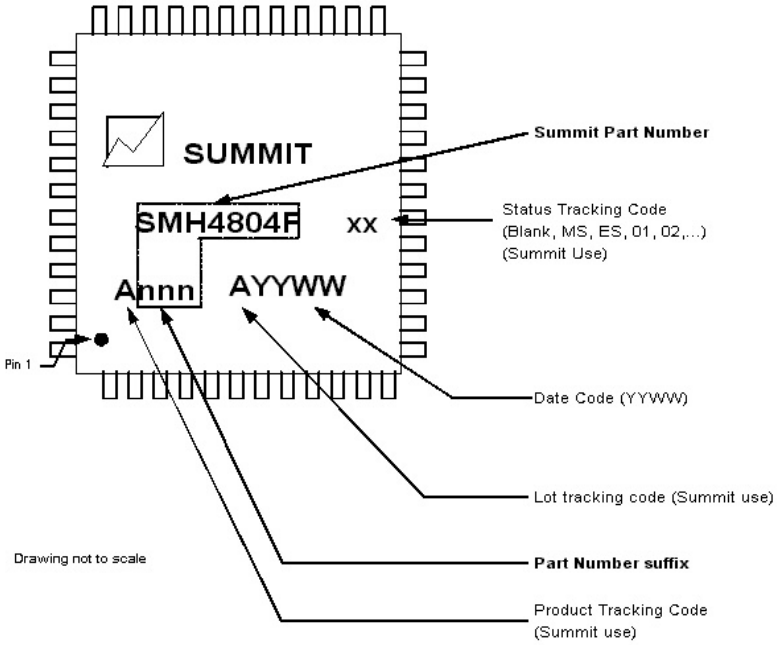


Figure 28. 48-Pin TQFP Package

ORDERING INFORMATION



PART MARKING



Revision 3.7 - This document supersedes all previous versions. Please check the Summit Microelectronics, Inc. web site at www.summitmicro.com for data sheet updates.