

20Mbps 7 Driver, 7 Receiver Multiprotocol Serial Transceiver with Termination Disable

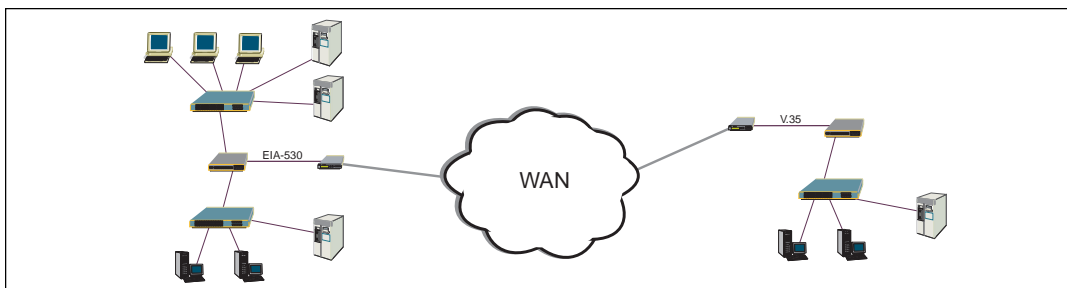
- 20Mbps Differential Transmission Rates
- Internal Termination Network Disable Control
- Interface Modes Supported:
 - ✓ RS-232 (v.28) ✓ X.21/RS-422 (v.11)
 - ✓ EIA-530 (v.10 & v.11) ✓ EIA-530A (v.10 & v.11)
 - ✓ RS-449 (v.10 & v.11) ✓ V.35 (v.35 & v.28)
 - ✓ V.36 (v.10 & v.11) ✓ RS-485 (un-terminated V.11)
- Software Protocol Selection
- Loopback Self-Test Mode
- Internal Transceiver Termination Resistors for V.11 and V.35 Protocols
- Driver and Receiver high-Z Control
- Improved ESD Tolerance for Analog I/Os
- Compliant to NET1/2 and TBR2 Physical Layer Requirements from SP505
- Applications include Routers, Switches, DSU/CSUs, and Access Devices



DESCRIPTION

The **SP516** is a monolithic device that supports eight (8) popular serial interface standards for DTE to DCE connectivity. The seven (7) drivers and seven (7) receivers can transmit and receive signals over 20Mbps. The **SP516** requires no additional external components for compliant operation for all of the eight (8) modes of operation. All necessary termination is integrated within the **SP516** and is switchable when V.35 drivers, V.35 receivers, and V.11 receivers are used. The **SP516** can operate as either a DTE or DCE.

Additional features with the **SP516** include internal loopback that can be initiated in either single-ended or differential modes. While in loopback mode, driver outputs are internally connected to receiver inputs, creating an internal signal path convenient for diagnostic testing. This eliminates the need for an external loopback plug. The **SP516** includes a termination network disable pin for the V.35 and V.11 receiver input termination circuitry. High-Z ability for the driver and receiver outputs is controlled by supplying a 4-bit word into the address decoder. Seven (7) drivers and one (1) receiver in the **SP516** include separate enable pins for added convenience.



ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}+7V

Input Voltages:

Logic.....-0.3V to (V_{CC} +0.5V)

Drivers.....-0.3V to (V_{CC} +0.5V)

Receivers..... $\pm 15.5V$

Output Voltages:

Logic.....-0.3V to (V_{CC} +0.5V)

Drivers..... $\pm 15V$

Receivers.....-0.3V to (V_{CC} +0.5V)

Storage Temperature.....-65°C to +150°C

Power Dissipation per package

80-pin QFP (derate 18.3mW/°C).....1500mW

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order to remove moisture prior to soldering. Sipex ships the 80-pin QFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

SPECIFICATIONS

$T_A = +25^\circ C$ and $V_{CC} = +4.75V$ to $+5.25V$ unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	$I_{OUT} = -3.2mA$
V_{OH}	2.4			Volts	$I_{OUT} = 1.0mA$
V.28 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			± 15	Volts	per Figure 1
Loaded Voltage	± 5.0		± 15	Volts	per Figure 2
Short-Circuit Current			± 100	mA	per Figure 3
Power-Off Impedance	300			Ω	per Figure 4
AC Parameters					$V_{CC} = +5V$ for AC parameters
Outputs					
Transition Time			1.5	μs	per Figure 5; +3V to -3V
Instantaneous Slew Rate			30	V/ μs	per Figure 6
Propagation Delay					
t_{PHL}	0.5	1	5	μs	
t_{PLH}	0.5	1	5	μs	
Max. Transmission Rate	120	230		kbps	
V.28 RECEIVER					
DC Parameters					
Inputs					
Input Impedance	3		7	k Ω	per Figure 7
Open-Circuit Bias			+2.0	Volts	per Figure 8
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
AC Parameters					$V_{CC} = +5V$ for AC parameters
Propagation Delay					
t_{PHL}	50	100	500	ns	
t_{PLH}	50	100	500	ns	

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.28 RECEIVER (continued) AC Parameters (cont.) Max. Transmission Rate	120	230		kbps	
V.10 DRIVER DC Parameters Outputs Open Circuit Voltage Test-Terminated Voltage Short-Circuit Current Power-Off Current AC Parameters Outputs Transition Time Propagation Delay t _{PHL} t _{PLH} Max. Transmission Rate	±4.0 0.9V _{OC}		±6.0 ±150 ±100	Volts Volts mA µA	per Figure 9 per Figure 10 per Figure 11 per Figure 12 V_{CC} = +5V for AC parameters
V.10 RECEIVER DC Parameters Inputs Input Current Input Impedance Sensitivity AC Parameters Propagation Delay t _{PHL} t _{PLH} Max. Transmission Rate	-3.25 4		+3.25 ±0.3	mA kΩ Volts	per Figures 14 and 15 V_{CC} = +5V for AC parameters
V.11 DRIVER DC Parameters Outputs Open Circuit Voltage Test Terminated Voltage Balance Offset Short-Circuit Current Power-Off Current AC Parameters Outputs Transition Time Propagation Delay t _{PHL} t _{PLH} Differential Skew Max. Transmission Rate	±2.0 0.5V _{OC}		±5.0 0.67V _{OC} ±0.4 +3.0 ±150 ±100	Volts Volts Volts Volts mA µA	per Figure 16 per Figure 17 per Figure 17 per Figure 17 per Figure 18 per Figure 19 V_{CC} = +5V for AC parameters
V.11 RECEIVER DC Parameters Inputs Common Mode Range Sensitivity	-7		+7 ±0.3	Volts Volts	per Figures 21 and 36; 10% to 90% per Figures 33 and 36, C _L = 50pF per Figures 33 and 36, C _L = 50pF per Figures 33 and 36, C _L = 50pF per Figure 33, C _L = 50pF f _{IN} = 10MHz

SPECIFICATIONS

T_A = +25°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.11 RECEIVER (continued)					
DC Parameters (cont.)					
Input Current	-3.25		±3.25	mA	per Figure 20 and 22
Current w/ 100Ω Termination			±60.75	mA	per Figure 23 and 24
Input Impedance	4			kΩ	
AC Parameters					
Propagation Delay					V_{CC} = +5V for AC parameters
t _{PHL}	30	65	85	ns	per Figures 33 and 38; C _L = 50pF
t _{PLH}	30	65	85	ns	per Figures 33 and 38; C _L = 50pF
Differential Skew		10		ns	per Figure 33; C _L = 50pF
Max.Transmission Rate	20			Mbps	per Figure 33; C _L = 50pF f _{IN} = 10MHz
V.35 DRIVER					
DC Parameters					
Outputs					
Open Circuit Voltage			±1.20	Volts	per Figure 16
Test Terminated Voltage	±0.44		±0.66	Volts	per Figure 25
Offset			±0.6	Volts	per Figure 25
Source Impedance	50		150	Ω	per Figure 27; Z _S = V ₂ /V ₁ x 50Ω
Short-Circuit Impedance	135		165	Ω	per Figure 28
AC Parameters					
Outputs					
Transition Time		30	40	ns	per Figure 29; 10% to 90%
Propagation Delay					
t _{PHL}	50	70	90	ns	per Figures 33 and 36; C _L = 20pF
t _{PLH}	50	70	90	ns	per Figures 33 and 36; C _L = 20pF
Differential Skew		60	10	ns	per Figures 33 and 36; C _L = 20pF
Max.Transmission Rate	20			Mbps	per Figure 33; C _L = 20pF f _{IN} = 10MHz
V.35 RECEIVER					
DC Parameters					
Inputs					
Sensitivity		±80		mV	
Source Impedance	90		110	Ω	per Figure 30; Z _S = V ₂ /V ₁ x 50Ω
Short-Circuit Impedance	135		165	Ω	per Figure 31
AC Parameters					
Propagation Delay					V_{CC} = +5V for AC parameters
t _{PHL}	30	50	90	ns	per Figures 33 and 38; C _L = 20pF
t _{PLH}	30	50	90	ns	per Figures 33 and 38; C _L = 20pF
Differential Skew		10		ns	per Figure 33; C _L = 20pF
Max.Transmission Rate	20			Mbps	per Figure 33; C _L = 20pF f _{IN} = 10MHz
TRANSCEIVER LEAKAGE CURRENTS					
Driver Output 3-State Current		500		μA	per Figure 32; Drivers disabled
Rcvr Output 3-State Current		1	10	μA	DEC _X = 0000, 0.4V ≤ V _O ≤ 2.4V

OTHER AC CHARACTERISTICS

$T_A = +25^\circ\text{C}$ and $V_{CC} = +5.0\text{V}$ unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND high-Z MODE					
RS-232/V.28					
t_{PZL} ; high-Z to Output LOW		0.70	5.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_1 closed
t_{PZH} ; high-Z to Output HIGH		0.40	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PLZ} ; Output LOW to high-Z		0.20	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_1 closed
t_{PHZ} ; Output HIGH to high-Z		0.40	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
RS-423/V.10					
t_{PZL} ; high-Z to Output LOW		0.15	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_1 closed
t_{PZH} ; high-Z to Output HIGH		0.20	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
t_{PLZ} ; Output LOW to high-Z		0.20	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_1 closed
t_{PHZ} ; Output HIGH to high-Z		0.15	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 40; S_2 closed
RS-422/V.11					
t_{PZL} ; high-Z to Output LOW		2.80	10.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PZH} ; high-Z to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_2 closed
t_{PLZ} ; Output LOW to high-Z		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PHZ} ; Output HIGH to high-Z		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_2 closed
V.35					
t_{PZL} ; high-Z to Output LOW		2.60	10.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PZH} ; high-Z to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 34 & 37; S_2 closed
t_{PLZ} ; Output LOW to high-Z		0.10	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_1 closed
t_{PHZ} ; Output HIGH to high-Z		0.15	2.0	μs	$C_L = 15\text{pF}$, Fig. 34 & 37; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND high-Z MODE					
RS-232/V.28					
t_{PZL} ; high-Z to Output LOW		0.12	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_1 closed
t_{PZH} ; high-Z to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_2 closed
t_{PLZ} ; Output LOW to high-Z		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_1 closed
t_{PHZ} ; Output HIGH to high-Z		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_2 closed
RS-423/V.10					
t_{PZL} ; high-Z to Output LOW		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_1 closed
t_{PZH} ; high-Z to Output HIGH		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_2 closed
t_{PLZ} ; Output LOW to high-Z		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_1 closed
t_{PHZ} ; Output HIGH to high-Z		0.10	2.0	μs	$C_L = 100\text{pF}$, Fig. 35 & 38; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-422/V.11					
t _{PZL} ; high-Z to Output LOW		0.10	2.0	μs	C _L = 100pF, Fig. 35 & 39; S ₁ closed
t _{PZH} ; high-Z to Output HIGH		0.10	2.0	μs	C _L = 100pF, Fig. 35 & 39; S ₂ closed
t _{PLZ} ; Output LOW to high-Z		0.10	2.0	μs	C _L = 15pF, Fig. 35 & 39; S ₁ closed
t _{PHZ} ; Output HIGH to high-Z		0.10	2.0	μs	C _L = 15pF, Fig. 35 & 39; S ₂ closed
V.35					
t _{PZL} ; high-Z to Output LOW		0.10	2.0	μs	C _L = 100pF, Fig. 35 & 39; S ₁ closed
t _{PZH} ; high-Z to Output HIGH		0.10	2.0	μs	C _L = 100pF, Fig. 35 & 39; S ₂ closed
t _{PLZ} ; Output LOW to high-Z		0.10	2.0	μs	C _L = 15pF, Fig. 35 & 39; S ₁ closed
t _{PHZ} ; Output HIGH to high-Z		0.10	2.0	μs	C _L = 15pF, Fig. 35 & 39; S ₂ closed
TRANSCEIVER TO TRANSCEIVER SKEW (per Figures 33, 36, 38)					
V.28 Driver		100		ns	[(t _{phi}) _{TX1} - (t _{phi}) _{TX6,7}]
		100		ns	[(t _{phi}) _{TX1} - (t _{phi}) _{TX6,7}]
V.28 Receiver		20		ns	[(t _{phi}) _{RX1} - (t _{phi}) _{RX2,7}]
		20		ns	[(t _{phi}) _{RX1} - (t _{phi}) _{RX2,7}]
V.11 Driver		2		ns	[(t _{phi}) _{TX1} - (t _{phi}) _{TX6,7}]
		2		ns	[(t _{phi}) _{TX1} - (t _{phi}) _{TX6,7}]
V.11 Receiver		3		ns	[(t _{phi}) _{RX1} - (t _{phi}) _{RX2,7}]
		3		ns	[(t _{phi}) _{RX1} - (t _{phi}) _{RX2,7}]
V.10 Driver		5		ns	[(t _{phi}) _{TX2} - (t _{phi}) _{TX3,4,5}]
		5		ns	[(t _{phi}) _{TX2} - (t _{phi}) _{TX3,4,5}]
V.10 Receiver		5		ns	[(t _{phi}) _{RX2} - (t _{phi}) _{RX3,4,5}]
		5		ns	[(t _{phi}) _{RX2} - (t _{phi}) _{RX3,4,5}]
V.35 Driver		4		ns	[(t _{phi}) _{TX1} - (t _{phi}) _{TX6,7}]
		4		ns	[(t _{phi}) _{TX1} - (t _{phi}) _{TX6,7}]
V.35 Receiver		6		ns	[(t _{phi}) _{RX1} - (t _{phi}) _{RX2,7}]
		6		ns	[(t _{phi}) _{RX1} - (t _{phi}) _{RX2,7}]

POWER REQUIREMENTS

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V _{CC}	4.75	5.00	5.25	Volts	
I _{CC} (No Mode Selected) (V.28/RS-232) (V.11/RS-422) (EIA-530 & RS-449) (V.35)		30 65 175 250 100		mA mA mA mA mA	All I _{CC} values are with V _{CC} = +5V f _{IN} = 120kbps; Drivers active & loaded. f _{IN} = 10Mbps; Drivers active & loaded. f _{IN} = 10Mbps; Drivers active & loaded. V.35 @ f _{IN} = 10Mbps, V.28 @ 20kbps; Drivers active & loaded.

TEST CIRCUITS

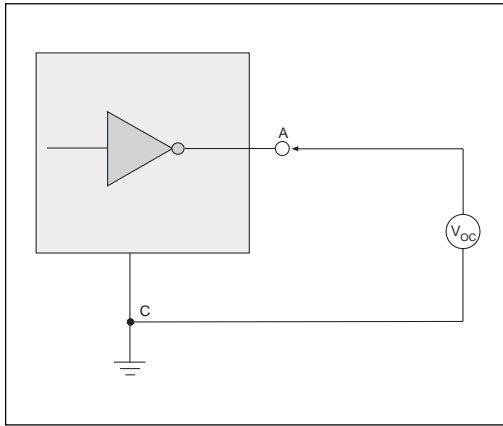


Figure 1. V.28 Driver Output Open Circuit Voltage

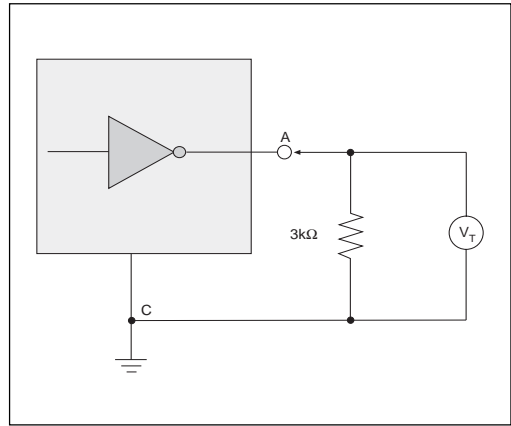


Figure 2. V.28 Driver Output Loaded Voltage

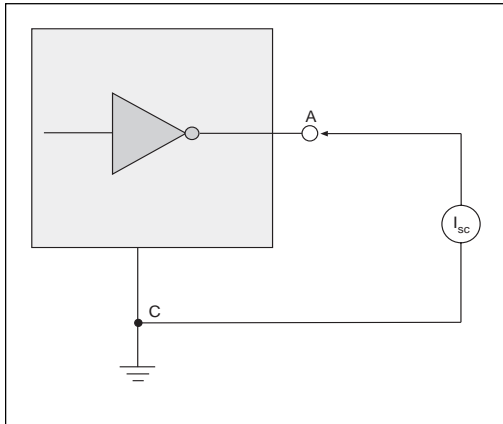


Figure 3. V.28 Driver Output Short-Circuit Current

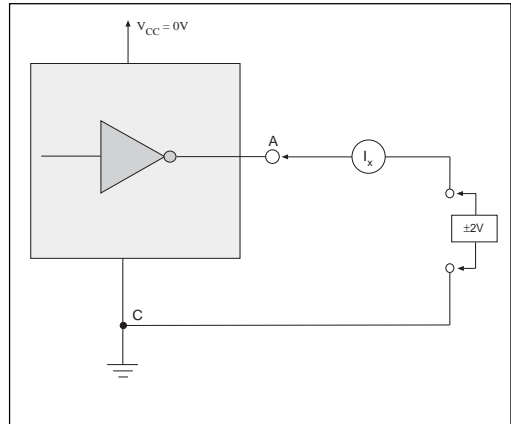


Figure 4. V.28 Driver Output Power-Off Impedance

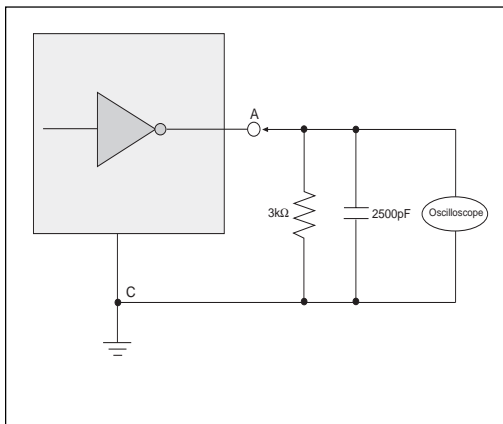


Figure 5. V.28 Driver Output Rise/Fall Times

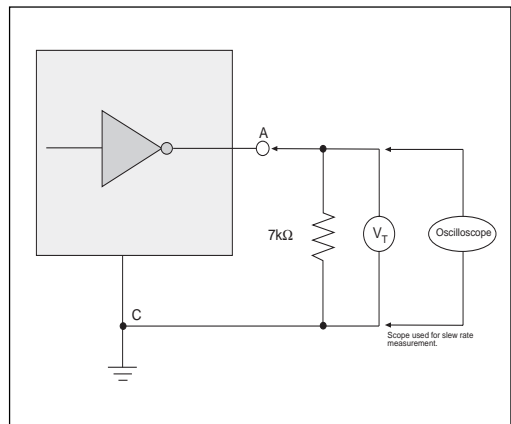


Figure 6. V.28 Driver Output Slew Rate

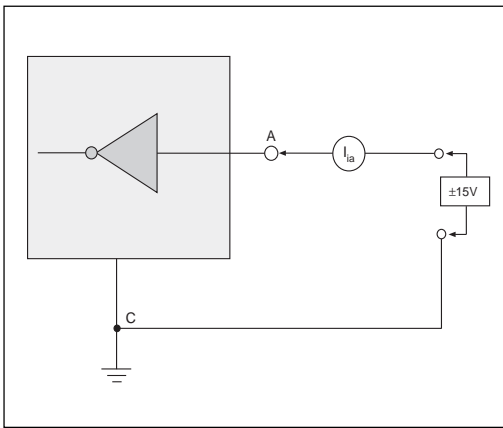


Figure 7. V.28 Receiver Input Impedance

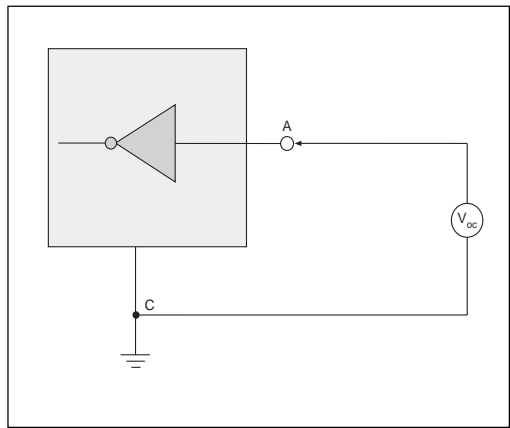


Figure 8. V.28 Receiver Input Open Circuit Bias

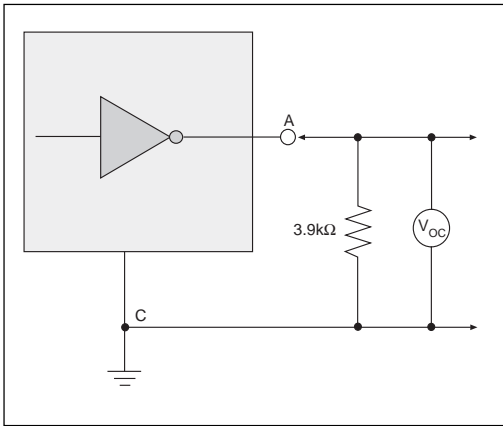


Figure 9. V.10 Driver Output Open-Circuit Voltage

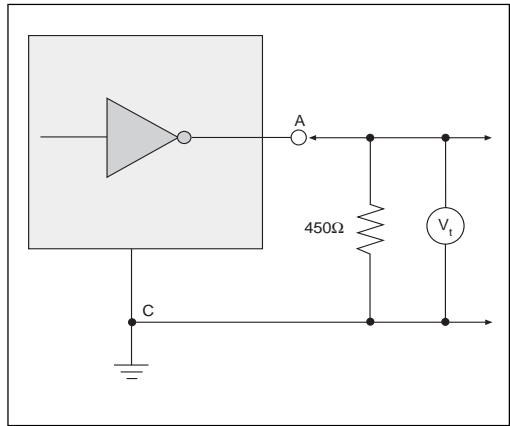


Figure 10. V.10 Driver Output Test Terminated Voltage

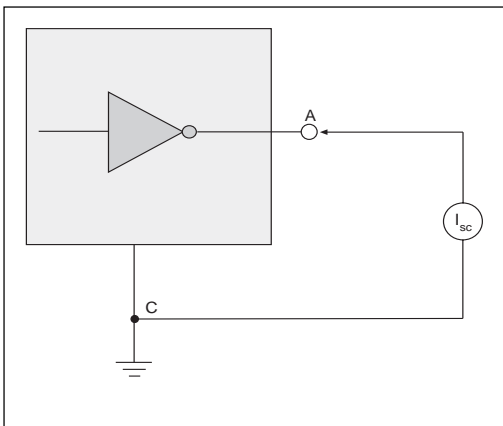


Figure 11. V.10 Driver Output Short-Circuit Current

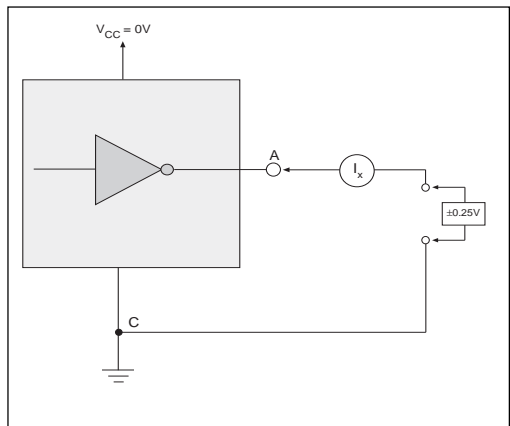


Figure 12. V.10 Driver Output Power-Off Current

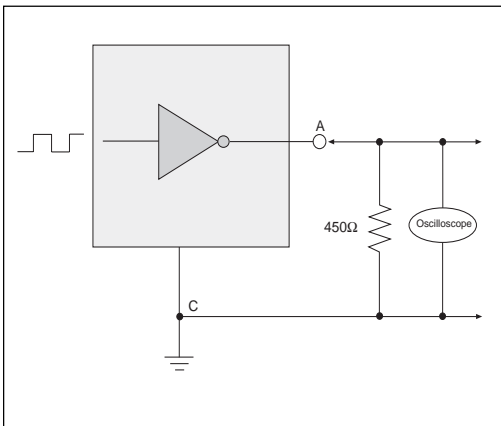


Figure 13. V.10 Driver Output Transition Time

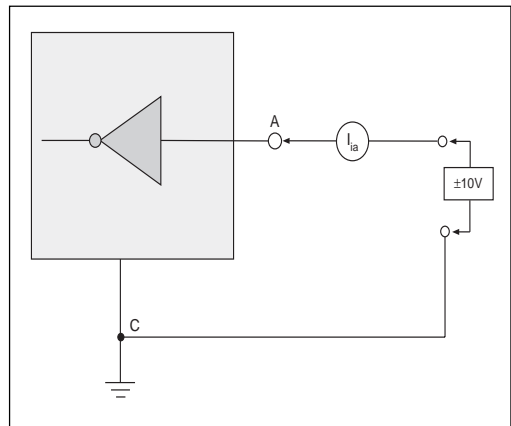


Figure 14. V.10 Receiver Input Current

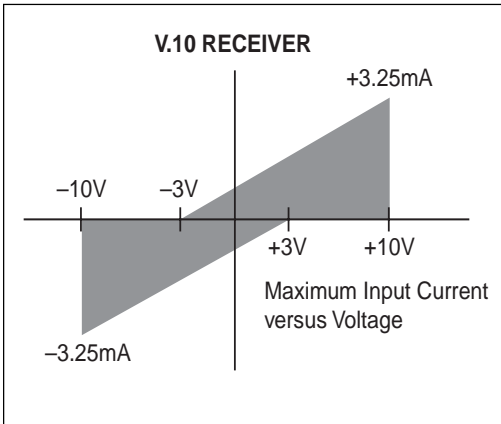


Figure 15. V.10 Receiver Input IV Graph

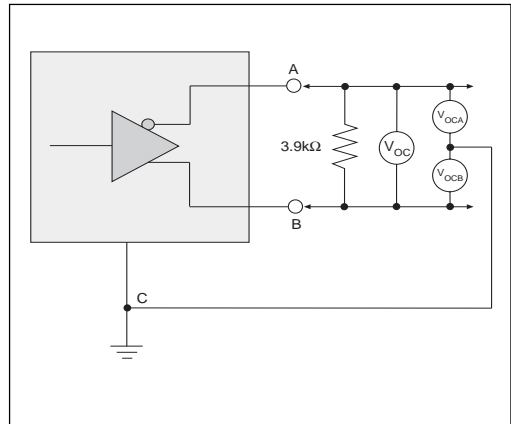


Figure 16. V.11 and V.35 Driver Output Open-Circuit Voltage

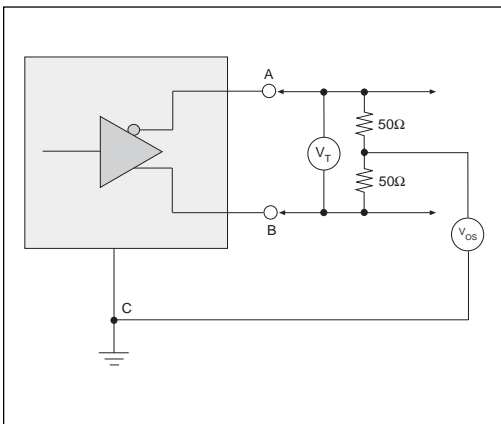


Figure 17. V.11 Driver Output Test Terminated Voltage

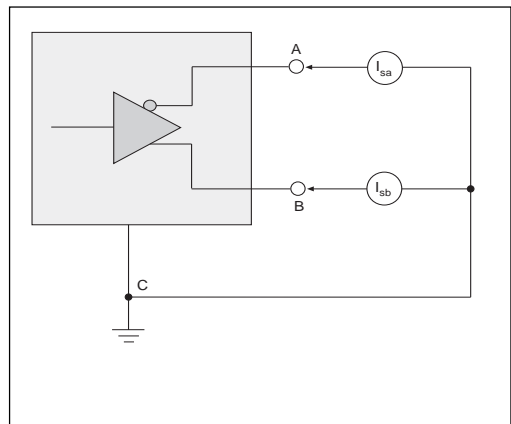


Figure 18. V.11 Driver Output Short-Circuit Current

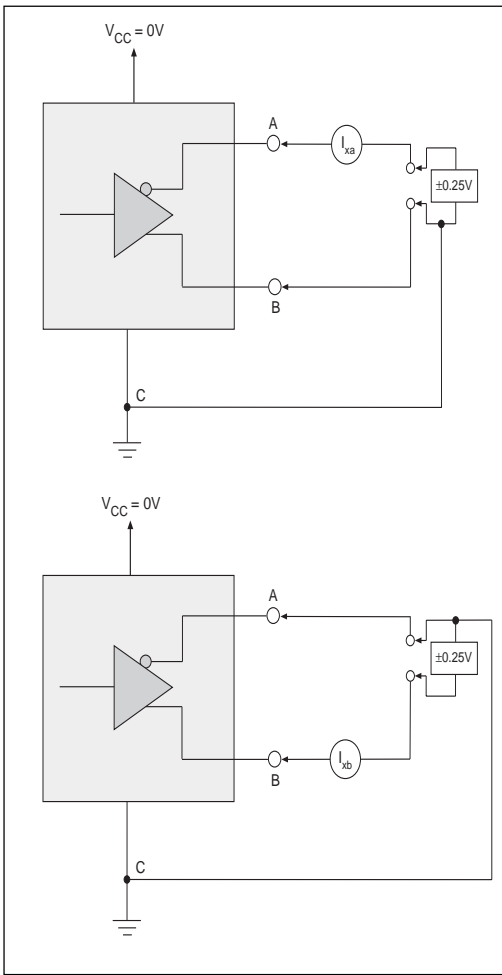


Figure 19. V.11 Driver Output Power-Off Current

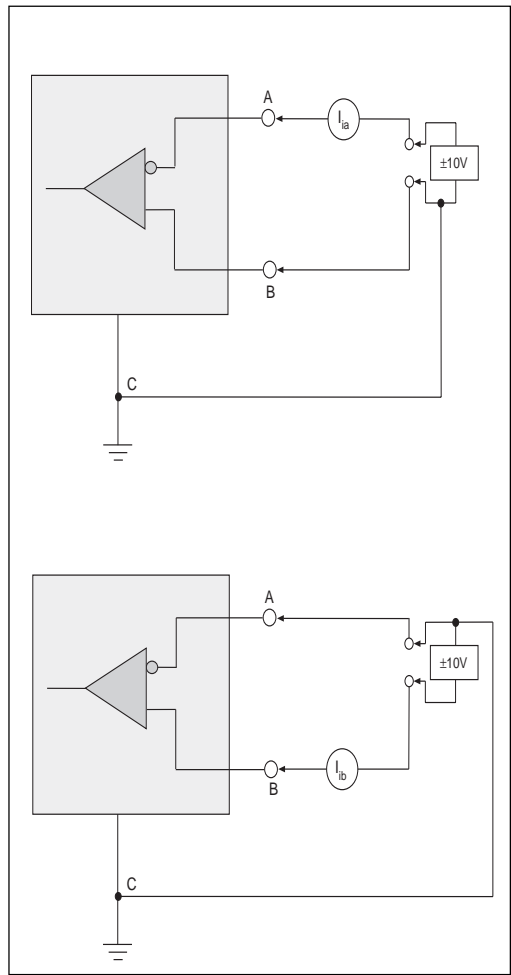


Figure 20. V.11 Receiver Input Current

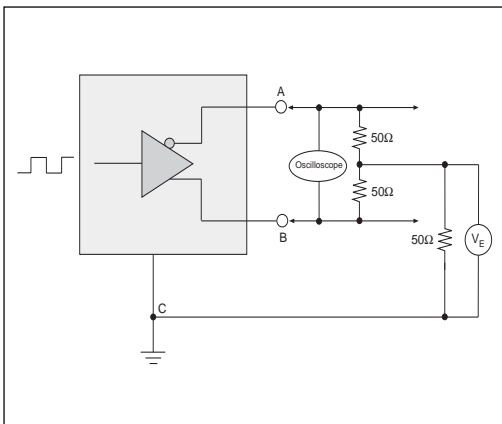


Figure 21. V.11 Driver Output Rise/Fall Time

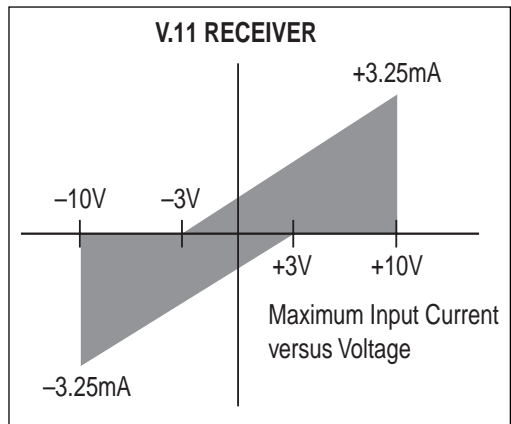


Figure 22. V.11 Receiver Input IV Graph

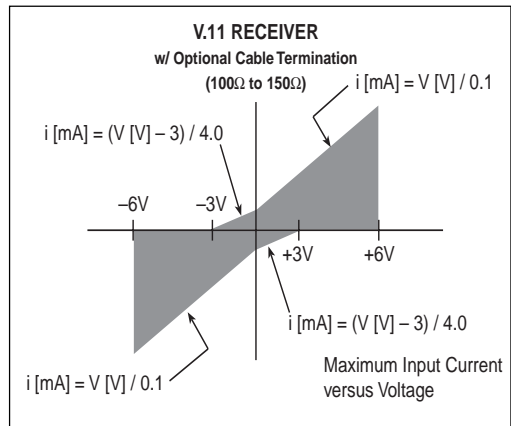
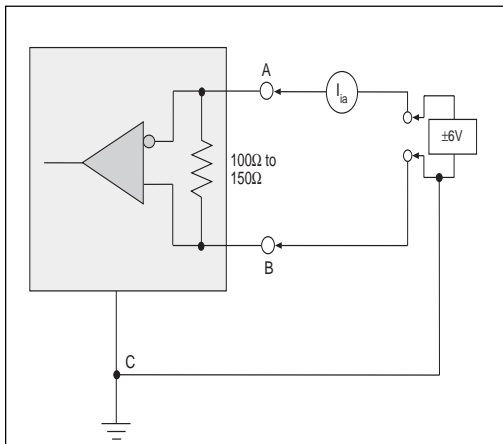


Figure 24. V.11 Receiver Input Graph w/ Termination

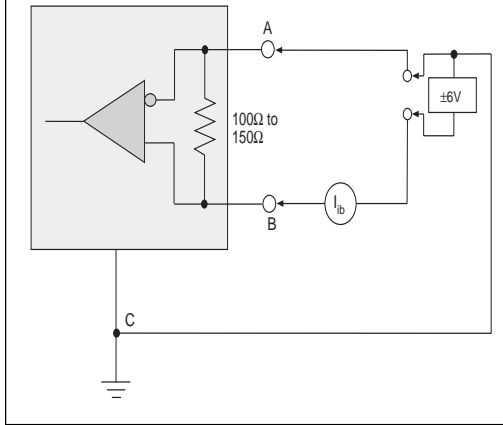


Figure 23. V.11 Receiver Input Current w/ Termination

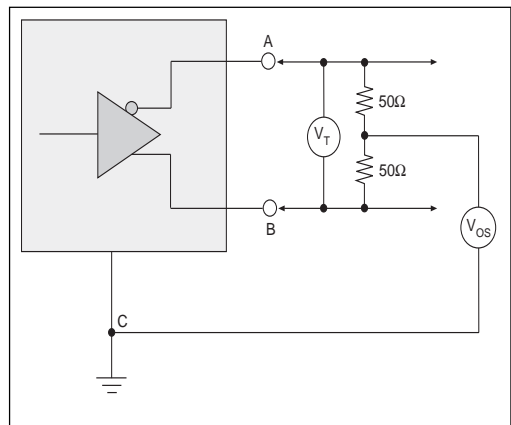


Figure 25. V.35 Driver Output Test Terminated Voltage

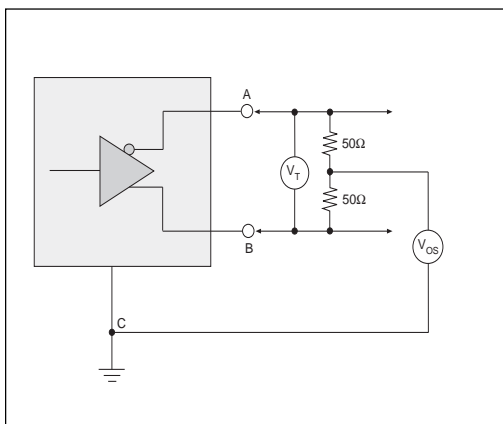


Figure 26. V.35 Driver Output Offset Voltage

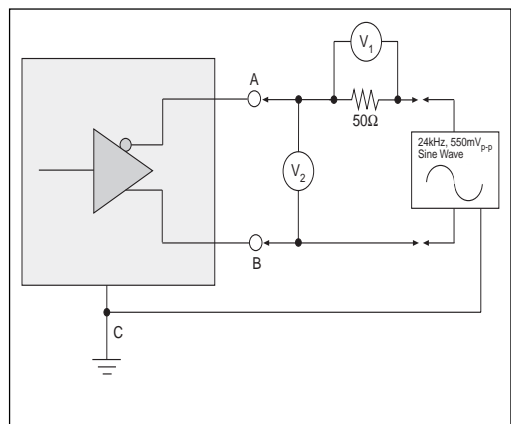


Figure 27. V.35 Driver Output Source Impedance

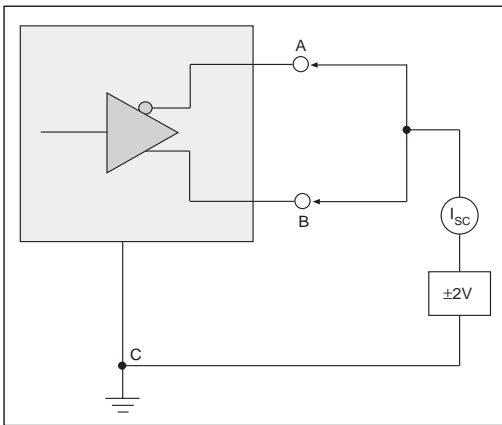


Figure 28. V.35 Driver Output Short-Circuit Impedance

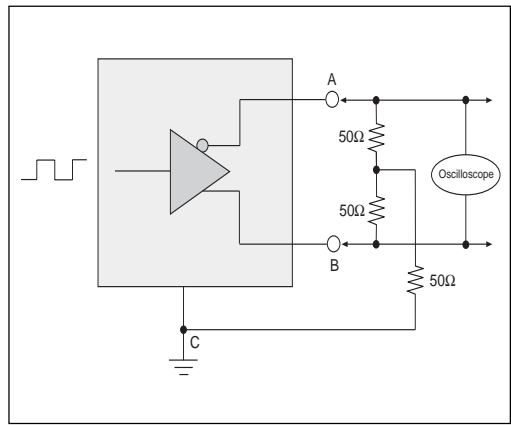


Figure 29. V.35 Driver Output Rise/Fall Time

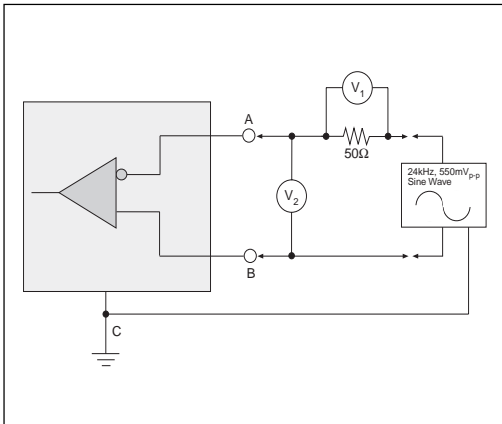


Figure 30. V.35 Receiver Input Source Impedance

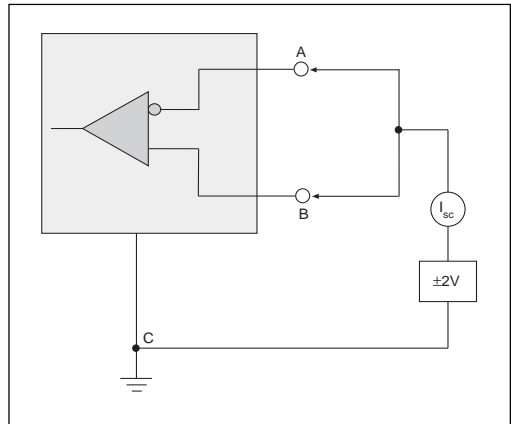


Figure 31. V.35 Receiver Input Short-Circuit Impedance

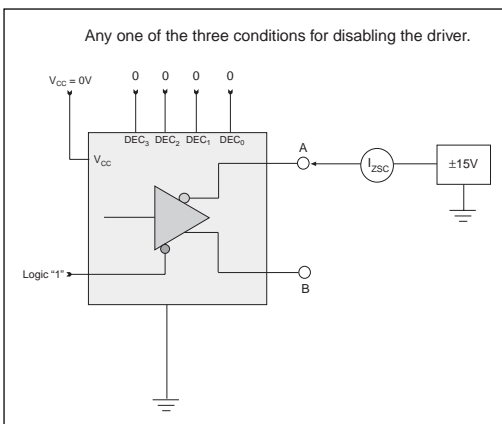


Figure 32. Driver Output Leakage Current Test

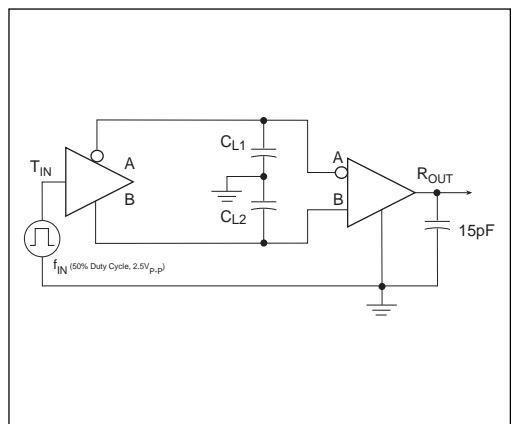


Figure 33. Driver/Receiver Timing Test Circuit

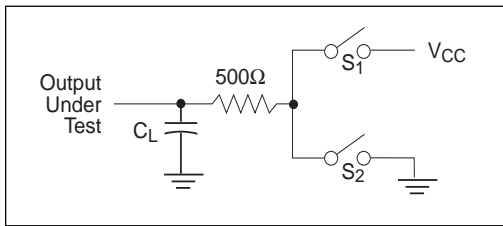


Figure 34. Driver Timing Test Load Circuit

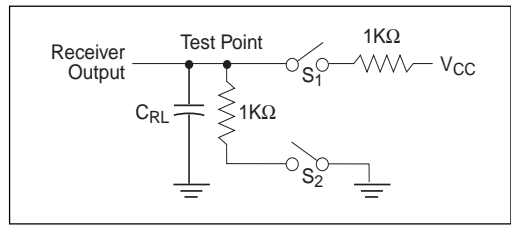


Figure 35. Receiver Timing Test Load Circuit

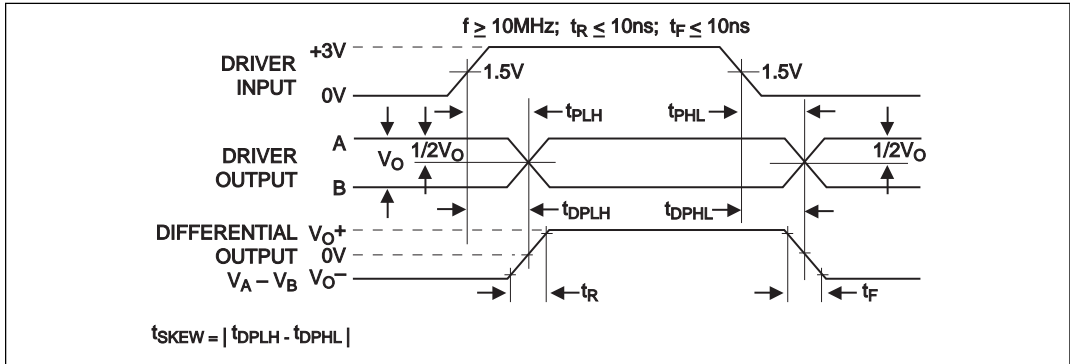


Figure 36. Driver Propagation Delays

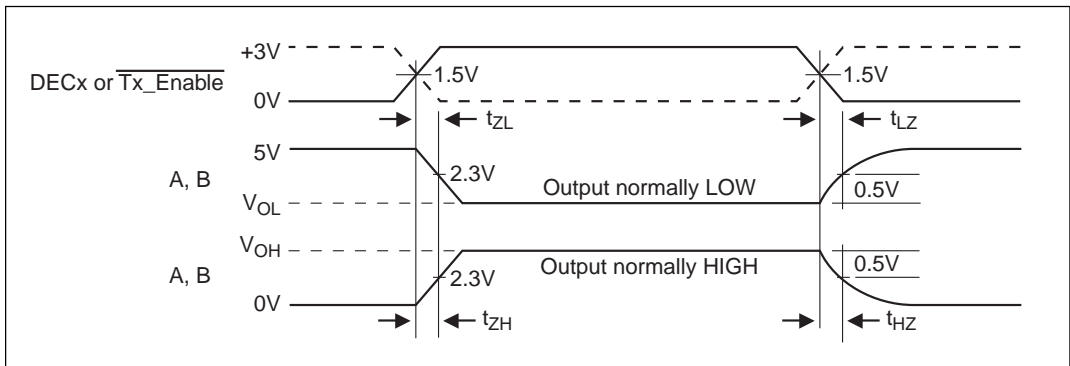


Figure 37. Driver Enable and Disable Times

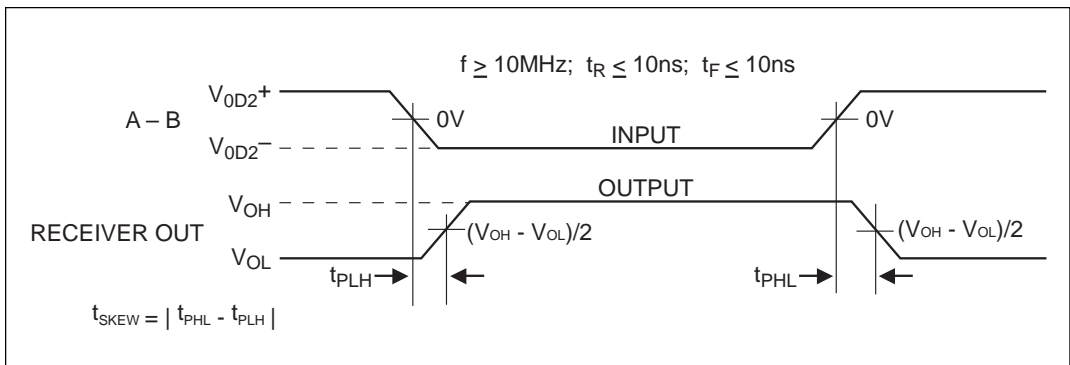


Figure 38. Receiver Propagation Delays

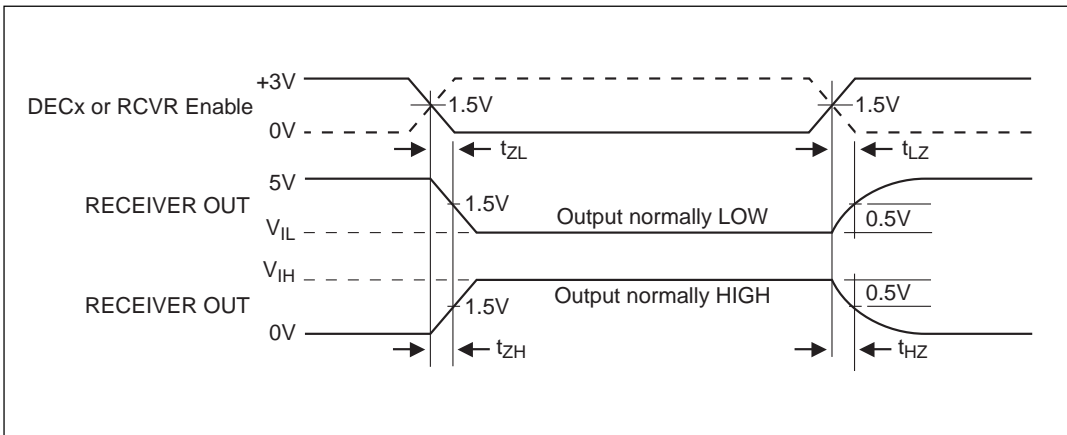


Figure 39. Receiver Enable and Disable Times

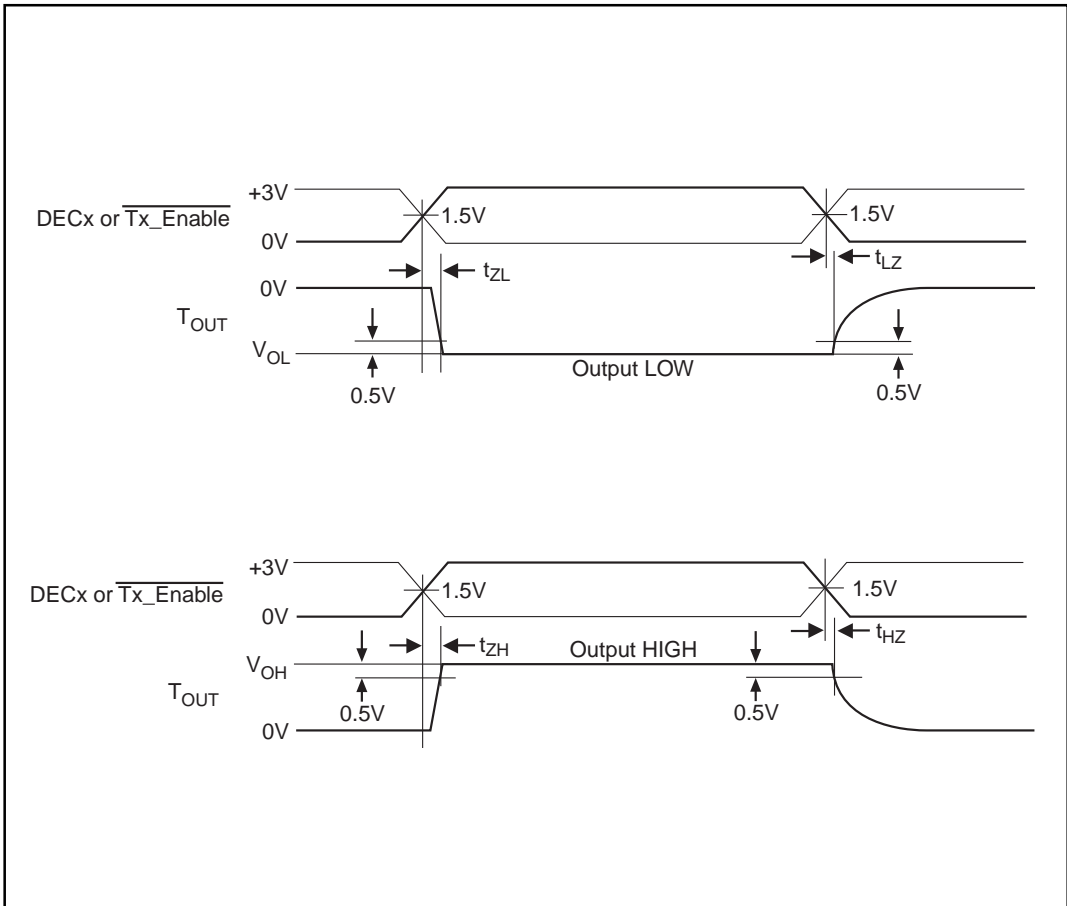


Figure 40. V.28 (RS-232) and V.10 (RS-423) Driver Enable and Disable Times

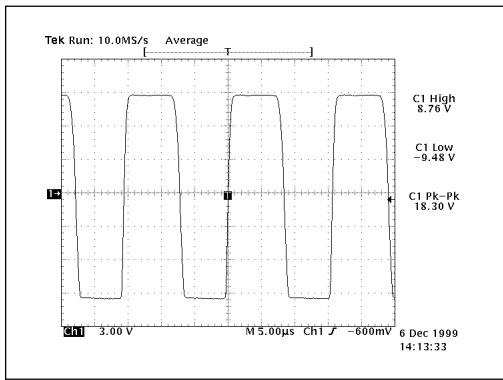


Figure 41. Typical V.28 Driver Output Waveform

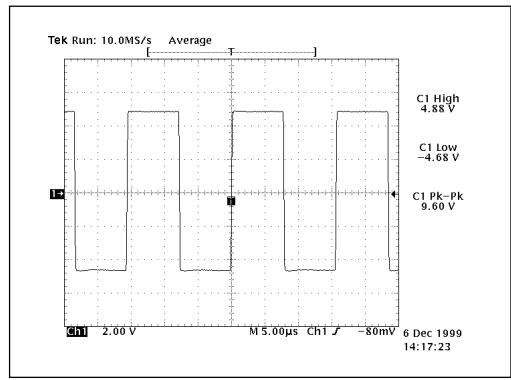


Figure 42. Typical V.10 Driver Output Waveform

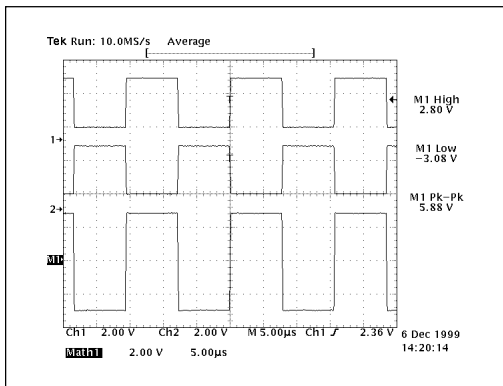


Figure 43. Typical V.11 Driver Output Waveform

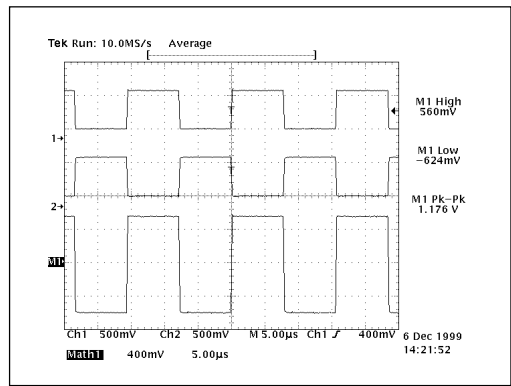
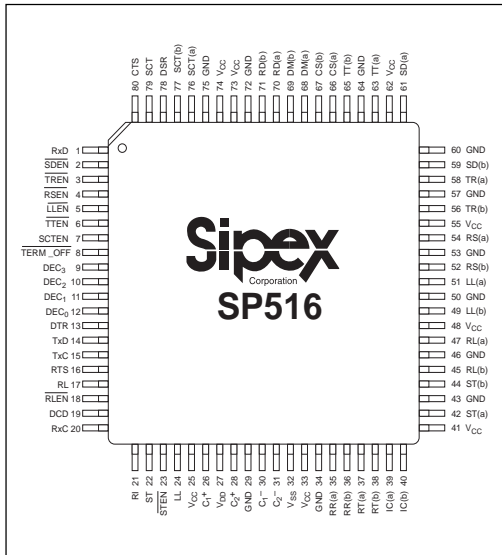


Figure 44. Typical V.35 Driver Output Waveform

PINOUT



PIN ASSIGNMENTS

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non-inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit; analog input, non-inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 19 — DCD — Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring In; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a) — Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b) — Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a) — Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b) — Incoming Call; analog input, non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49 — LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a) — Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b) — Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a) — Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b) — Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR — Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS — Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pin 2 — $\overline{\text{SDEN}}$ — Enables TxD driver, active low; TTL input.

Pin 3 — $\overline{\text{TREN}}$ — Enables DTR driver, active low; TTL input.

Pin 4 — $\overline{\text{RSEN}}$ — Enables RTS driver, active low; TTL input.

Pin 5 — $\overline{\text{LLEN}}$ — Enables LL driver, active low; TTL input.

Pin 6 — $\overline{\text{TTEN}}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pin 8 — $\overline{\text{TERM_OFF}}$ — Active low control pin disconnects the receiver input termination circuitry. Logic high input connects the V.35 and V.11 receiver input termination circuitry.

Pins 12–9 — DEC_0 – DEC_3 — Transmitter and receiver decode register; configures transmitter and receiver modes; TTL inputs.

Pin 18 — $\overline{\text{RLEN}}$ — Enables RL driver; active low; TTL input.

Pin 23 — $\overline{\text{STEN}}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — $V_{\text{DD}} +10\text{V}$ Charge Pump Capacitor — Connects from V_{DD} to V_{CC} . Suggested capacitor size is 22 μF , 16V.

Pin 32 — $V_{\text{SS}} -10\text{V}$ Charge Pump Capacitor — Connects from ground to V_{SS} . Suggested capacitor size is 22 μF , 16V.































Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^- . Suggested capacitor size is 22 μF , 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^- . Suggested capacitor size is 22 μF , 16V.

Table 1 SP516 Driver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422 w/Term.	RS422	RS449	EIA530	EIA-530A	V.36
DEC ₃ - DEC ₀	0000	0010	1110	0100	0101	1100	1101	1111	0110
SD(a)	high-Z	V.28	V.35-	V.11-	V.11-	V.11-	V.11-	V.11-	V.11-
SD(b)	high-Z	high-Z	V.35+	V.11+	V.11+	V.11+	V.11+	V.11+	V.11+
TR(a)	high-Z	V.28	V.28	V.11-	V.11-	V.11-	V.11-	V.10	V.10
TR(b)	high-Z	high-Z	high-Z	V.11+	V.11+	V.11+	V.11+	high-Z	high-Z
RS(a)	high-Z	V.28	V.28	V.11-	V.11-	V.11-	V.11-	V.11-	V.10
RS(b)	high-Z	high-Z	high-Z	V.11+	V.11+	V.11+	V.11+	V.11+	high-Z
RL(a)	high-Z	V.28	V.28	V.11-	V.11-	V.10	V.11-	V.11-	V.10
RL(b)	high-Z	high-Z	high-Z	V.11+	V.11+	high-Z	V.11+	V.11+	high-Z
LL(a)	high-Z	V.28	V.28	V.11-	V.11-	V.10	V.10	V.10	V.10
LL(b)	high-Z	high-Z	high-Z	V.11+	V.11+	high-Z	high-Z	high-Z	high-Z
ST(a)	high-Z	V.28	V.35-	V.11-	V.11-	V.11-	V.11-	V.11-	V.11-
ST(b)	high-Z	high-Z	V.35+	V.11+	V.11+	V.11+	V.11+	V.11+	V.11+
TT(a)	high-Z	V.28	V.35-	V.11-	V.11-	V.11-	V.11-	V.11-	V.11-
TT(b)	high-Z	high-Z	V.35+	V.11+	V.11+	V.11+	V.11+	V.11+	V.11+

Table 2 SP516 Receiver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422 w/Term.	RS422	RS449	EIA530	EIA-530A	V.36
DEC ₃ - DEC ₀	0000	0010	1110	0100	0101	1100	1101	1111	0110
RD(a)	>10kΩ to GND	V.28	V.35-	V.11- 	V.11-	V.11- 	V.11- 	V.11- 	V.11- 
RD(b)	>10kΩ to GND	>10kΩ to GND	V.35+	V.11+ 	V.11+	V.11+ 	V.11+ 	V.11+ 	V.11+ 
RT(a)	>10kΩ to GND	V.28	V.35-	V.11- 	V.11-	V.11- 	V.11- 	V.11- 	V.11- 
RT(b)	>10kΩ to GND	>10kΩ to GND	V.35+	V.11+ 	V.11+	V.11+ 	V.11+ 	V.11+ 	V.11+ 
CS(a)	>10kΩ to GND	V.28	V.28	V.11-	V.11-	V.11-	V.11-	V.11-	V.10
CS(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND
DM(a)	>10kΩ to GND	V.28	V.28	V.11-	V.11-	V.11-	V.11-	V.10	V.10
DM(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND	>10kΩ to GND
RR(a)	>10kΩ to GND	V.28	V.28	V.11-	V.11-	V.11-	V.11-	V.11-	V.10
RR(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	V.11+	V.11+	V.11+	>10kΩ to GND
IC(a)	>10kΩ to GND	V.28	V.28	V.11-	V.11-	V.10	V.10	V.10	V.10
IC(b)	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	V.11+	V.11+	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND	>10kΩ to GND
SCT(a)	>10kΩ to GND	V.28	V.35-	V.11- 	V.11-	V.11- 	V.11- 	V.11- 	V.11- 
SCT(b)	>10kΩ to GND	>12kΩ to GND	V.35+	V.11+ 	V.11+	V.11+ 	V.11+ 	V.11+ 	V.11+ 

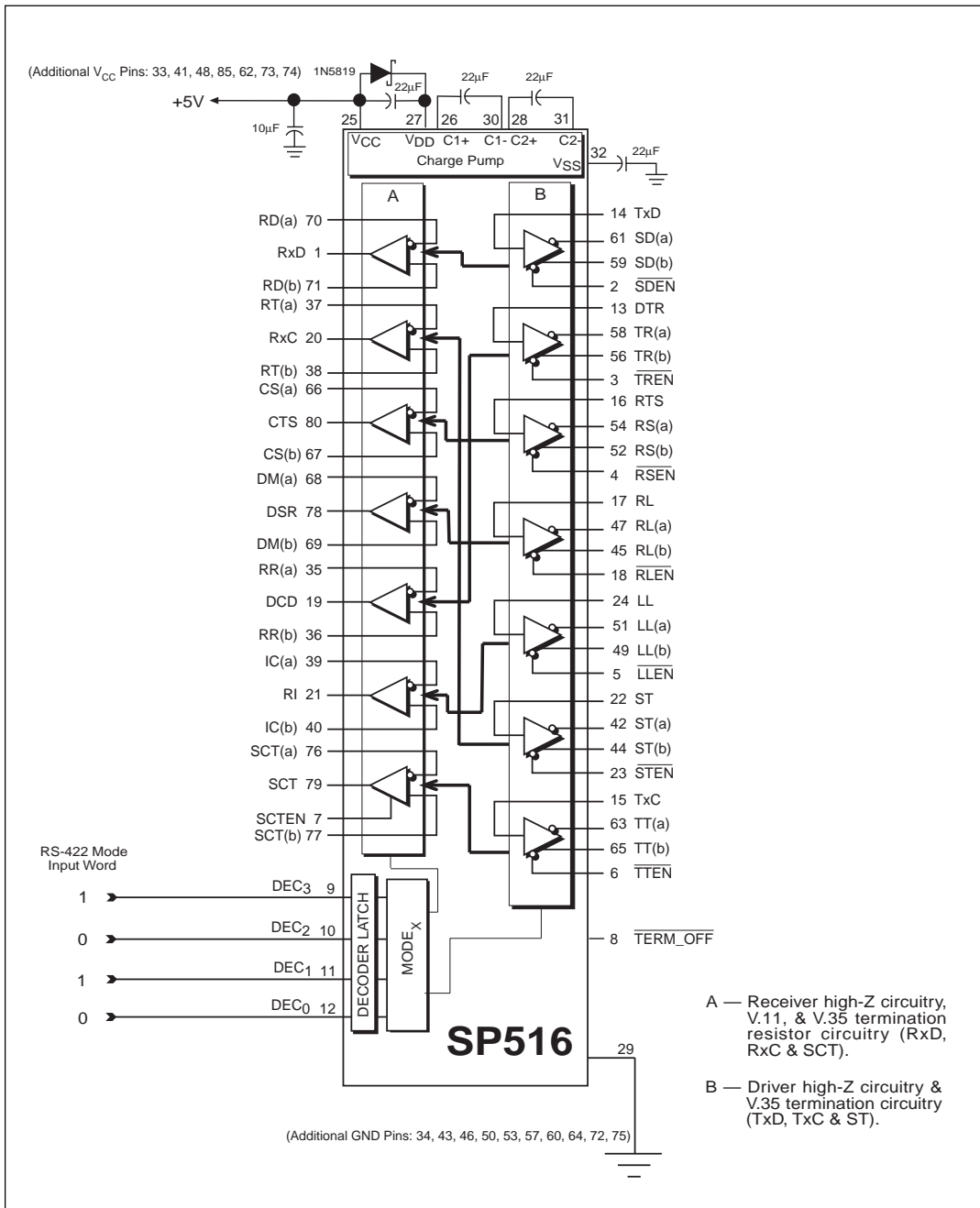
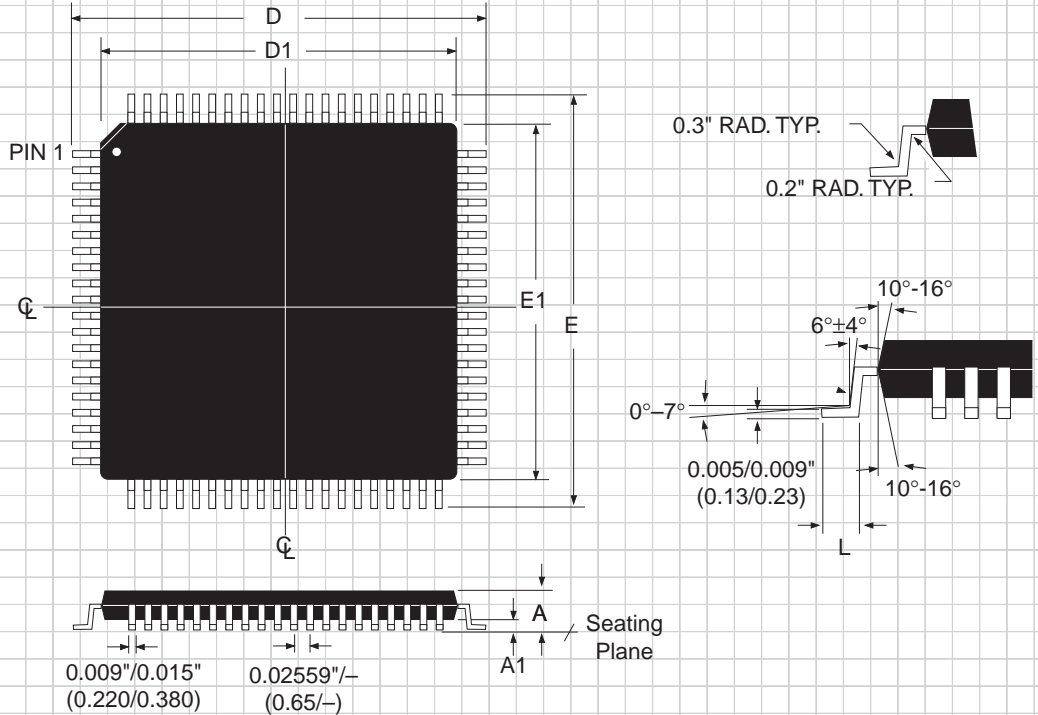


Figure 45. SP516 Typical Operating Circuit

**PACKAGE: QUAD FLATPACK
JEDEC "BE-2" OUTLINE**



DIMENSIONS in Inches Minimum/Maximum (mm)	JEDEC BE-2 Outline 80-PIN
A	-/0.0925 (-/2.350)
A1	-/0.010 (-/0.250)
D	0.667/0.687 (16.950/17.450)
D1	0.547/0.555 (13.900/14.100)
E	0.667/0.687 (16.950/17.450)
E1	0.547/0.555 (13.900/14.100)
L	0.0255/0.0375 (0.650/0.950)

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP516CF	0°C to +70°C	80-pin JEDEC (BE-2 Outline) QFP



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