Multi-Purpose Flash Plus + PSRAM ComboMemory

SST32HF64A2

Preliminary Specifications

FEATURES:

- **ComboMemories organized as:**
  - SST32HF64A2: 4M x16 Flash + 1024K x16 PSRAM
- **Single 2.7-3.3V Read and Write Operations**
- **Concurrent Operation**
  - Read from or Write to PSRAM while Erase/Program Flash
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption:**
  - Active Current: 15 mA (typical) for Flash or PSRAM Read
  - Standby Current: 60 µA (typical)
- **Flexible Erase Capability**
  - Uniform 2 KWord sectors
  - Uniform 32 KWord size blocks
- **Erase-Suspend/Erase-Resume Capabilities**
- **Security-ID Feature**
  - SST: 128 bits; User: 128 bits
- **Fast Read Access Times:**
  - Flash: 70 ns
  - PSRAM: 70 ns
- **Hardware Block-Protection/WP# Input Pin**
  - Top Block-Protection (top 32 KWord) for SST32HF64A2
- **Latched Address and Data for Flash**
- **Flash Fast Erase and Word-Program:**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 40 ms (typical)
  - Word-Program Time: 7 µs (typical)
- **Flash Automatic Erase and Program Timing**
  - Internal V_{PP} Generation
- **Flash End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Package Available**
  - 56-ball LFBGA (8mm x 10mm x 1.4mm)
  - 64-ball LFBGA (8mm x 10mm x 1.4mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST32HF64A2 ComboMemory device integrates a CMOS flash memory bank with a CMOS PseudoSRAM (PSRAM) memory bank in a Multi-Chip Package (MCP), manufactured with SST proprietary, high-performance SuperFlash technology.

Featuring high-performance Word-Program, the flash memory bank provides a maximum Word-Program time of 7 µsec. To protect against inadvertent flash write, the SST32HF64A2 device contains on-chip hardware and software data protection schemes. The SST32HF64A2 device offers a guaranteed endurance of 10,000 cycles, and data retention greater than 100 years.

The SST32HF64A2 device consists of two independent memory banks, each with enable signals. The flash and PSRAM memory banks are superimposed in the same memory address space, and both banks share common address lines, data lines, WE# and OE#. The memory bank is selected using the memory bank enable signals. The PSRAM bank enable signal, BES1#, selects the PSRAM bank. The flash memory bank enable signal, BEF#, selects the flash memory bank. The WE# signal is used with the Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The SDP command sequence protects the data stored in the flash memory bank from accidental alteration.

The SST32HF64A2 provides the added functionality of being able to simultaneously read from, or write to, the PSRAM bank while erasing or programming in the flash memory bank. The PSRAM memory bank can be read or written while the flash memory bank performs Sector-Erase, Bank-Erase, or Word-Program concurrently. All flash memory Erase and Program operations will automatically latch the input address and data signals and complete the operation in background without further input stimulus required. Once the internally controlled Erase or Program cycle in the flash bank commences, the PSRAM bank can be accessed for Read or Write.

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The SST32HF64A2 device is suited for applications that use both flash memory and PSRAM memory to store code or data, and is ideal for systems requiring low power and small form factor. The SST32HF64A2 significantly improves performance and reliability, while lowering power consumption, when compared with multiple chip solutions. The total energy consumed is a function of the applied voltage, current, and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

Device Operation

The SST32HF64A2 uses BES1#, BES2 and BEF# to control operation of either the flash or the PSRAM memory bank. When BEF# is low, the flash bank is activated for Read, Program or Erase operation. When BES1# is low and BES2 is high, the PSRAM is activated for Read and Write operation. BEF# and BES1# cannot be at low level, and BES2 cannot be at high level at the same time. **If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage.** All address, data, and control lines are shared by flash and PSRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# and BES1# bank enables are raised to V_{IHC} (Logic High) or when BEF# is high and BES2 is low.

Concurrent Read/Write Operation

The SST32HF64A2 provides the unique benefit of being able to read from or write to PSRAM, while simultaneously erasing or programming the flash. This allows data alteration code to be executed from PSRAM, while altering the data in flash. See Figure 28 for a flowchart. The following table lists all valid states.

Concurrent Read/Write State Table

Flash	PSRAM
Program/Erase	Read
Program/Erase	Write

The device will ignore all SDP commands when an Erase or Program operation is in progress. Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Flash Read Operation

The Read operation of the SST32HF64A2 is controlled by BEF# and OE#. Both have to be low, with WE# high, for the system to obtain data from the outputs. BEF# is used for flash memory bank selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to Figure 7 for further details.

Flash Word-Program Operation

The flash memory bank of the SST32HF64A2 is programmed on a word-by-word basis. Before Program operations, the memory must be erased first. The Program operation consists of three steps.

1. Load the three-byte sequence for Software Data Protection.
2. Load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first.
3. Initiate the internal Program operation after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed, within 10 µs. See Figures 8 and 9 for WE# and BEF# controlled Program operation timing diagrams, and Figure 23 for flowcharts.

During the Program operation, the only valid flash Read operations are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. During the command sequence, WP# should be statically held high or low. Any SDP commands loaded during the internal Program operation will be ignored.

Flash Sector/Block-Erase Operation

The SST32HF64A2 offers both Sector-Erase and Block-Erase operations. The Flash Sector/Block-Erase operation erases the device on a sector-by-sector (or block-by-block) basis. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode is based on uniform block size of 32 KWord.

Initiate the Sector-Erase operation by executing a six-byte command sequence with Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The address lines A_{MS}-A_{11} are used to determine the sector address. Initiate the Block-Erase operation by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The address lines A_{MS}-A_{15} are used to determine the block address. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse.

Erase operations begin after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 13 and 14 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored, WP# should be statically held high or low.

Erase-Suspend/Erase-Resume Commands

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation allowing data to be read from any memory location, or programed to any sector/block that is not suspended for an Erase operation. Execute the operation by issuing a one byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode typically within 20 µs after the Erase-Suspend command had been issued.

Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ_2 toggling and DQ_6 at '1'. While in Erase-Suspend mode, a Word-Program operation is allowed except for the sector or block selected for Erase-Suspend.

To resume the Sector-Erase or Block-Erase operation which has been suspended, the system must issue the Erase Resume command. Execute the operation by issuing a one byte command sequence with Erase-Resume command (30H) at any address in the last Byte sequence.

Flash Chip-Erase Operation

The SST32HF64A2 provides a Chip-Erase operation, which allows the user to erase the entire memory array to the '1' state. This is useful when the entire device must be quickly erased.

Initiate the Chip-Erase operation executing a six- byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 6 for the command sequence, Figure 11 for timing diagram, and Figure 27 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Write Operation Status Detection

The SST32HF64A2 provides two software means to detect the completion of a write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. To prevent spurious rejection, in the event of an erroneous result, the software routine must include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

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Flash Data# Polling (DQ_7)

When the SST32HF64A2 flash memory banks are in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is complete, DQ_7 will produce true data. However, even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 µs.

During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is complete, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operation. For Sector- or Block-Erase, the Data# Polling is valid after the rising edge of the sixth WE# (or BEF#) pulse. See Figure 10 for Data# Polling timing diagram and Figure 24 for a flowchart.

Toggle Bits (DQ6 and DQ2)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 bit will alternate between '1' and '0'. When the internal Program or Erase operation is complete, the DQ_6 bit will stop toggling. The device is then ready for the next operation.

For Sector-, Block-, or Chip-Erase, the toggle bit (DQ_6) is valid after the rising edge of sixth WE# (or BEF#) pulse. DQ_6 will be set to '1' if a Read operation is attempted on an Erase-Suspended Sector/Block. If a Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ_6 will toggle.

An additional Toggle Bit is available on DQ_2, which is used in conjunction with DQ_6 to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bits information. The Toggle Bit (DQ_2) is valid after the rising edge of the last WE# (or BEF#) pulse of Write operation. See Figure 11 for Toggle Bit timing diagram and Figure 24 for a flowchart.

TABLE 1: Write Operation Status

Status		DQ_7	DQ_6	DQ_2
Normal Operation	Standard Program	DQ_7#	Toggle	No Toggle
	Standard Erase	0	Toggle	Toggle
Erase-Suspend Mode	Read from Erase-Suspended Sector/Block	1	1	Toggle
	Read from Non- Erase-Suspended Sector/Block	Data	Data	Data
	Program	DQ_7#	Toggle	N/A

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Note: DQ_7 and DQ_2 require a valid address when reading status information.

Flash Memory Data Protection

The SST32HF64A2 flash memory bank provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Flash Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the flash Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST32HF64A2 supports top hardware block protection, which protects the top 32 KWord block of the device. The Boot Block address ranges are described in Table 2.

Program and Erase operations are prevented on the 32 KWord when WP# is low. If WP# is left floating, it is internally held high via a pull-up resistor, and the Boot Block is unprotected, enabling Program and Erase operations on that block.

TABLE 2: Boot Block Address Ranges

Product	Address Range
Top Boot Block	
SST32HF64A2	3F8000H-3FFFFFH

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Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode. When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 18).

The Erase or Program operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity.

Flash Software Data Protection (SDP)

The SST32HF64A2 provides the JEDEC approved software data protection scheme for all flash memory bank data-alteration operations, i.e., Program and Erase. Any Program operation requires a three-byte sequence series.

Using the three byte-load sequence to initiate the Program operation, provides optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires a six-byte load sequence.

The SST32HF64A2 devices are shipped with the software data protection permanently enabled. See Table 6 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode, within T_{RC}. The contents of DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

PSRAM Deep Power-down Mode

The PSRAM Deep Power-down Mode is used to lower the power consumption of the PSRAM in the SST32HF64A2. Deep Power-down occurs 1 µs after being enabled by driving BES2 low. Normal operation occurs 500 µs after driving BES2 high. In Deep Power-down mode, PSRAM data is lost. See Figure 22 for the state diagram.

PSRAM Read

The PSRAM Read operation of the SST32HF64A2 is controlled by OE# and BES1#, both have to be low with WE# and BES2 high for the system to obtain data from the outputs. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 4, for further details.

PSRAM Write

The PSRAM Write operation of the SST32HF64A2 is controlled by WE# and BES1#, both have to be low, BES2 must be high for the system to write to the PSRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES1# or WE#, whichever occurs first. The write time is measured from the last falling edge of BES1# or WE# to the first rising edge of BES1# or WE#. Refer to the Write cycle timing diagrams, Figures 5 and 6, for further details.

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Product Identification

The Product Identification mode identifies the device as the SST32HF64A2 and manufacturer as SST. **This mode is accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers, cannot be used on this device because of the shared lines between flash and PSRAM in the multi-chip package. Therefore, application of high voltage to pin A_9 may damage this device.**

Use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 5 and 6 for software operation, Figure 15 for the software ID entry and read timing diagram and Figure 25 for the ID entry command sequence flowchart.

TABLE 3: Product Identification

	Address	Data
Manufacturer's ID	0000H	BFH
Device ID		
SST32HF64A2	0001H	236CH

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Product Identification Mode Exit/Reset

To return to the standard read mode, the Software Product Identification mode must be exited. Exit by issuing the Exit ID command sequence which returns the device to the Read operation. However, the software reset command is ignored during an internal Program or Erase operation. This command may also be used to reset the device to Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g. not read correctly. See Table 6 for software command codes, Figure 16 for timing waveform and Figure 25 for a flowchart.

Security ID

The SST32HF64A2 device offers a 256-bit Security ID space. The Secure ID space is divided into two 128-bit segments - one factory programmed segment and one user programmed segment. The first segment is programmed and locked at SST with a random 128-bit number. The user segment is left un-programmed for the customer to program as desired.

Use the Security ID Word-Program to program the user segment of the Security ID. To detect end-of-write for the SEC ID, read the toggle bits, not Data# Polling. Once this is complete, the Sec ID is locked using the User Sec ID Program Lock-Out. This disables any future corruption of this space. Regardless of whether or not the Sec ID is locked, neither Sec ID segment can be erased.

The Secure ID space can be queried by executing a three-byte command sequence with Enter Sec ID command (88H) at address 555H in the last byte sequence. To exit this mode, the Exit Sec ID command should be executed. Refer to Table 6 for more details.

Design Considerations

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS}, e.g., less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin.

FUNCTIONAL BLOCK DIAGRAM

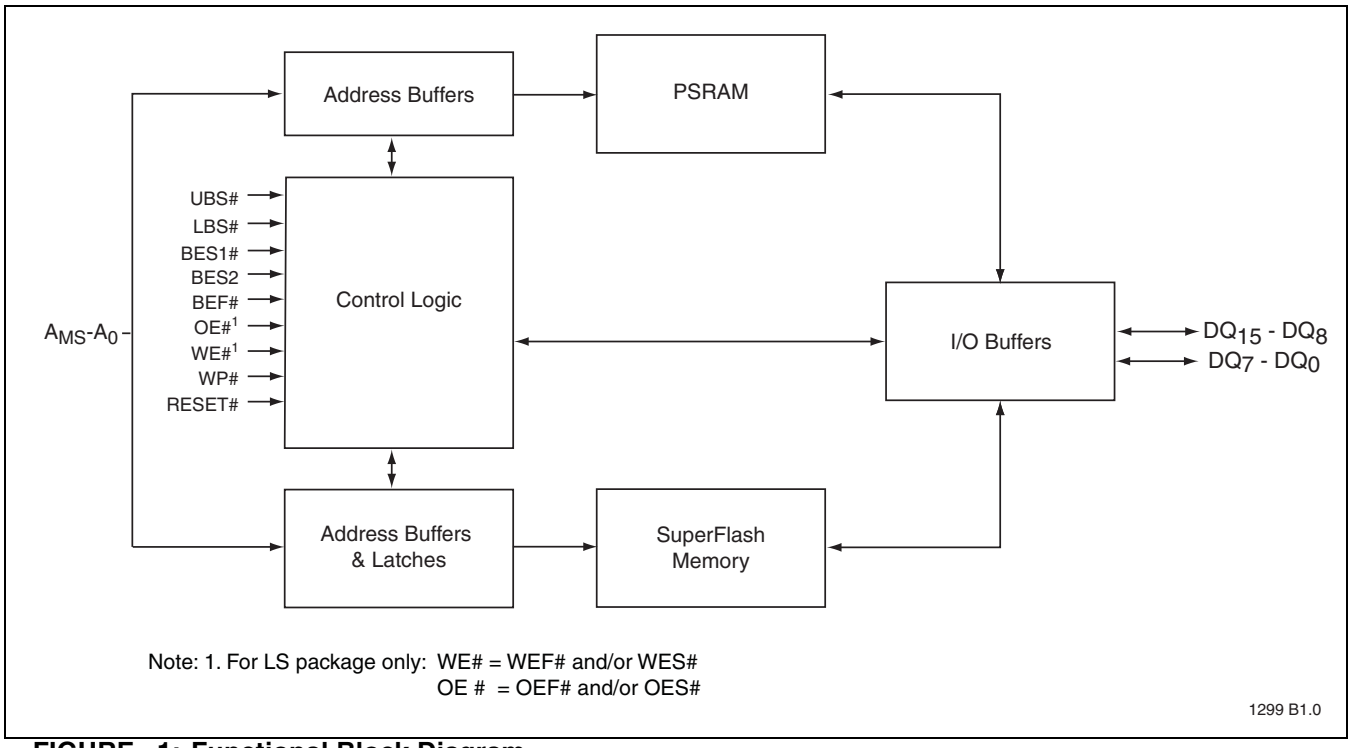

FIGURE 1: Functional Block Diagram

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PIN DESCRIPTION

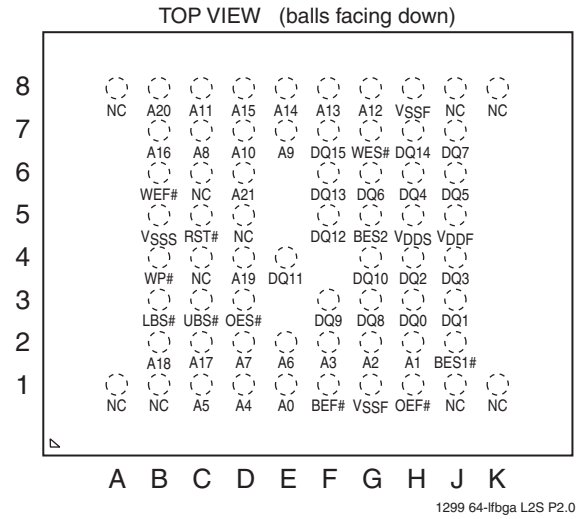

FIGURE 2: Pin Assignments for 64-ball LFBGA (8mm x 10mm)

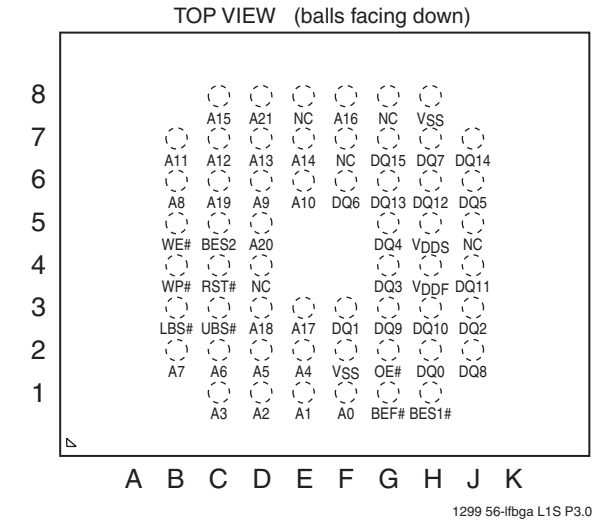

FIGURE 3: Pin Assignments for 56-ball LFBGA (8mm x 10mm)

TABLE 4: Pin Description

Symbol	Pin Name	Functions
A_{MS}[1] to A_0	Address Inputs	To provide flash address, A_{21}-A_0.
A_{MSS}[1] to A_0	Address Inputs	To provide PSRAM address, A_{19}-A_0
DQ_{15}-DQ_0	Data Inputs/Outputs	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE# is high or BES1# is high or BES2 is low and BEF# is high.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low
BES1#	PSRAM Memory Bank Enable	To activate the PSRAM memory bank when BES1# is low
BES2	PSRAM Deep Power-down Enable	To activate the PSRAM memory deep power-down mode when BES2 is V_{IL}
OEF#[2]	Output Enable	To gate the data output buffers for Flash only
OES#[2]	Output Enable	To gate the data output buffers for PSRAM only
WEF#[2]	Write Enable	To control the Write operations for Flash only
WES#[2]	Write Enable	To control the Write operations for PSRAM only
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
UBS#	Upper Byte Control (PSRAM)	To enable DQ_{15}-DQ_8
LBS#	Lower Byte Control (PSRAM)	To enable DQ_7-DQ_0
WP#	Write Protect	To protect and unprotect sectors from Erase or Program operation
RST#	Reset	To Reset and return the device to Read mode
V_{SSF}[2]	Ground	Flash only[2]
V_{SSS}[2]	Ground	PSRAM only[2]
V_{SS}	Ground	
V_{DDF}	Power Supply (Flash)	2.7-3.3V Power Supply to Flash only
V_{DDS}	Power Supply (PSRAM)	2.7-3.3V Power Supply to PSRAM only
NC	No Connection	Unconnected pins

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1. A_{MS} = Most Significant Flash Address
   A_{MSS} = Most Significant PSRAM Address
2. For L2S package only

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TABLE 5: Operational Modes Selection[1]

Mode	BEF#[2]	BES1#[2]	BES2	OE#[3]	WE#[3]	LBS#	UBS#	DQ_{7-0}	DQ_{15-8}
Full Standby	V_{IH}	V_{IH}	V_{IH}	X	X	X	X	HIGH-Z	HIGH-Z
PSRAM Deep Power-down[4]	V_{IH}	V_{IL}	V_{IL}	X	X	X	X	HIGH-Z	HIGH-Z
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	HIGH-Z	HIGH-Z
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	HIGH-Z	HIGH-Z
Flash Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	X	D_{OUT}	D_{OUT}
Flash Write	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	D_{IN}	D_{IN}
Flash Erase	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	X	X
PSRAM Read	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	D_{OUT}	D_{OUT}
						V_{IH}	V_{IL}	HIGH-Z	D_{OUT}
						V_{IL}	V_{IH}	D_{OUT}	HIGH-Z
PSRAM Write	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	D_{IN}	D_{IN}
						V_{IH}	V_{IL}	HIGH-Z	D_{IN}
						V_{IL}	V_{IH}	D_{IN}	HIGH-Z
Product Identification[5]	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	X	X	Manufacturer's ID[6] Device ID[6]	

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1. X can be V_{IL} or V_{IH}, but no other value.
2. For SST32HF64A2, **to avoid bus contention do not apply BEF# = V_{IL} and BES1# = V_{IL} at the same time**
3. OE# = OEF# and OES#
   WE# = WEF# and WES#
4. In PSRAM Deep power-down, PSRAM data is lost.
5. Software mode only
6. With A_{21}-A_1 = 0; SST Manufacturer's ID = 00BFH, is read with A_0=0,
   SST32HF64A2 Device ID = 236CH, is read with A_0=1.

TABLE 6: Software Command Sequence

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Word-Program	555H	AAH	2AAH	55H	555H	A0H	WA[3]	Data				
Sector-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA_X[4]	50H
Block-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA_X[4]	30H
Chip-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Erase-Suspend	XXXXH	B0H										
Erase-Resume	XXXXH	30H										
Query Sec ID[5]	555H	AAH	2AAH	55H	555H	88H						
User Security ID Word-Program	555H	AAH	2AAH	55H	555H	A5H	WA[6]	Data				
User Security ID Program Lock-Out	555H	AAH	2AAH	55H	555H	85H	XXH[6]	0000H				
Software ID Entry[7,8]	555H	AAH	2AAH	55H	555H	90H						
Software ID Exit[9,10] /Sec ID Exit	555H	AAH	2AAH	55H	555H	F0H						
Software ID Exit[9,10] /Sec ID Exit	XXH	F0H										

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1. Address format A_{11}-A_0 (Hex).
   Addresses A_{12}-A_{21} can be V_{IL} or V_{IH}, but no other value, for Command sequence for SST32HF64A2.
2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for Command sequence
3. WA = Program Word address
4. SA_X for Sector-Erase; uses A_{MS}-A_{11} address lines
   BA_X, for Block-Erase; uses A_{MS}-A_{15} address lines
   A_{MS} = Most significant address
   A_{MS} = A_{21} for SST32HF64A2.
5. With A_{MS}-A_4 = 0; Sec ID is read with A_3-A_0,
   SST ID is read with A_3 = 0 (Address range = 000000H to 000007H),
   User ID is read with A_3 = 1 (Address range = 000010H to 000017H).
   Lock Status is read with A_7-A_0 = 0000FFH. Unlocked: DQ_3 = 1 / Locked: DQ_3 = 0.
6. Valid Word-Addresses for Sec ID are from 000000H-000007H and 000010H-000017H.
7. The device does not remain in Software Product ID Mode if powered down.
8. With A_{MS}-A_1 =0; SST Manufacturer ID = 00BFH, is read with A_0 = 0,
   SST32HF64A2 Device ID = 236CH, is read with A_0=1.
   A_{MS} = Most significant address
   A_{MS} = A_{21} for SST32HF64A2.
9. Both Software ID Exit operations are equivalent
10. If users never lock after programming, Sec ID can be programmed over the previously unprogrammed bits (data=1) using the Sec ID mode again (the programmed “0” bits cannot be reversed to “1”). Valid Word-Addresses for Sec ID are from 000000H-000007H and 000010H-000017H.

Preliminary Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}[1]+0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD}[1]+1.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Solder Reflow Temperature . . . . . 260°C for 10 seconds
Output Short Circuit Current[2] . . . . . 50 mA

1. V_{DD} = V_{DDF} and V_{DDS}
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{DD}
Extended	-20°C to +85°C	2.7-3.3V

AC Conditions of Test

Input Rise/Fall Time . . . . . 5 ns
Output Load . . . . . C_L = 30 pF
See Figures 20 and 21

TABLE 7: DC Operating Characteristics (V_{DD} = V_{DDF} and V_{DDS} = 2.7-3.3V)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Active V_{DD} Current				Address input = V_{ILT}/V_{IHT}, at f=5 MHz, V_{DD}=V_{DD} Max, all DQs open
	Read				OE#=V_{IL}, WE#=V_{IH}
	Flash		18	mA	BEF#=V_{IL}, BES1#=V_{IH}, or BES2=V_{IL}
	PSRAM		30	mA	BEF#=V_{IH}, BES1#=V_{IL} , BES2=V_{IH}
	Concurrent Operation		40	mA	BEF#=V_{IH}, BES1#=V_{IL} , BES2=V_{IH}
	Write[1]				WE#=V_{IL}
	Flash		35	mA	BEF#=V_{IL}, BES1#=V_{IH}, or BES2=V_{IL}, OE#=V_{IH}
	PSRAM		30	mA	BEF#=V_{IH}, BES1#=V_{IL} , BES2=V_{IH}
I_{SB}	Standby V_{DD} Current		135	µA	V_{DD} = V_{DD} Max, BEF#=BES1#=V_{IHC}, BES2=V_{IHC}
I_{SBP}	Deep Power Down: PSRAM		10	µA	BES2=V_{ILC}, BEF#=V_{IHC}
I_{RT}	Reset V_{DD} Current		30	µA	Reset=V_{SS}±0.3V
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage		0.8	V	V_{DD}=V_{DD} Min
V_{ILC}	Input Low Voltage (CMOS)		0.2	V	V_{DD}=V_{DD} Max
V_{IH}	Input High Voltage	0.7 V_{DD}		V	V_{DD}=V_{DD} Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	V_{DD}=V_{DD} Max
V_{OLF}	Flash Output Low Voltage		0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OHF}	Flash Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min
V_{OLS}	PSRAM Output Low Voltage		0.4	V	I_{OL} =1 mA, V_{DD}=V_{DD} Min
V_{OHS}	PSRAM Output High Voltage	2.2		V	I_{OL} =-500 µA, V_{DD}=V_{DD} Min

T7.0 1299

1. I_{DD} active while Erase or Program is in progress.

Preliminary Specifications

TABLE 8: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Program/Erase Operation	100	µs

T8.0 1299

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: Capacitance (T_A = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	12 pF

T9.0 1299

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: Flash Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T10.0 1299

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 11: PSRAM Read Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{RCS}	Read Cycle Time	70		ns
T_{AAS}	Address Access Time		70	ns
T_{BES}	Bank Enable Access Time		70	ns
T_{OES}	Output Enable Access Time		35	ns
T_{BYES}	UBS#, LBS# Access Time		70	ns
T_{BLZS}[1]	BES1# to Active Output	0		ns
T_{OLZS}[1]	Output Enable to Active Output	0		ns
T_{BYLZS}[1]	UBS#, LBS# to Active Output	0		ns
T_{BHZS}[1]	BES1# to High-Z Output		25	ns
T_{OHZS}[1]	Output Disable to High-Z Output	0	25	ns
T_{BYHZS}[1]	UBS#, LBS# to High-Z Output		35	ns
T_{OHS}	Output Hold from Address Change	10		ns

T11.0 1299

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: PSRAM Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{WCS}	Write Cycle Time	70		ns
T_{BWS}	Bank Enable to End-of-Write	60		ns
T_{AWS}	Address Valid to End-of-Write	60		ns
T_{ASTS}	Address Set-up Time	0		ns
T_{WPS}	Write Pulse Width	60		ns
T_{WRS}	Write Recovery Time	0		ns
T_{BYWS}	UBS#, LBS# to End-of-Write	60		ns
T_{ODWS}	Output Disable from WE# Low		30	ns
T_{OEWS}	Output Enable from WE# High	0		ns
T_{DSS}	Data Set-up Time	30		ns
T_{DHS}	Data Hold from Write Time	0		ns

T12.0 1299

Preliminary Specifications

TABLE 13: Flash Read Cycle Timing Parameters V_{DD} = 2.7-3.6V

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{CLZ}[1]	BEF# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	BEF# High to High-Z Output		20	ns
T_{OHZ}[1]	OE# High to High-Z Output		20	ns
T_{OH}[1]	Output Hold from Address Change	0		ns
T_{RP}[1]	RST# Pulse Width	500		ns
T_{RHR}[1]	RST# High before Read	50		ns
T_{RY}[1,2]	RST# Pin Low to Read Mode		20	µs

T13.0 1299

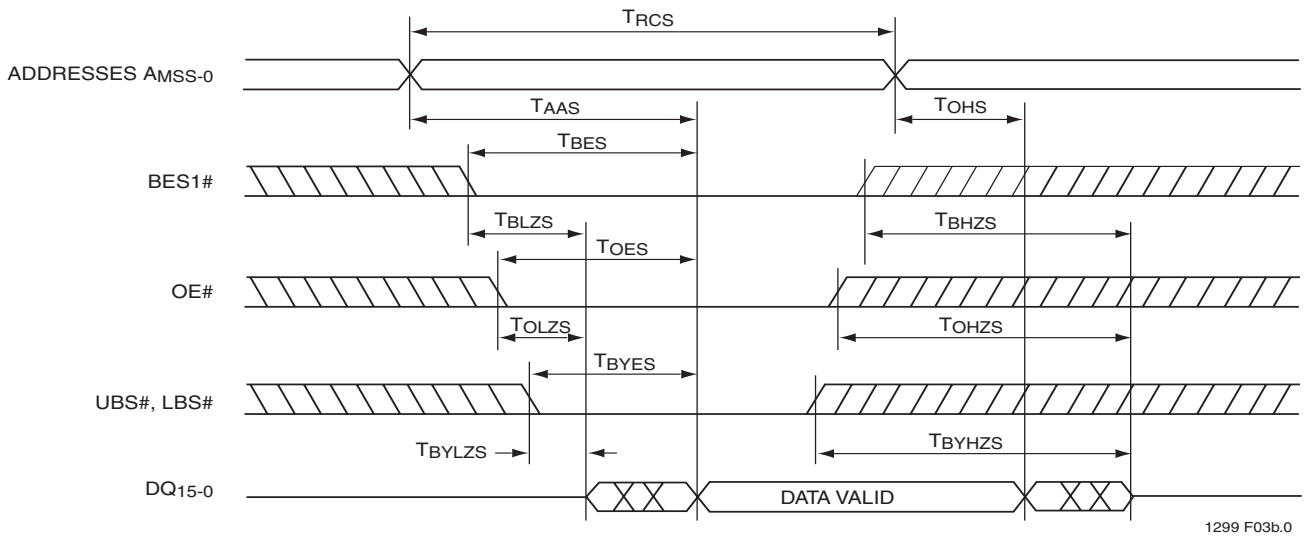
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. This parameter applies to Sector-Erase, Block-Erase and Program operations.
   This parameter does not apply to Chip-Erase operations.

TABLE 14: Flash Program/Erase Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		10	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and BEF# Setup Time	0		ns
T_{CH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms

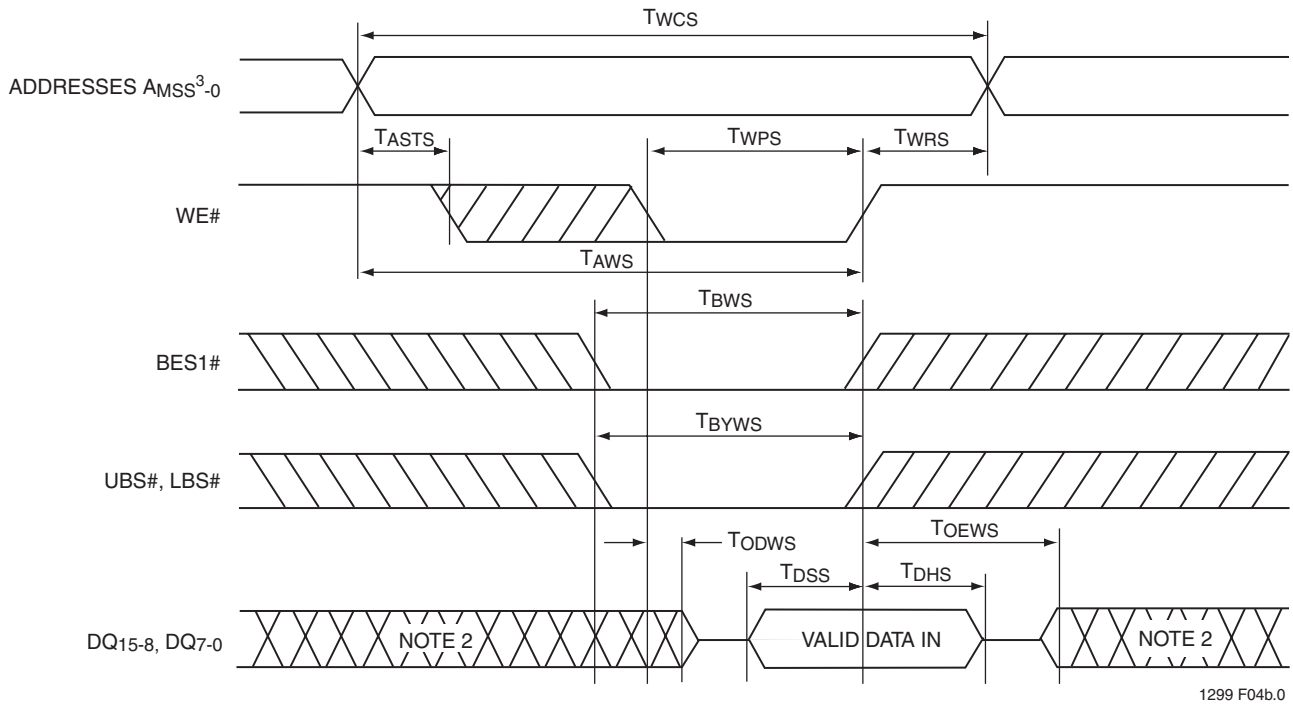
T14.0 1299

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



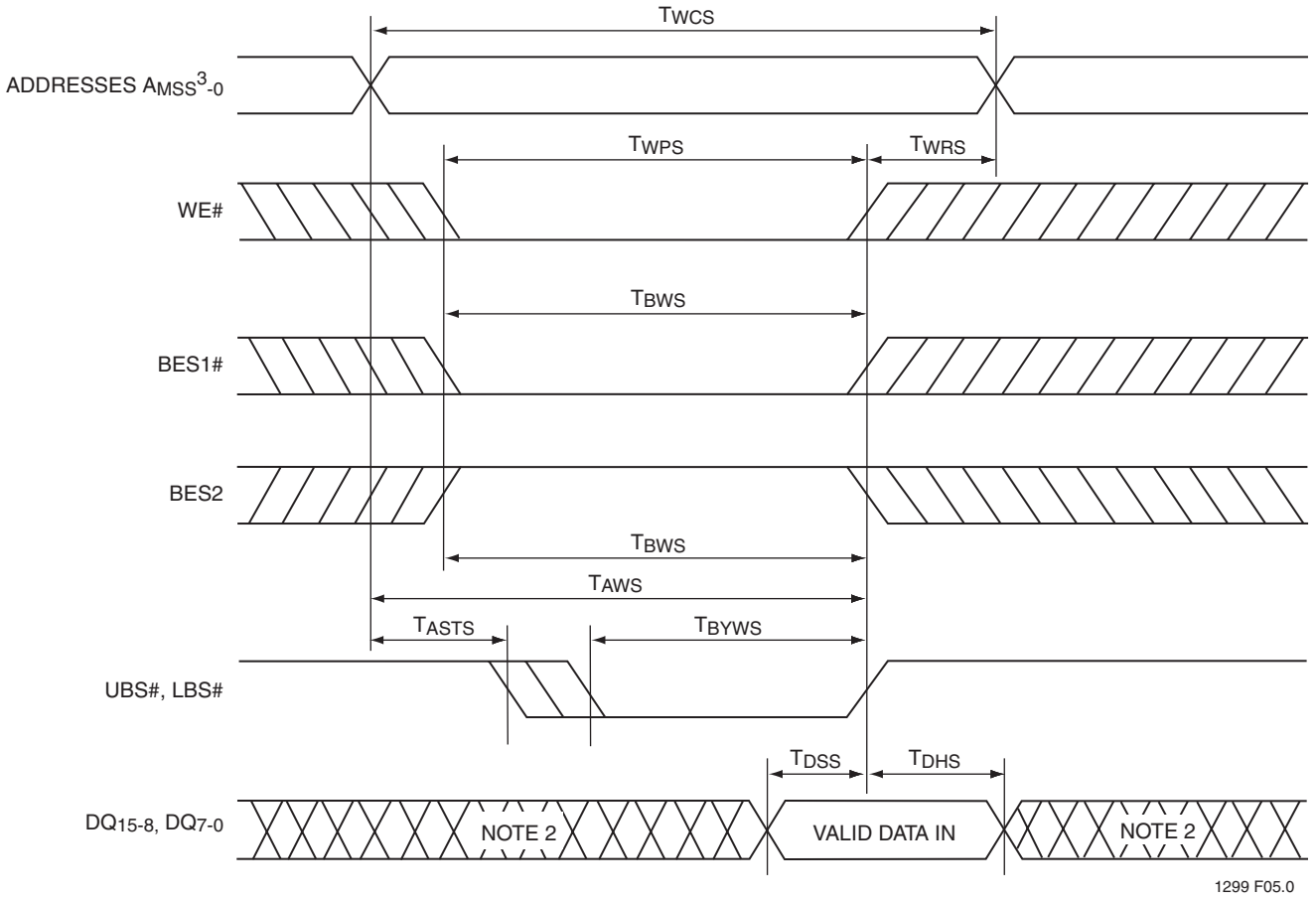
Note: A_{MSS} = Most Significant PSRAM Address
$A_{MSS} = A_{19}$ for SST32HF64A2

FIGURE 4: PSRAM Read Cycle Timing Diagram for SST32HF64A2



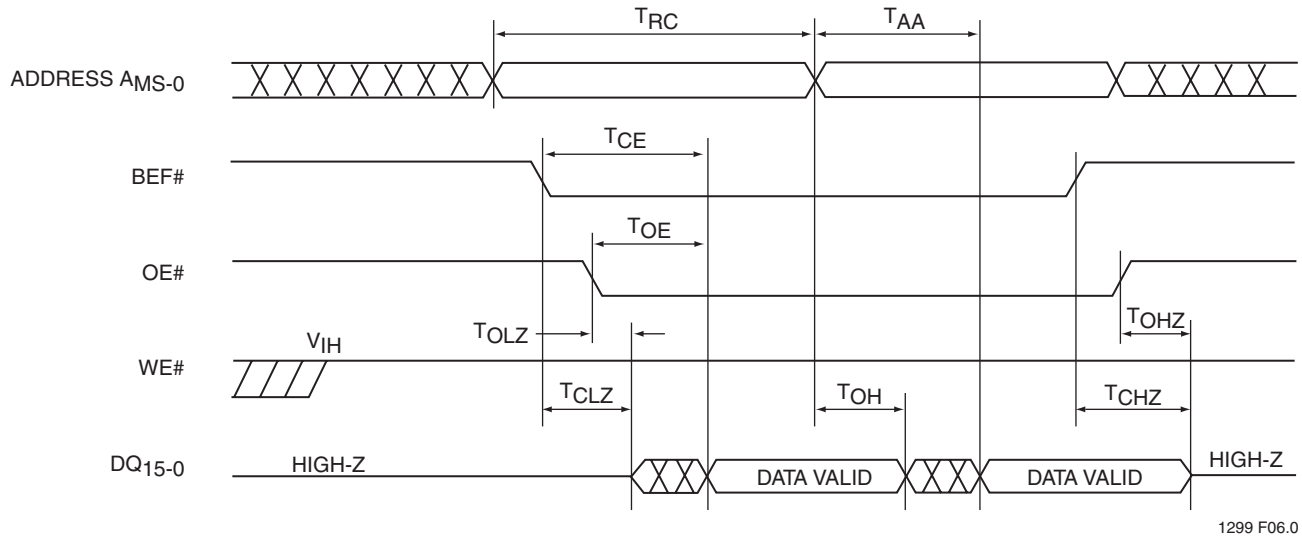
Note: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES1# goes Low coincident with or after WE# goes Low, the output will remain at high impedance.
If BES1# goes High coincident with or before WE# goes High, the output will remain at high impedance.
Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. A_{MSS} = Most Significant PSRAM Address
$A_{MSS} = A_{19}$ for SST32HF64A2

FIGURE 5: PSRAM Write Cycle Timing Diagram for SST32HF64A2 (WE# Controlled)[1]



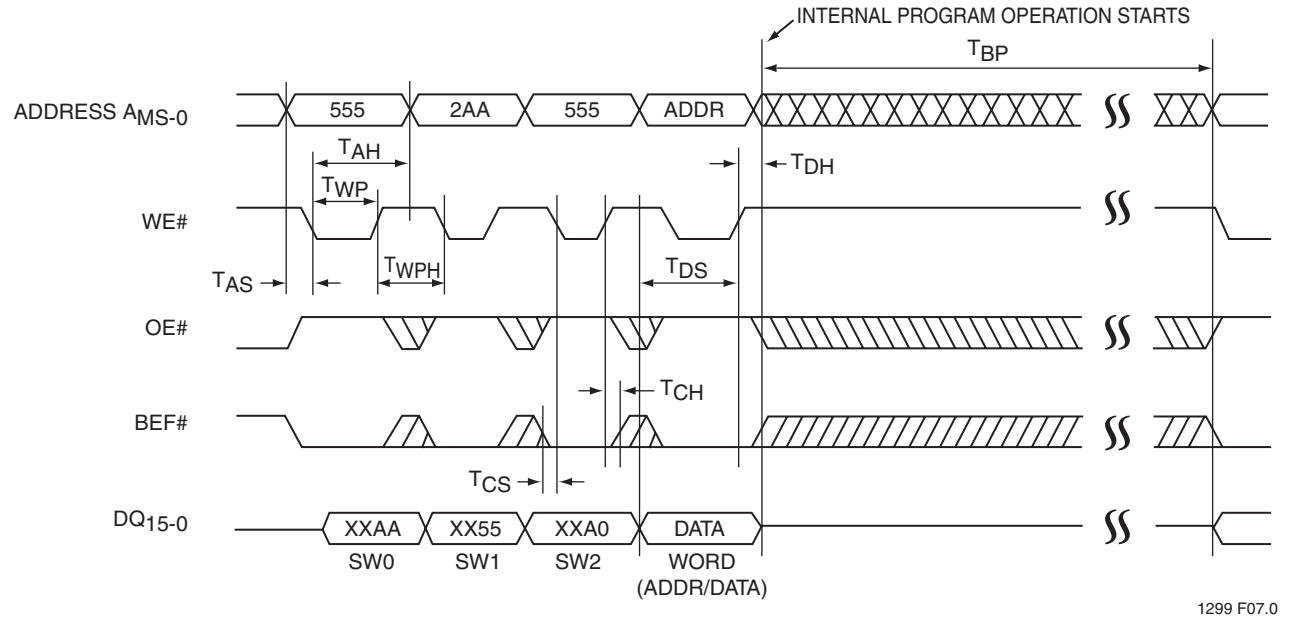
Note: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. A_{MSS} = Most Significant PSRAM Address
A_{MSS} = A_{19} for SST32HF64A2

FIGURE 6: PSRAM Write Cycle Timing Diagram (UBS#, LBS# Controlled)[1]



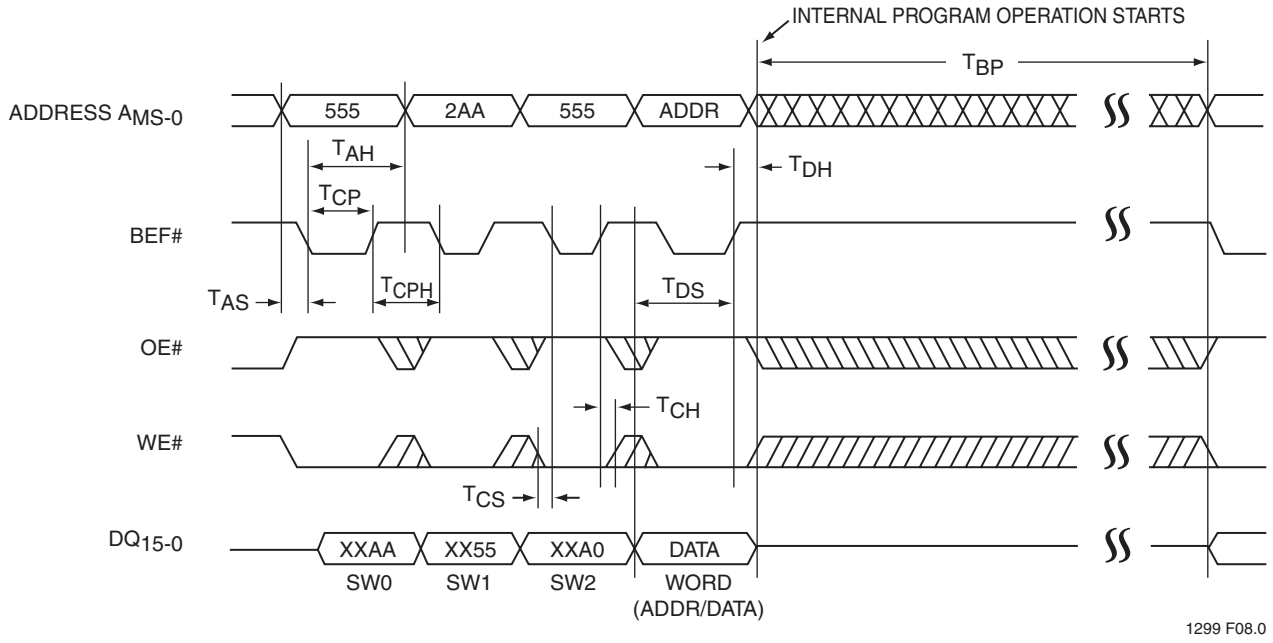
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2

FIGURE 7: Flash Read Cycle Timing Diagram



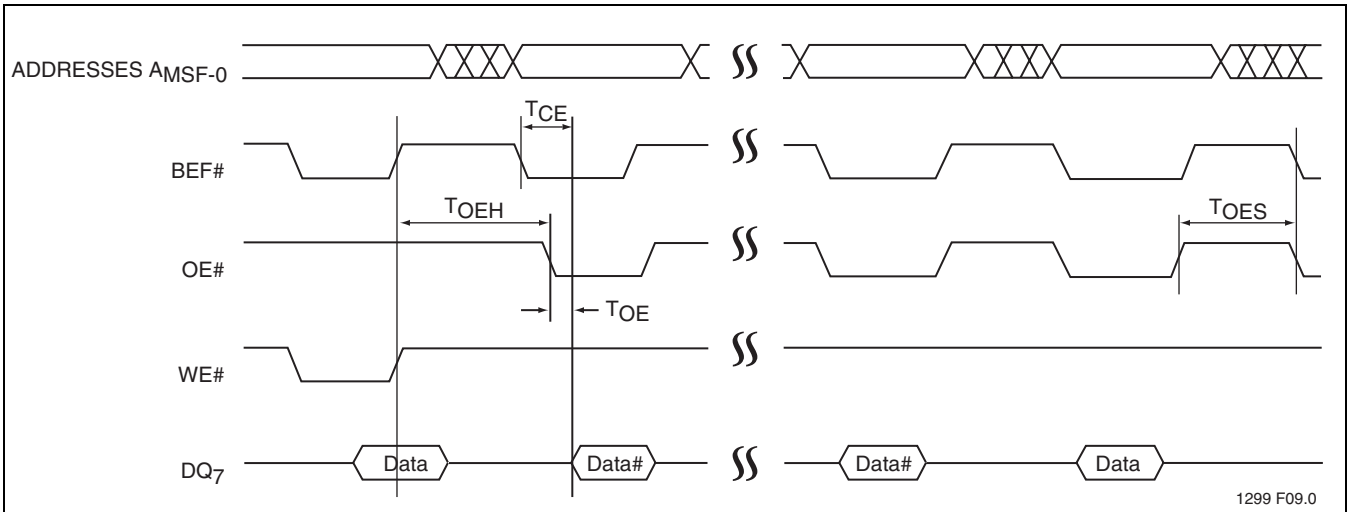
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence
X can be V_{IL} or V_{IH}, but no other value

FIGURE 8: Flash WE# Controlled Program Cycle Timing Diagram



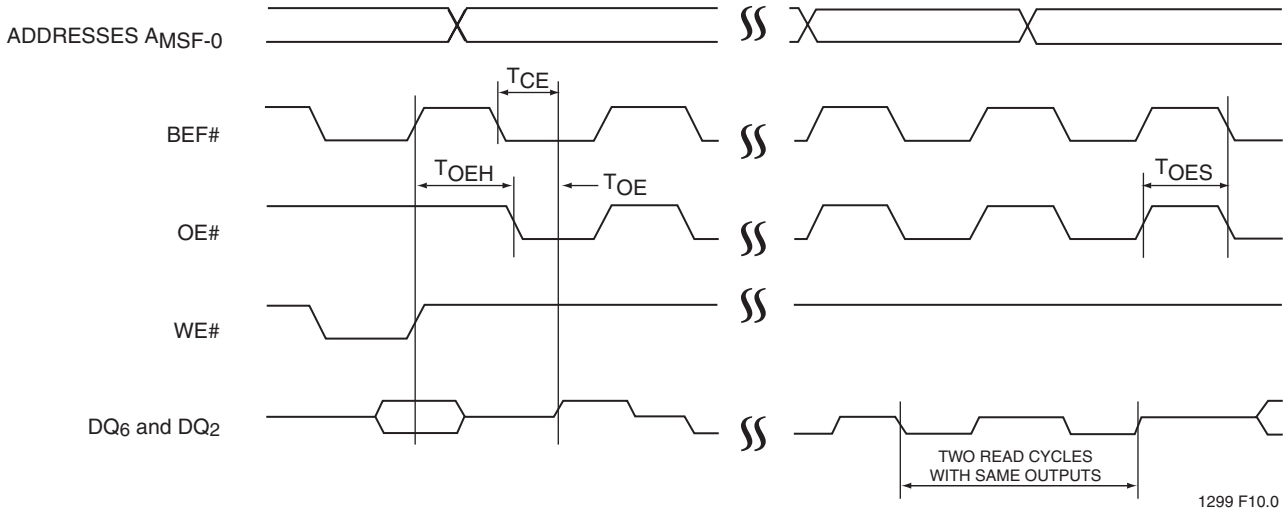
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence
X can be V_{IL} or $V_{IH,}$ but no other value

FIGURE 9: BEF# Controlled Flash Program Cycle Timing Diagram



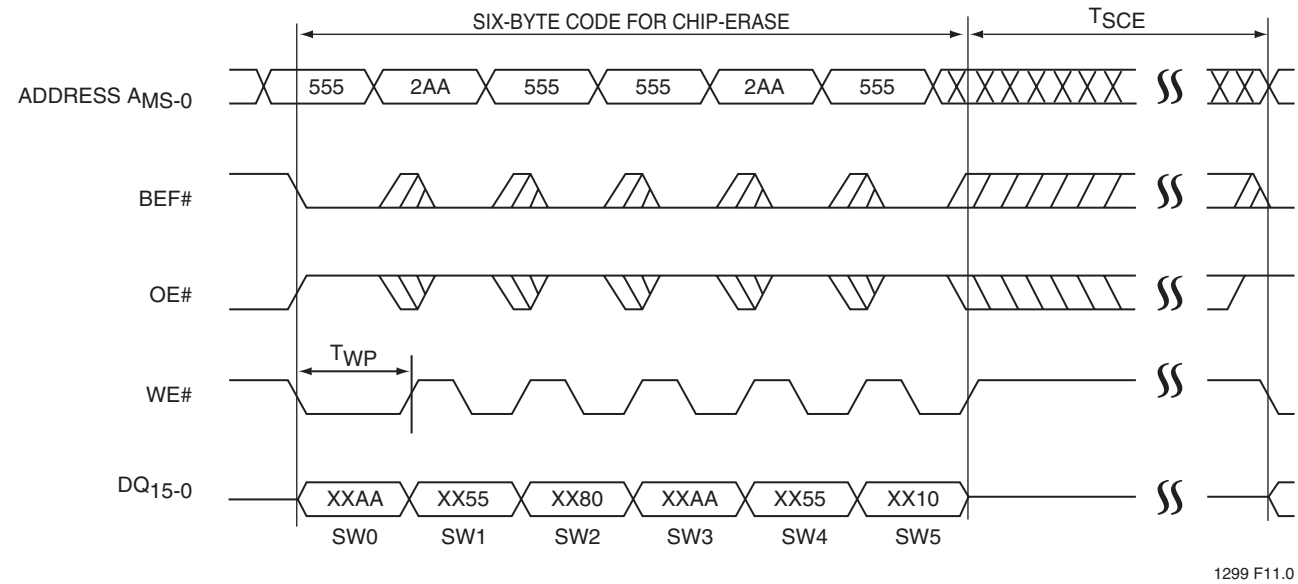
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2

FIGURE 10: Flash Data# Polling Timing Diagram



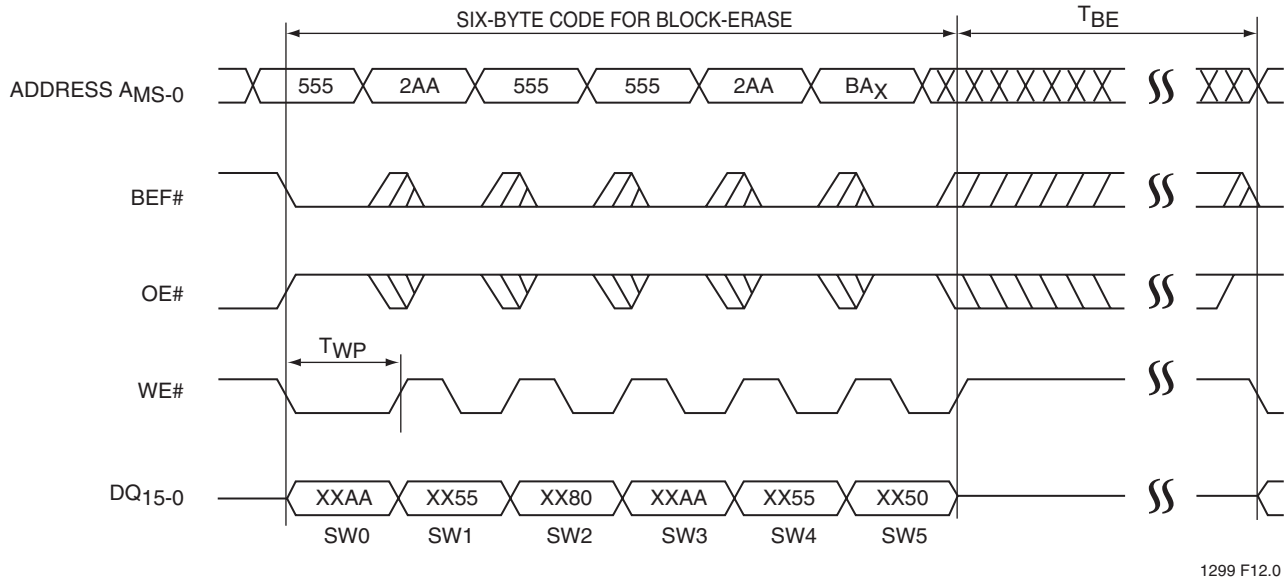
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2

FIGURE 11: Flash Toggle Bit Timing Diagram



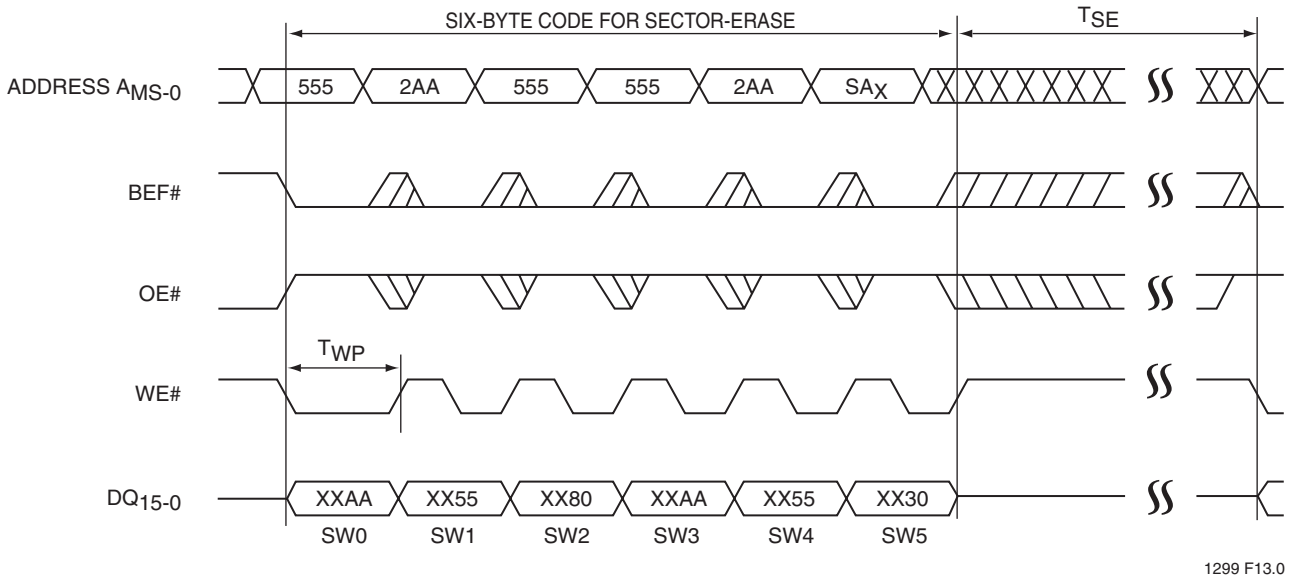
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence
This device also supports BEF# controlled Chip-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are meet. (See Table 14)
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 12: WE# Controlled Flash Chip-Erase Timing Diagram



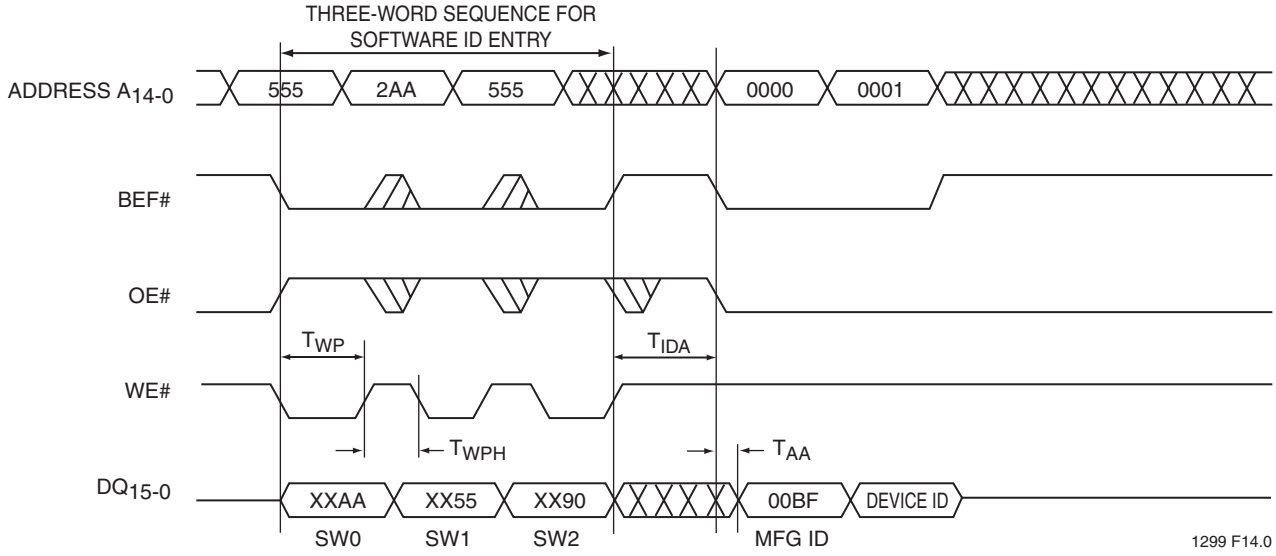
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2
This device also supports BEF# controlled Block-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are meet. (See Table 14.)
BA_X = Block Address
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence
X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 13: WE# Controlled Flash Block-Erase Timing Diagram



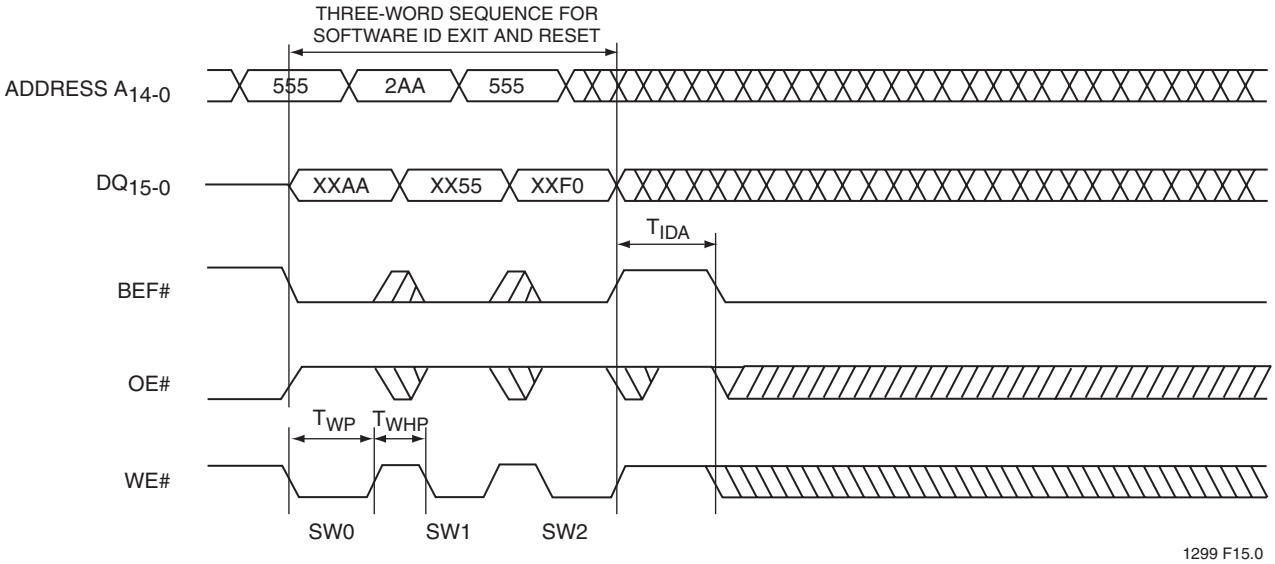
Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2
This device also supports BEF# controlled Sector-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are meet. (See Table 14.)
SA_X = Sector Address
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence
X can be V_{IL} or V_{IH}, but no other value.

FIGURE 14: WE# Controlled Flash Sector-Erase Timing Diagram



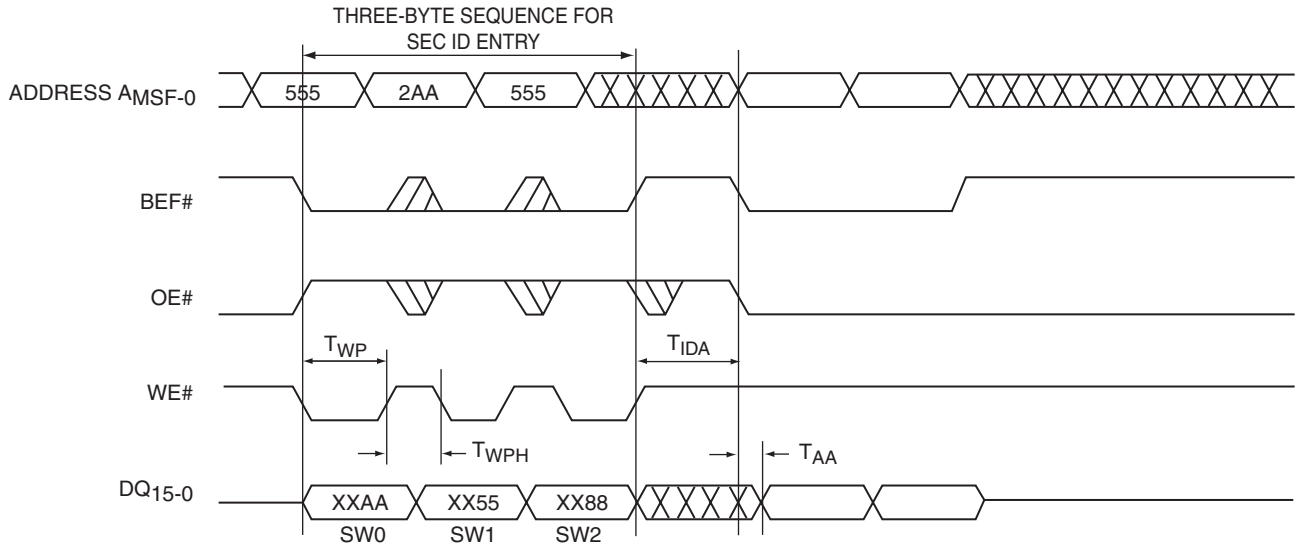
Note: X can be V_{IL} or $V_{IH,}$ but no other value.
Device ID - See Table 3 on page 6

FIGURE 15: Software ID Entry and Read



Note: X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 16: Software ID Exit and Reset



Note: A_{MS} = Most Significant Flash Address
$A_{MS} = A_{21}$ for SST32HF64A2
WP# must be held in proper logic state (V_{IL} or V_{IH}) 1 µs prior to and 1 µs after the command sequence.
X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 17: Flash Sec ID Entry

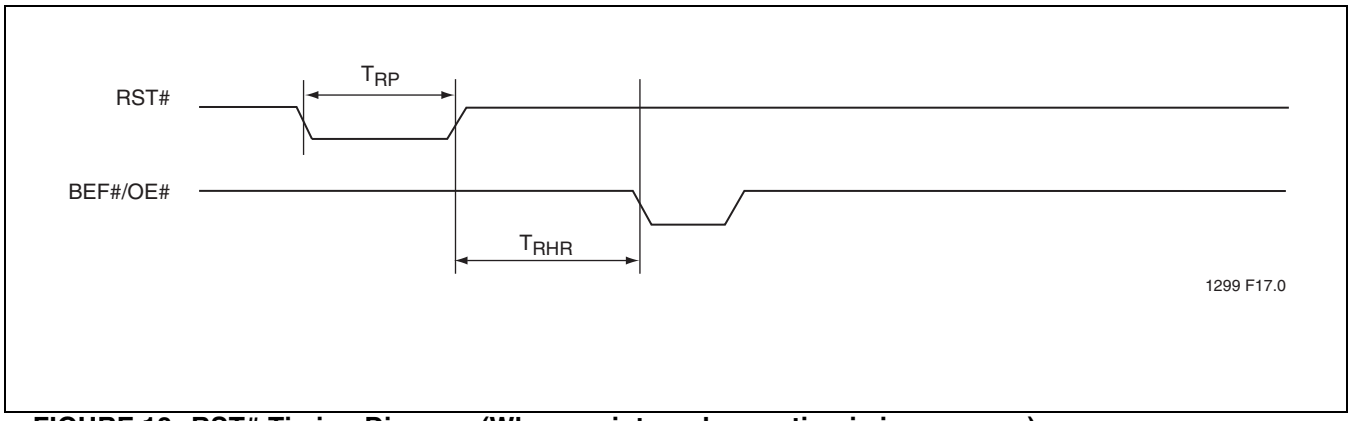


FIGURE 18: RST# Timing Diagram (When no internal operation is in progress)

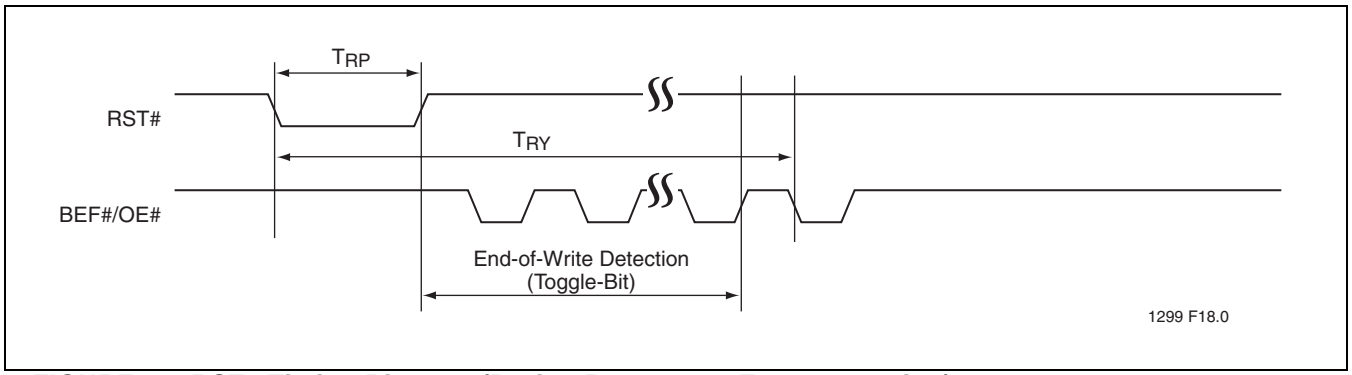
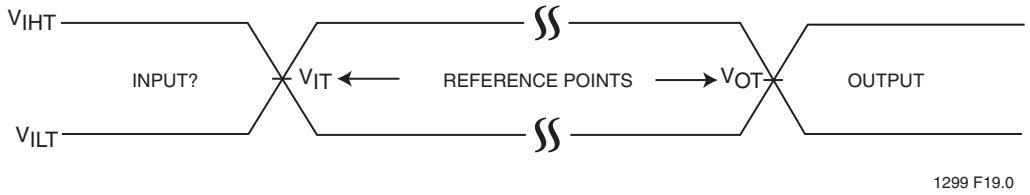


FIGURE 19: RST# Timing Diagram (During Program or Erase operation)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 20: AC Input/Output Reference Waveforms

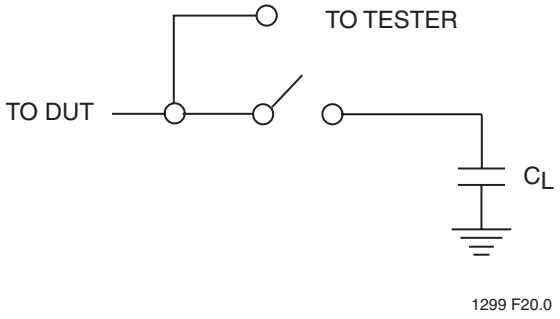


FIGURE 21: A Test Load Example

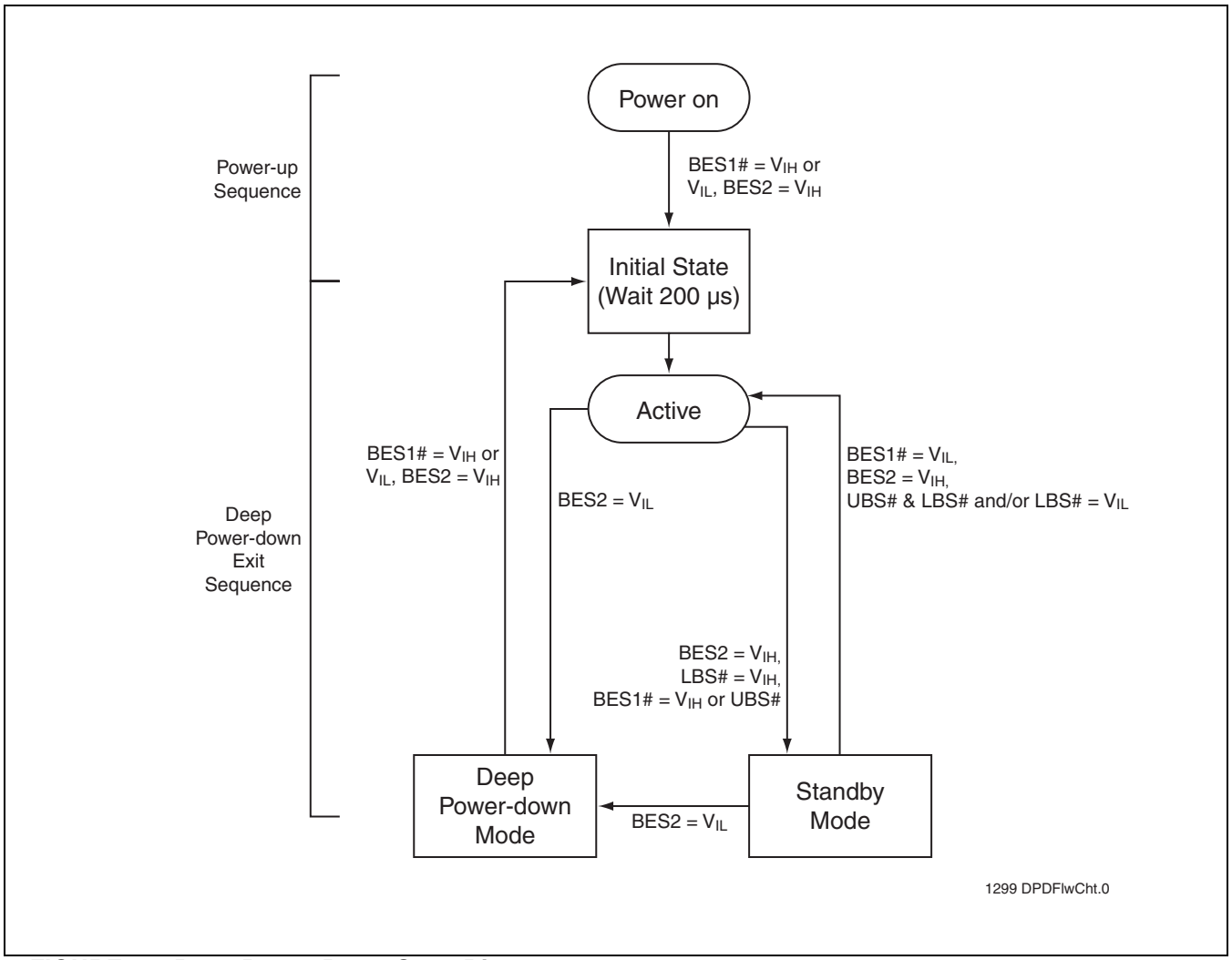
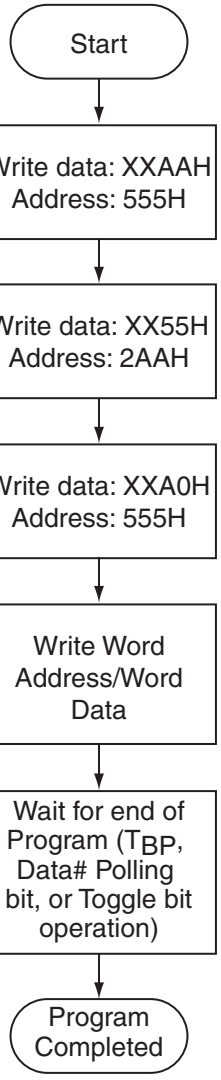


FIGURE 22: Deep Power-Down State Diagram



Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 23: Word-Program Algorithm

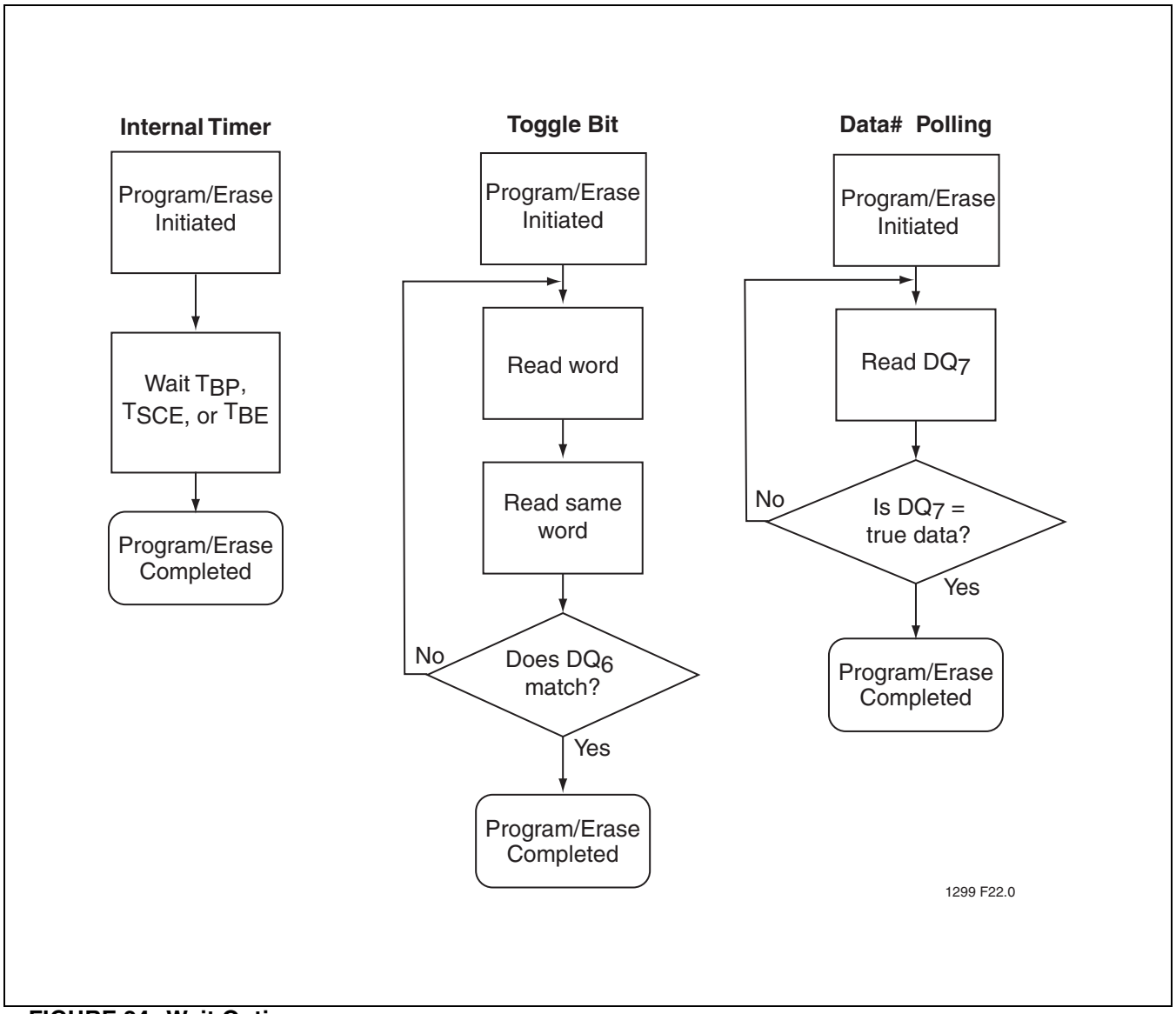


FIGURE 24: Wait Options

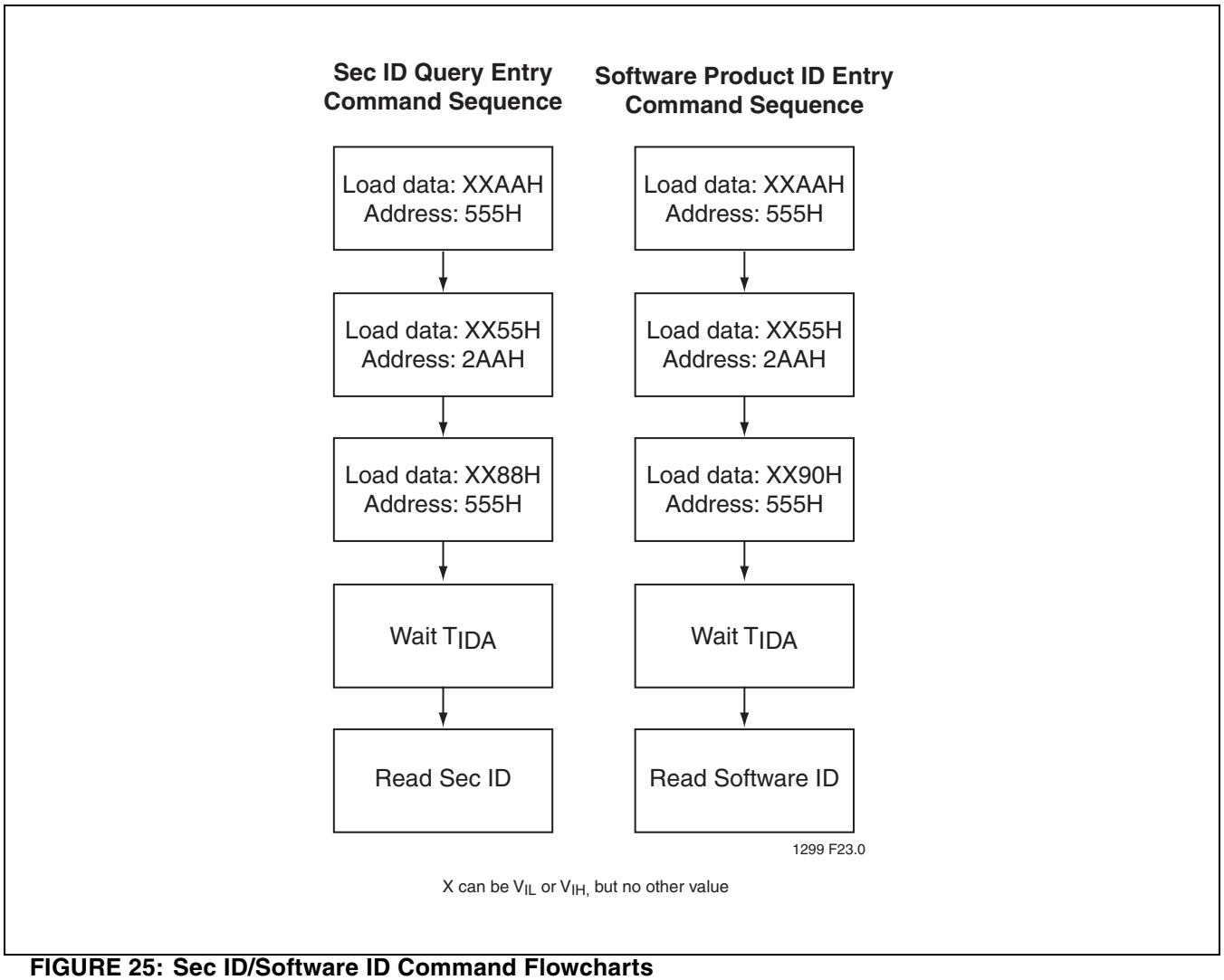


FIGURE 25: Sec ID/Software ID Command Flowcharts

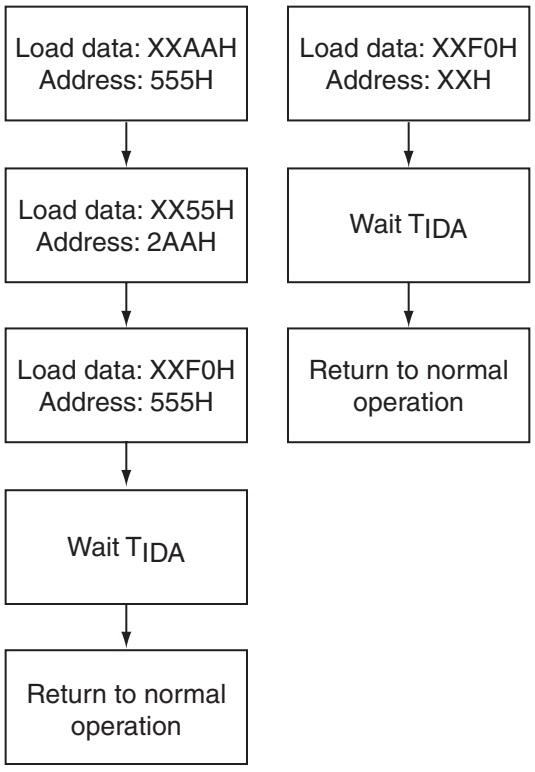
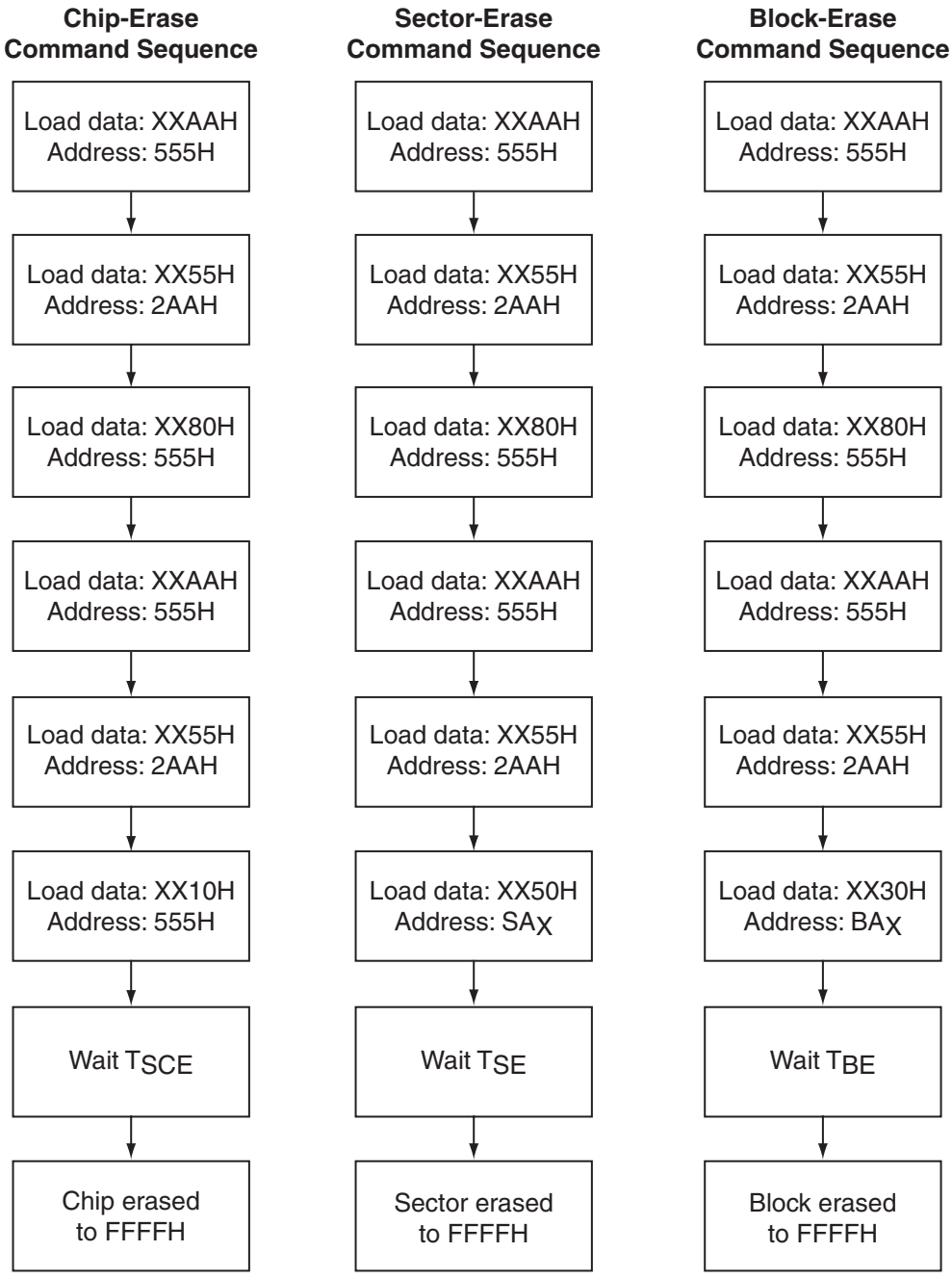


FIGURE 26: Software ID/Sec ID Command Flowcharts



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 27: Erase Command Sequence

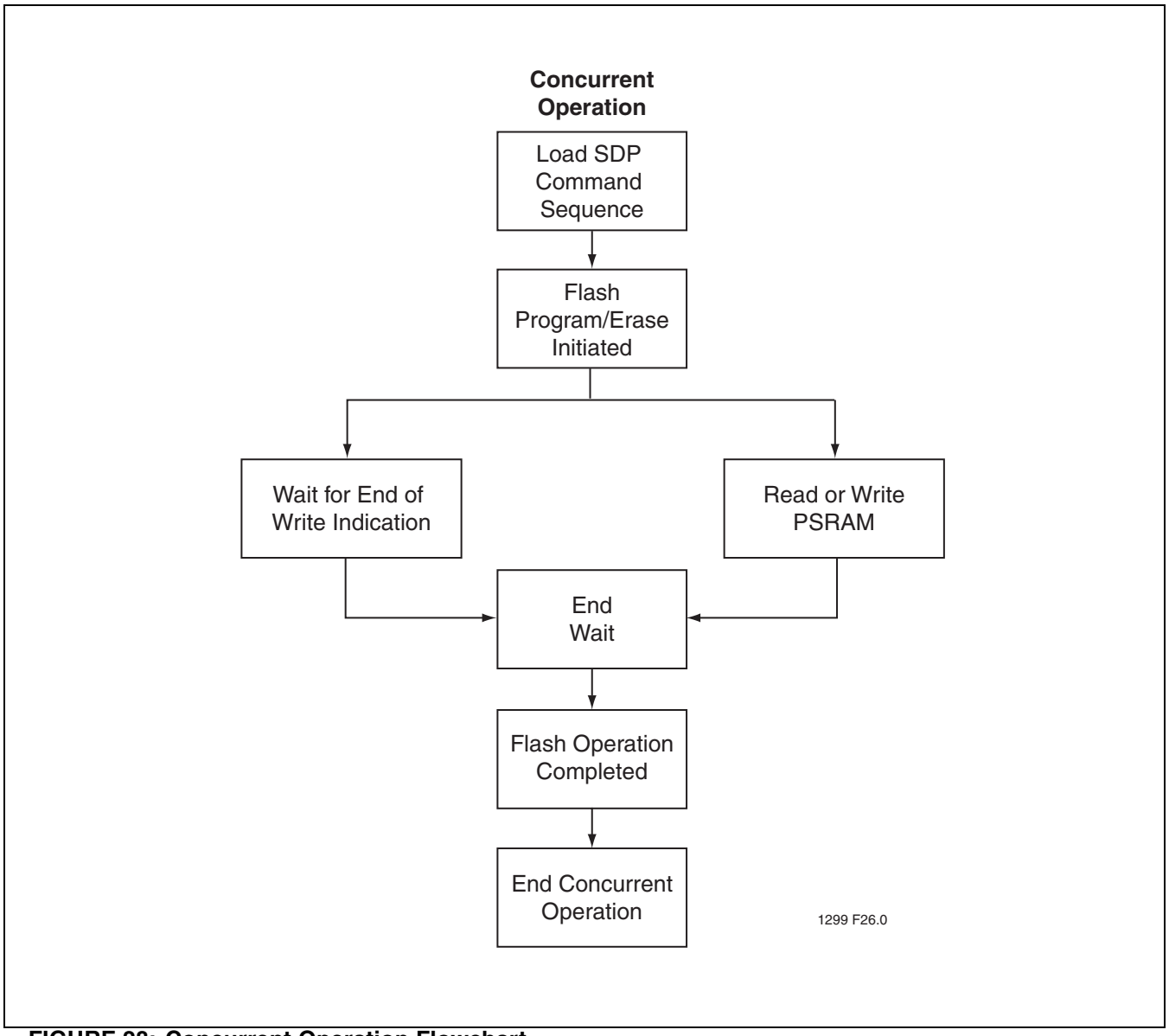
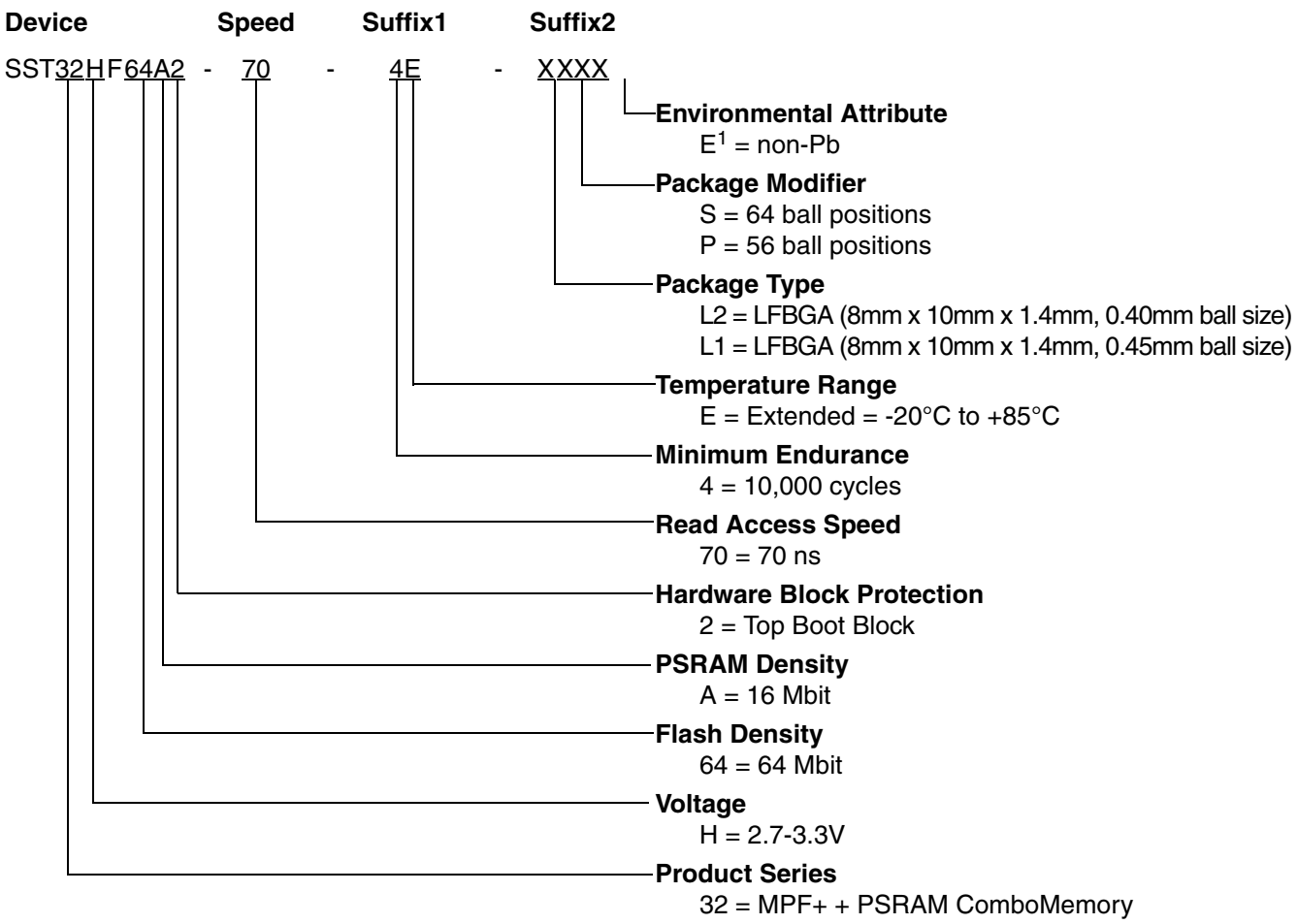


FIGURE 28: Concurrent Operation Flowchart

Preliminary Specifications

PRODUCT ORDERING INFORMATION



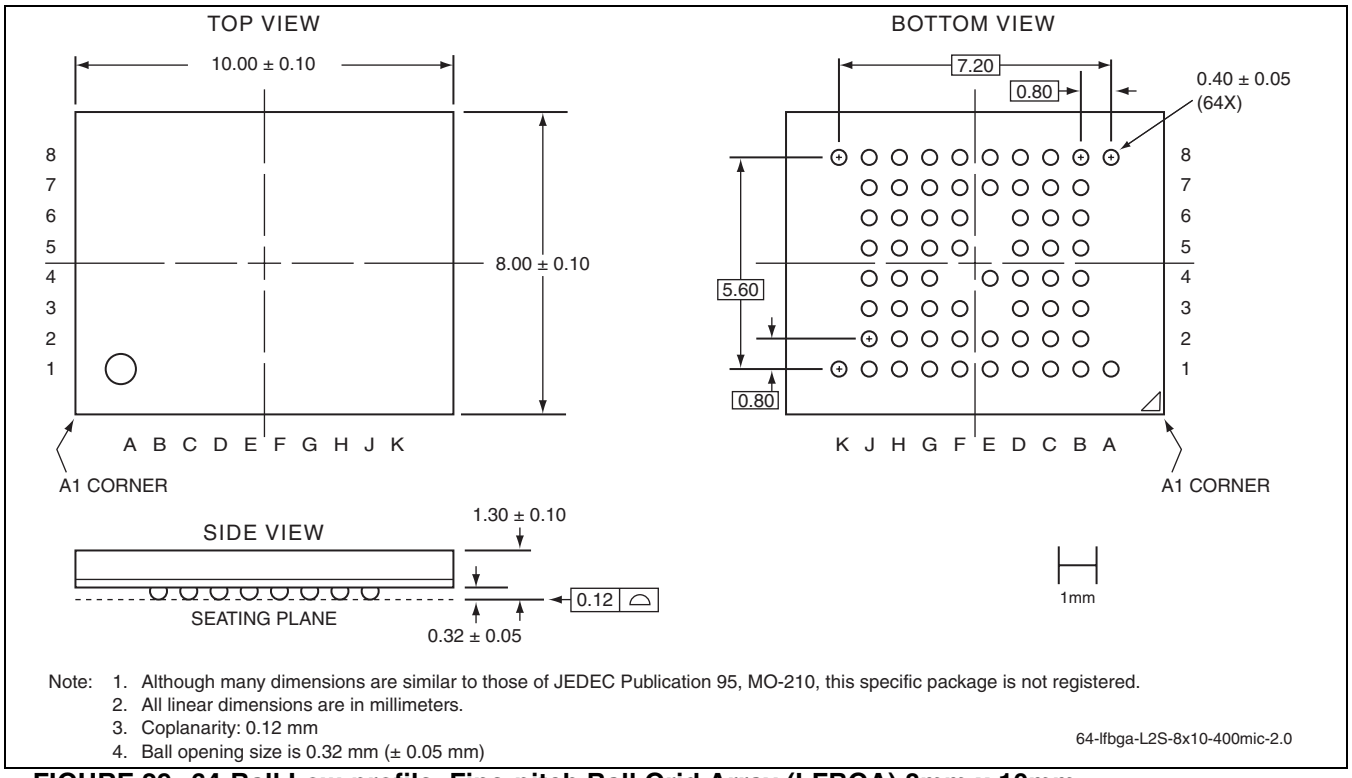
1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST32HF64A2

SST32HF64A2-70-4E-L2SE
SST32HF64A2-70-4E-L1PE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

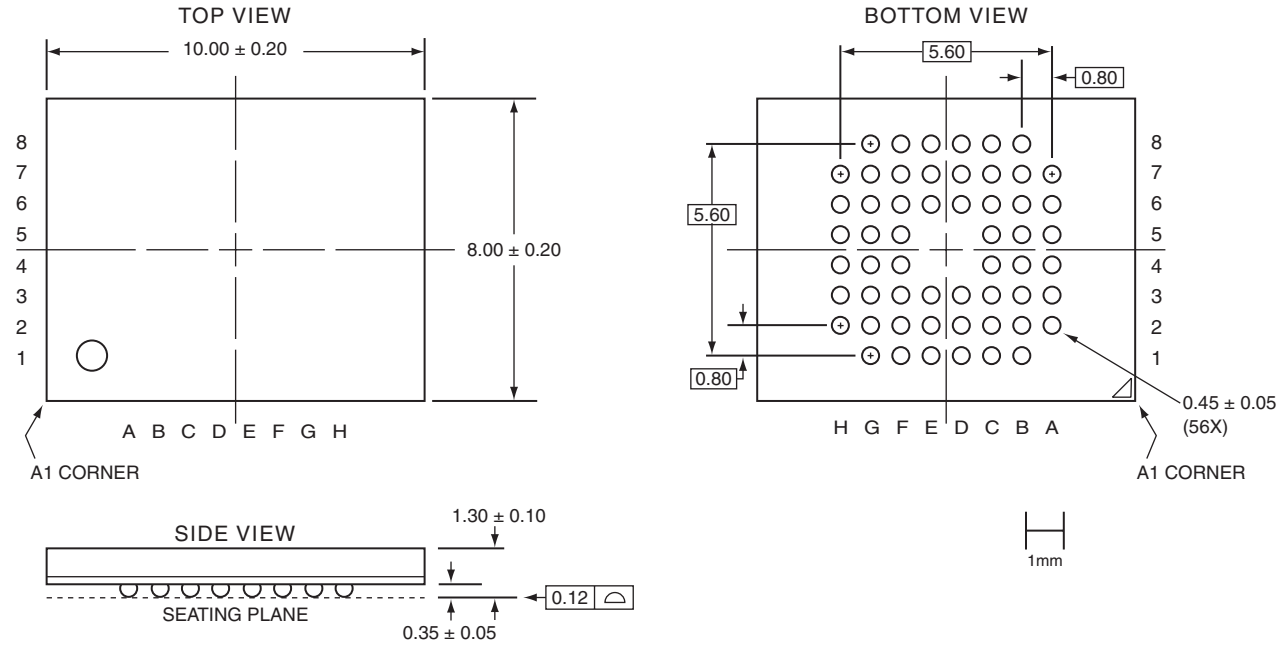
PACKAGING DIAGRAMS



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.32 mm (± 0.05 mm)

64-lfbga-L2S-8x10-400mic-2.0

FIGURE 29: 64-Ball Low-profile, Fine-pitch Ball Grid Array (LFBGA) 8mm x 10mm
SST Package Code: L2S



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

56-lfbga-L1P-8x10-450mic-4

FIGURE 30: 56-Ball Low-profile, Fine-pitch Ball Grid Array (LFBGA) 8mm x 10mm
SST Package Code: L1P

TABLE 15: Revision History

Number	Description	Date
00	• Initial Release of S71299 • Includes 64 MB devices and extended temperature MPNs previously released in data sheets S71260 and S71261 • Removed 63-Ball Low-Profile, Fine-Pitch Ball Grid Array (LFBGA) 8mm x 10mm	Dec 2005
01	• Changed I_{SB} max limits to 135 µA in DC Operating Characteristics Table 7 page 13	Apr 2006
02	• Removed SST32HF64A1, SST32HF64B1, and SST32HF64B2 (These part numbers were never produced.) • Added 56-Ball Low-Profile, Fine-Pitch Ball Grid Array (LFBGA) 8mm x10mm • Revised A_{MS} to A_0 and A_{MSS} to A_0 in Pin Assignment Table 4 • Edited Note 1 for Pin Assignment Table 4	Nov 2006