

STD40NF03L

N-channel 30V - 0.0090Ω - 40A - DPAK Low gate charge STripFET™ II Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	I _D
STD40NF03L	30V	<0.011Ω	40A

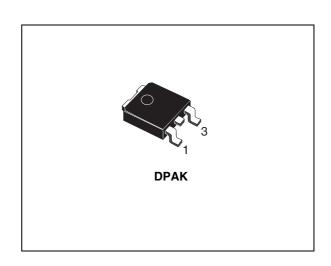
- Logic level device
- Optimal R_{DS(on)} x Q_g trade-off
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive

Description

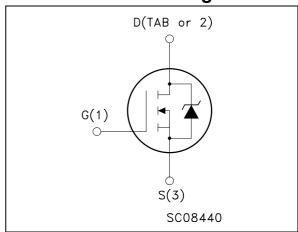
This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

Applications

■ Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging	
STD40NF03LT4	D40NF03L	DPAK	Tape & reel	

Contents STD40NF03L

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STD40NF03L Electrical ratings

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit	
V _{DS}	Drain-source voltage (V _{GS} = 0)	30	V	
V _{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	30	V	
V _{GS}	Gate- source voltage	± 20	V	
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25°C	40	Α	
I _D	Drain current (continuous) at T _C = 100°C	28	А	
I _{DM} ⁽²⁾	Drain current (pulsed)	160	Α	
P _{tot} Total dissipation at T _C = 25°C		80	W	
	Derating Factor		W/°C	
dv/dt (3)	Peak diode recovery voltage slope	5.5	V/ns	
E _{AS} (4)	Single pulse avalanche energy	850	mJ	
T _{stg}	Storage temperature	-55 to 175	°C	
Tj	Max. operating junction temperature	-55 to 175	C	

- 1. Current limited by package
- 2. Pulse width limited by safe operating area.
- 3. I_{SD} 40A, di/dt \$50A/ μ s, $V_{DD} \le V_{(BR)DSS}$, $T_j \le T_{JMAX}$
- 4. Starting $T_i = 25$ °C, $I_D = 20A$, $V_{DD} = 25V$

Table 2. Thermal data

Rthj-case	-case Thermal resistance junction-case max		°C/W
Rthj-amb Thermal resistance junction-ambient max		100	°C/W
T _J Maximum lead temperature for soldering purpose		300	°C

Electrical characteristics STD40NF03L

2 Electrical characteristics

(T_{CASE} =25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_{C} = 125°C			1 10	μ Α μ Α
I _{GSS} Gate-body leakage current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA	
V _{GS(th)} Gate threshold voltage		$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1			٧
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10V, I_D = 20A$ $V_{GS} = 5V, I_D = 10A$		0.0090 0.0150	0.0110 0.0195	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs} (1)	Forward transconductance	$V_{DS} = 15V_{,} I_{D} = 20A$		23		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		1440 560 135		pF pF pF
$\begin{array}{c} t_{\text{d(on)}} \\ t_{\text{r}} \\ t_{\text{d(off)}} \\ t_{\text{f}} \end{array}$	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 15V, I_D = 20A R_G = 4.7 Ω V_{GS} = 5V (see <i>Figure 13</i>)		22 165 21 25		ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 15V, I_D = 40A, V_{GS} = 5V, R_G = 4.7 Ω (see <i>Figure 14</i>)		22.5 9 12	30	nC nC nC

^{1.} Pulsed: Pulse duration = 300 μs, duty cycle 1.5%.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current Source-drain current (pulsed)				40 160	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 20A, V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40A, di/dt = 100A/µs, V_{DD} = 20V, T_j = 150°C (see <i>Figure 15</i>)		42 52 2.5		ns nC A

^{1.} Pulse width limited by safe operating area.

^{2.} Pulsed: Pulse duration = 300 μ s, duty cycle 1.5%

Electrical characteristics STD40NF03L

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

Figure 2. Thermal impedance

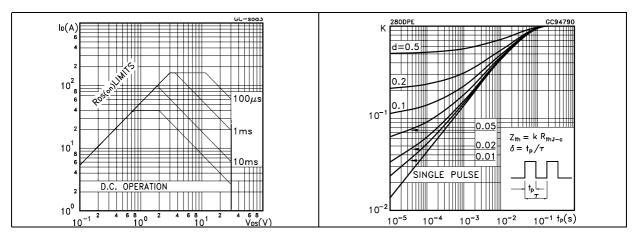


Figure 3. Output characteristics

Figure 4. Transfer characteristics

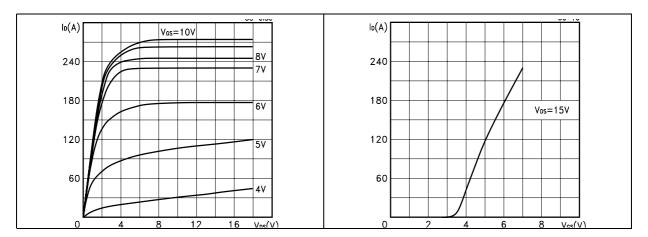
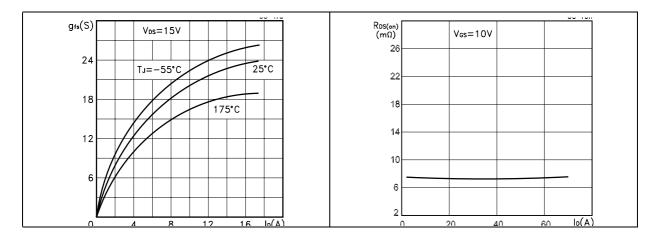


Figure 5. Transconductance

Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs. gate-source voltage Figure 8. Capacitance variations

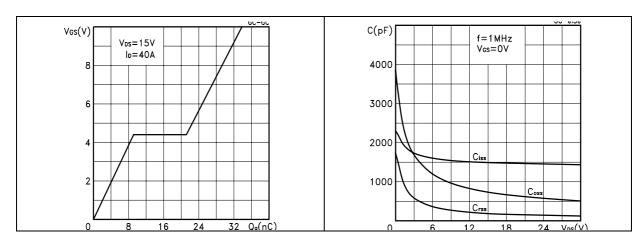


Figure 9. Normalized gate threshold voltage Figure 10. Normalized on resistance vs. vs. temperature temperature

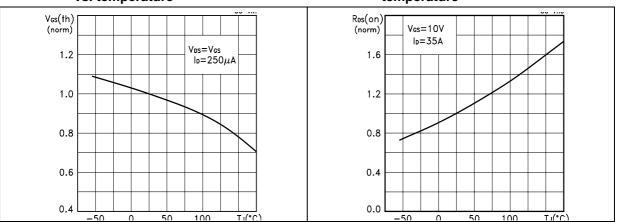
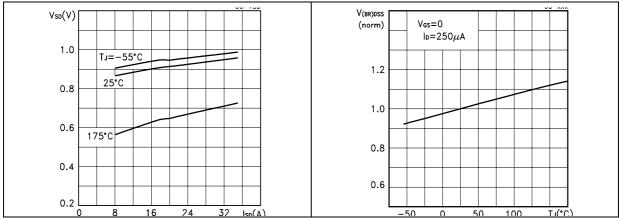


Figure 11. Source-drain diode forward characteristics

Figure 12. Normalized breakdown voltage vs. temperature



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Test circuit STD40NF03L

3 Test circuit

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

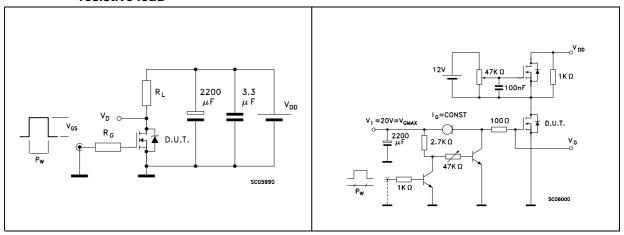


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped Inductive load test circuit

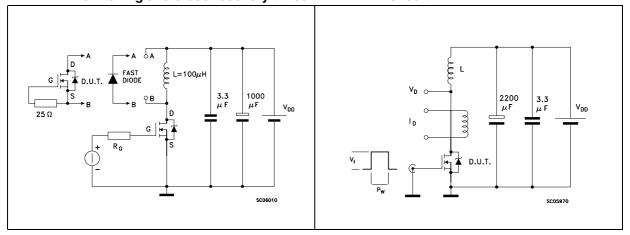
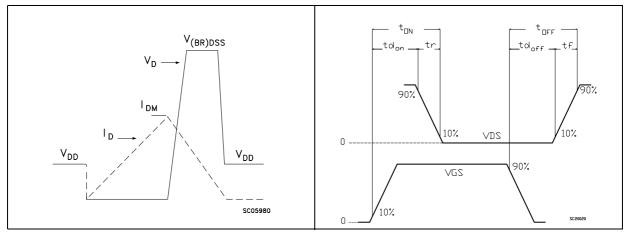


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



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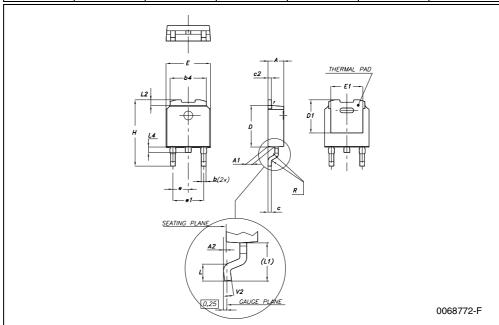
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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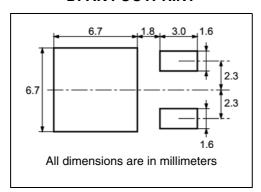
DPAK MECHANICAL DATA

D.114		mm.		inch		
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
Α	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	B 0.64	0.23	0.001		0.009	
В		0.9	0.025		0.035	
b4		5.4	0.204		0.212	
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
е		2.28			0.090	
e1	4.4		4.6	0.173		0.181
Н	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

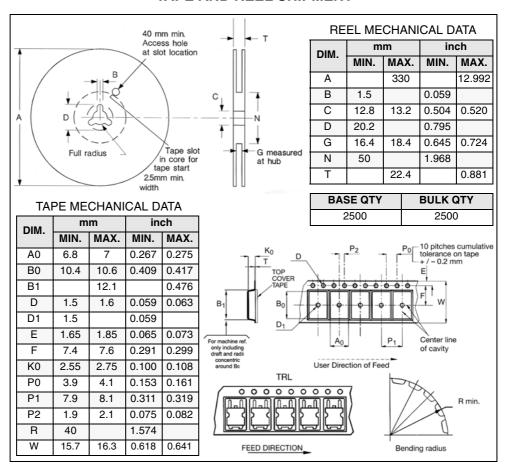


5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



Revision history STD40NF03L

6 Revision history

Table 6. Revision history

Date	Revision	Changes
21-Jun-2004	9	Preliminary data
11-Jul-2006	10	New template, no content change
20-Feb-2007	11	Typo mistake on page 1

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