

# STSJ25NF3LL

## N-CHANNEL 30V - 0.0085 Ω - 25A PowerSO-8<sup>™</sup> LOW GATE CHARGE STripFET<sup>™</sup> II POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STSJ25NF3LL	30 V	<0.0105 Ω	25 A

- TYPICAL R<sub>DS</sub>(on) = 0.0085 Ω @ 10V
- TYPICAL Q<sub>g</sub> = 24 nC @ 4.5 V
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- IMPROVED JUNCTION-CASE THERMAL RESISTANCE

#### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size<sup>TM</sup>" strip-based process. This silicon, housed in thermally improved SO-8<sup>TM</sup> package, exhibits optimal on-resistance versus gate charge tradeoff plus lower  $R_{thj-c.}$ 



#### INTERNAL SCHEMATIC DIAGRAM



#### APPLICATIONS

 SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS FOR MOBILE PC<sub>S</sub>

#### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS}$ = 20 k $\Omega$ )	30	V
V <sub>GS</sub>	Gate- source Voltage	± 16	V
I <sub>D</sub>	Drain Current (continuous) at $T_C = 25^{\circ}C$ (*)	25	A
I <sub>D</sub>	Drain Current (continuous) at $T_C = 25^{\circ}C$ (#)	12	A
ID	Drain Current (continuous) at $T_C = 100^{\circ}C$	16	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	100	A
P <sub>tot</sub>	Total Dissipation at $T_C = 25^{\circ}C$ Total Dissipation at $T_C = 25^{\circ}C$ (#)	70 3	W W

(•) Pulse width limited by safe operating area.

(\*) Value limited by wires bonding

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NEW DATASHEET ACCORDING TO PCN DSG/CT/2C13 MARKING: 25NF3LL@

#### STSJ25NF3LL

#### THERMAL DATA

Rthj-c	Thermal Resistance Junction-case	Max	1.8	°C/W
Rthj-amb	(*)Thermal Resistance Junction-ambient	Max	42	°C/W
T <sub>j</sub>	Maximum Operating Junction Temperature		150	°C
T <sub>stg</sub>	Storage Temperature		-55 to 150	℃

(\*) When mounted on FR-4 board with 0.5 in<sup>2</sup> pad of Cu.

### **ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25 \text{ °C}$ unless otherwise specified)

#### OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	30			V
IDSS	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating $V_{DS}$ = Max Rating $T_{C}$ = 125°C			1 10	μΑ μΑ
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16 V			±100	nA

#### ON (\*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I <sub>D</sub> = 250 μA	1			V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 12.5 A I <sub>D</sub> = 12.5 A		0.0085 0.011	0.0105 0.013	Ω Ω

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> =15 V I <sub>D</sub> = 12.5 A		20		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		1650 540 130		pF pF pF

#### ELECTRICAL CHARACTERISTICS (continued)

#### SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time			23 156		ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> =15V I <sub>D</sub> =25A V <sub>GS</sub> =4.5V (see test circuit, Figure 2)		24 8.5 12	33	nC nC nC

#### SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off Delay Time Fall Time	$ \begin{array}{ll} V_{DD} = 15 \ V & I_D = 12.5 \ A \\ R_G = 4.7 \Omega, & V_{GS} = 4.5 \ V \\ (\text{Resistive Load, Figure 3}) \end{array} $		27 28		ns ns

#### SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (●)	Source-drain Current Source-drain Current (pulsed)				25 100	A A
V <sub>SD</sub> (*)	Forward On Voltage	$I_{SD} = 25 \text{ A}$ $V_{GS} = 0$			1.2	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$\begin{split} I_{SD} &= 25 \text{ A} & \text{di/dt} = 100 \text{A}/\mu\text{s} \\ V_{DD} &= 25 \text{ V} & \text{T}_{j} = 150^{\circ}\text{C} \\ (\text{see test circuit, Figure 3}) \end{split}$		40 50 2.5		ns nC A

(\*)Pulsed: Pulse duration =  $300 \ \mu$ s, duty cycle 1.5 %.

(•)Pulse width limited by safe operating area.

Safe Operating Area



Thermal Impedance





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Normalized Gate Threshold Voltage vs Temperature

Normalized on Resistance vs Temperature



Normalized Breakdown Voltage vs Temperature.



**Fig. 1:** Switching Times Test Circuits For Resistive Load



Fig. 3: Test Circuit For Diode Recovery Behaviour



Fig. 2: Gate Charge test Circuit



**A7/** 

## PowerSO-8™ MECHANICAL DATA

DIM		mm.			inch			
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.		
А			1.75			0.068		
a1	0.1		0.25	0.003		0.009		
a2			1.65			0.064		
a3	0.65		0.85	0.025		0.033		
b	0.35		0.48	0.013		0.018		
b1	0.19		0.25	0.007		0.010		
С	0.25		0.5	0.010		0.019		
c1			45°	(typ.)				
D	4.8		5.0	0.188		0.196		
E	5.8		6.2	0.228		0.244		
e		1.27			0.050			
e3		3.81			0.150			
e4		2.79			0.110			
F	3.8		4.0	0.14		0.157		
L	0.4		1.27	0.015		0.050		
М			0.6			0.023		
S	8° (max.)							



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