# N-Channel 150-V (D-S) 175°C MOSFET

## CHARACTERISTICS

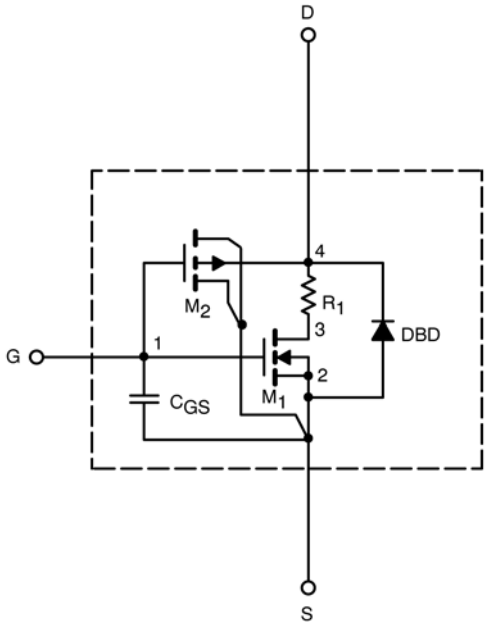
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

## DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## SUBCIRCUIT MODEL SCHEMATIC

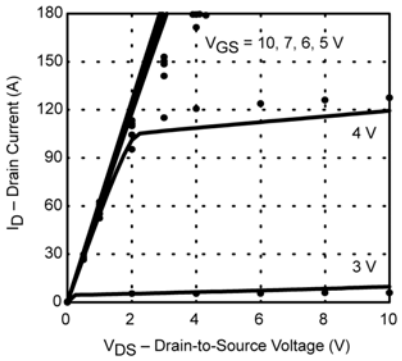


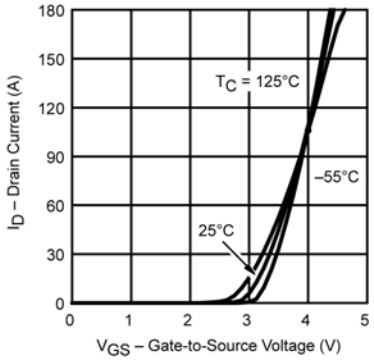

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

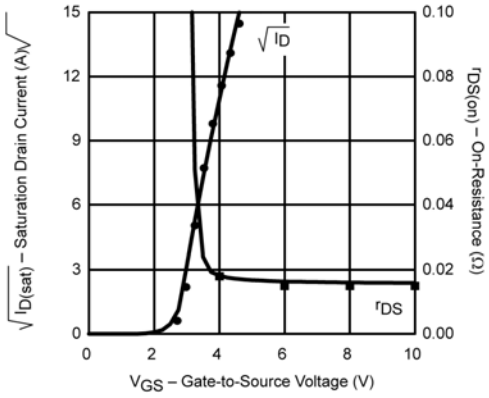
| SPECIFICATIONS ($T_J$ = 25°C UNLESS OTHERWISE NOTED) | | | | | |
|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Simulated Data** | **Measured Data** | **Unit** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1.7 | | V |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 10 V | 314 | | A |
| Drain-Source On-State Resistance[a] | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 30 A | 0.016 | 0.016 | Ω |
| | | $V_{GS}$ = 10 V, $I_D$ = 30 A, $T_J$ = 125°C | 0.023 | | |
| | | $V_{GS}$ = 10 V, $I_D$ = 30 A, $T_J$ = 175°C | 0.026 | | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 20 A | 0.017 | | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 30 A | 93 | | S |
| Forward Voltage[a] | $V_{SD}$ | $I_S$ = 80 A, $V_{GS}$ = 0 V | 0.92 | 1 | V |
| **Dynamic**[b] | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1 MHz | 6590 | 6500 | Pf |
| Output Capacitance | $C_{oss}$ | | 510 | 520 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 320 | 270 | |
| Total Gate Charge[c] | $Q_g$ | $V_{DS}$ = 50 V, $V_{GS}$ = 10 V, $I_D$ = 80 A | 114 | 110 | NC |
| Gate-Source Charge[c] | $Q_{gs}$ | | 21 | 21 | |
| Gate-Drain Charge[c] | $Q_{gd}$ | | 33 | 33 | |
| Turn-On Delay Time[c] | $t_{d(on)}$ | $V_{DD}$ = 50 V, $R_L$ = 0.93 Ω<br>$I_D$ ≅ 80 A, $V_{GEN}$ = 10 V, $R_G$ = 2.5 Ω | 176 | 20 | Ns |
| Rise Time[c] | $t_r$ | | 43 | 100 | |
| Turn-Off Delay Time[c] | $t_{d(off)}$ | | 43 | 70 | |
| Fall Time[c] | $t_f$ | | 49 | 135 | |

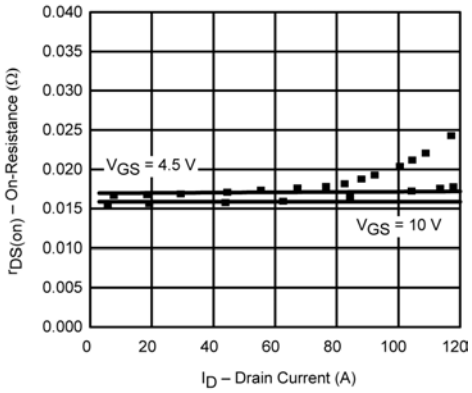
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

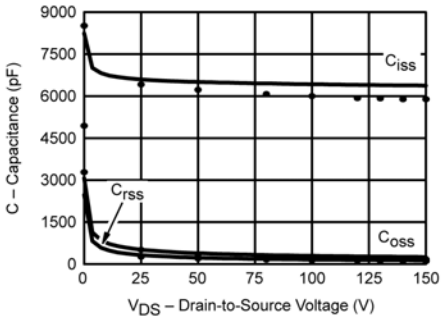
## COMPARISON OF MODEL WITH MEASURED DATA ($T_J$=25°C UNLESS OTHERWISE NOTED)

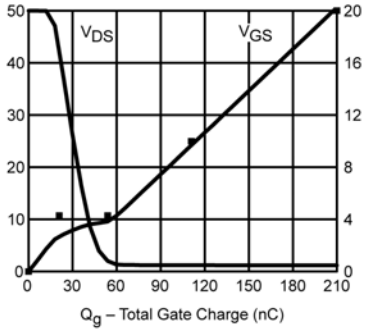



Note: Dots and squares represent measured data.