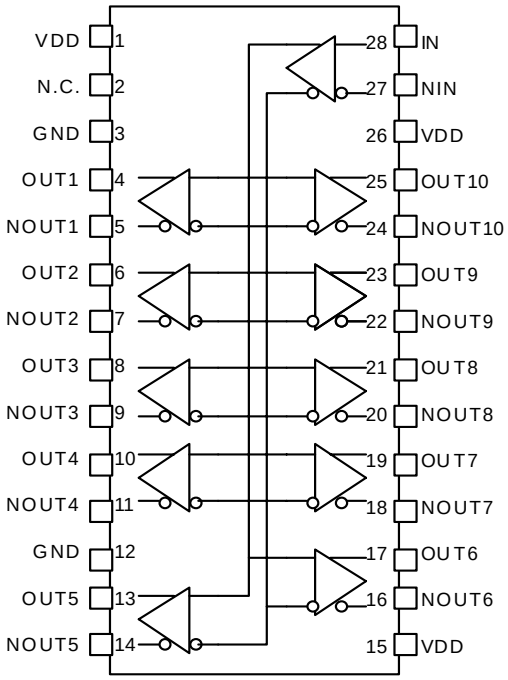


TQ8710

1.5GHz/2.7 Gb/s

1:10 50Ω Driver/Buffer

Features

- 1.5 GHz or 2.7Gb/s
- Single +3.3V Power Supply
- Differential LVPECL/ECL levels
- 50ps output-output skew
- 1pS RMS additive jitter
- Off-chip input termination for daisy chain applications
- May be AC or DC coupled
- 28-pin TSSOP surface mounted package

Applications

- Clock distribution to 1.5 GHz
- Data distribution to 2.7 Gb/S
- CMOS backplane buffering
- 50Ω Backplane driver
- 50Ω Coax driver

The TQ8710 is a 1 input to 10 output buffer utilizing a 3.3V single power supply and differential LVPECL/ECL input and output signal levels. The device is well suited to high speed clock fanout applications where low skew and low additive jitter are important considerations.

The device is capable of either direct coupled LVPECL/ECL interfacing or AC coupled operation. Minimum differential signal sensitivity of 200mVp-p allows the device to be AC coupled to most types of balanced high speed signalling levels. The device is suitable for driving 50Ω transmission lines, including stripline, microstrip, coax structures and cables.

The device is packaged in a plastic TSSOP package which addresses thermal management through the use of a metal tab on the bottom center of the package. This tab is utilized as a required Vdd power supply connection as well as a thermal path to the host circuit board.

Specifications

Table 1. Absolute Maximum Ratings[4]

Parameter	Notes	Symbol	Minimum	Nominal	Maximum	Unit
Storage Temperature		T_{store}	–65		150	°C
Junction Temperature		T_{CH}	–65		150	°C
Case Temperature w/bias	(1)	T_C	0		100	°C
Supply Voltage	(2)	V_{DD}	0		5.5	V
Voltage to any input	(2)	V_{in}	–0.5		V_{DD} + 0.5	V
Voltage to any output	(2)	V_{out}	–0.5		V_{DD} + 0.5	V
Current to any LVTTL input	(2)	I_{in}	–1.0		1.0	mA
Current to any LVPECL input	(2)	I_{in}	–1.0		1.0	mA
Current from any output	(2)	I_{out}			40.0	mA
Power Dissipation of output	(3)	P_{out}			50.0	mW

Notes: 1. Tc is measured at case top.
2. All voltages are measured with respect to GND pin(0V) and are continuous.
3. Pout = (V_{DD} – V_{out}) x I_{out} .
4. Absolute maximum ratings, as detailed in this table, are the ratings beyond which the device's performance may be impaired and/or permanent damage to the device may occur.

Table 2. Recommended Operating Conditions [4]

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_C	Operating Case Temperature	0	—	85	°C	1
V_{DD}	Positive Supply Voltage	3.14	—	3.46	V	
I_{DD}	Positive Supply Current			300	mA	3
V_{TT}	Load Termination Supply Voltage		V_{DD} – 2.0		V	2
R_{LOAD}	Output Termination Load Resistance		50		Ω	2

Notes: 1. Package thermal pad to be soldered to PCB.
2. The V_{TT} and R_{LOAD} combination is subject to maximum output current and power restrictions. Note that the value shown is for DC coupled LVPECL I/O.
3. Outputs open.
4. Functionality and/or adherence to electrical specifications is not implied when the device is subjected to conditions that exceed, singularly or in combination, the operating range specified.

Table 3. DC Characteristics—LVPECL I/O [3]

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Input common mode voltage range		V_{ICOM}	V_{DD} – 1500	—	V_{DD} – 1100	mV
Input differential voltage (pk-pk)	(1)	V_{IDIFF}	600	—	2400	mV
Output common mode voltage range		V_{OCOM}	V_{DD}-1500	—	V_{DD} – 1100	mV
Output differential voltage (pk-pk)	(1,2)	V_{ODIFF}	1200	—	2400	mV
Equivalent Input resistance		R_{IN}	—	50	—	KΩ
Input capacitance		C_{IN}	—	0.5	—	pF
Output capacitance		C_{OUT}	—	0.5	—	pF
ESD breakdown rating		V_{ESD}	1000	—	—	V

Notes: 1. Differential Input Peak-Peak = 2| Vin - NVin |. LVDS signals up to 622MHz can be AC coupled, see application note #1. The minimum input sensitivity under these conditions is 500mV.
2. R_{LOAD} = 50 ohms to $V_{TT} = V_{DD} – 2.0V$.
3. Specifications apply over recommended operating ranges.

Table 4. AC Characteristics

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Data Rate/port			2.7			Gb/s
Clock Rate/port			1.5			GHz
Input pulse width	(1)	T_{pw}	333	—	—	ps
Rise/Fall time 20-80%		$T_{r/f}$	—	100	150	ps
Jitter (pk-pk)	(2)	T_{jitter}	—	6	10	ps
Jitter (RMS-fixed frequency)		T_{jitter}	—	0.6	1	ps

Notes: 1. Measured at crossing point of true and complement
2. Crossing of (On) – (NOn) measured with $2^{23} – 1$ PRBS, measured over extended time.

Table 5. Timing Specifications

Parameter	Condition	Symbol	Minimum	Nominal	Maximum	Unit
Channel Propagation Delay	(1)	T_{pd}	—	—	1000	ps
Ch-to-Ch Prop. Delay Skew	(1)	T_{skew}	—	—	50	ps

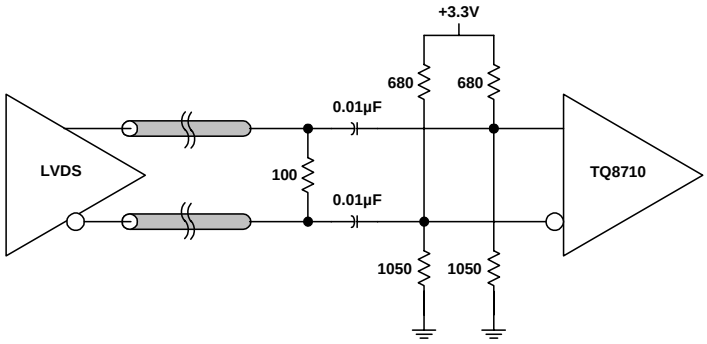
Notes: 1. Measured at crossing point of true and complement

Table 6. TQ8710 Pin Descriptions

Signal	Type	Pin Number	Description
Input Ports			
IN,NIN	DLVPECL Input	28,27	True and Complement DLVPECL Clock/Data In.
Output Ports			
OUT1,NOUT1	DLVPECL Output	4,5	True and Complement DLVPECL Clock/Data Out
OUT2,NOUT2	DLVPECL Output	6,7	True and Complement DLVPECL Clock/Data Out
OUT3,NOUT3	DLVPECL Output	8,9	True and Complement DLVPECL Clock/Data Out
OUT4,NOUT4	DLVPECL Output	10,11	True and Complement DLVPECL Clock/Data Out
OUT5,NOUT5	DLVPECL Output	13,14	True and Complement DLVPECL Clock/Data Out
OUT6,NOUT6	DLVPECL Output	17,16	True and Complement DLVPECL Clock/Data Out
OUT7,NOUT7	DLVPECL Output	19,18	True and Complement DLVPECL Clock/Data Out
OUT8,NOUT8	DLVPECL Output	21,20	True and Complement DLVPECL Clock/Data Out
OUT9,NOUT9	DLVPECL Output	23,22	True and Complement DLVPECL Clock/Data Out
OUT10,NOUT10	DLVPECL Output	25,24	True and Complement DLVPECL Clock/Data Out
Power Pins			
Signal	***Description***	***Pin Number***	
VDD	Positive Power Supply	1, 15, 26, Package Down Paddle (required)	
GND	Negative Power Supply	3, 12	
N/C	Do Not Connect	2	

Application notes

1. Recommended LVDS to TQ8710 interface for AC balanced signals above 100KHz.



2. Power supply connections for ECL operation.