DATA SHEET

TZA3005
SDH/SONET STM1/OC3 and STM4/OC12 transceiver

Objective specification
File under Integrated Circuits, IC19

1997 Aug 05

Philips
Semiconductors

PHILIPS

SDH/SONET STM1/OC3 and STM4/OC12 transceiver

TZA3005

FEATURES

- Supports STM1/OC3 (155.52 Mbits/s) and STM4/OC12 (622.08 Mbits/s)
- Supports 19.44, 38.88, 51.84 and 77.76 MHz reference clock frequencies
- Meets Bellcore, ANSI and ITU-T specifications
- Integral high-frequency PLL for clock generation
- Interface to TTL logic
- Low jitter PECL (Positive Emitter Coupled Logic) interface.
- 4- or 8-bit STM1/OC3 TTL/CMOS data path
- 4- or 8-bit STM4/OC12 TTL/CMOS data path
- No external filter components required
- QFP64 package
- Diagnostic and line loopback modes
- Lock detect
- LOS (Loss of Signal) input
- Low power (900 mW typically)

APPLICATIONS

- SDH/SONET modules
- SDH/SONET-based transmission systems
- SDH/SONET test equipment
- ATM over SDH/SONET
- Add drop multiplexers
- Broadband cross-connects
- Section repeaters
- Fiber optic test equipment.
- Fiber optic terminators

GENERAL DESCRIPTION

The TZA3005 SDH/SONET transceiver chip is a fully integrated serialization/deserialization SDH/SONET STM4/OC12 (622.08 Mbits/s) and STM1/OC3 (155.52 Mbits/s) interface device. It performs all necessary serial-to-parallel and parallel-to-serial functions in accordance with SDH/SONET transmission standards. It is suitable for SONET-based applications and can be used in conjunction with the TZA3004 clock recovery device, the TZA3000 optical receiver and the TZA3001 laser driver. Figure 13 shows a typical network application.

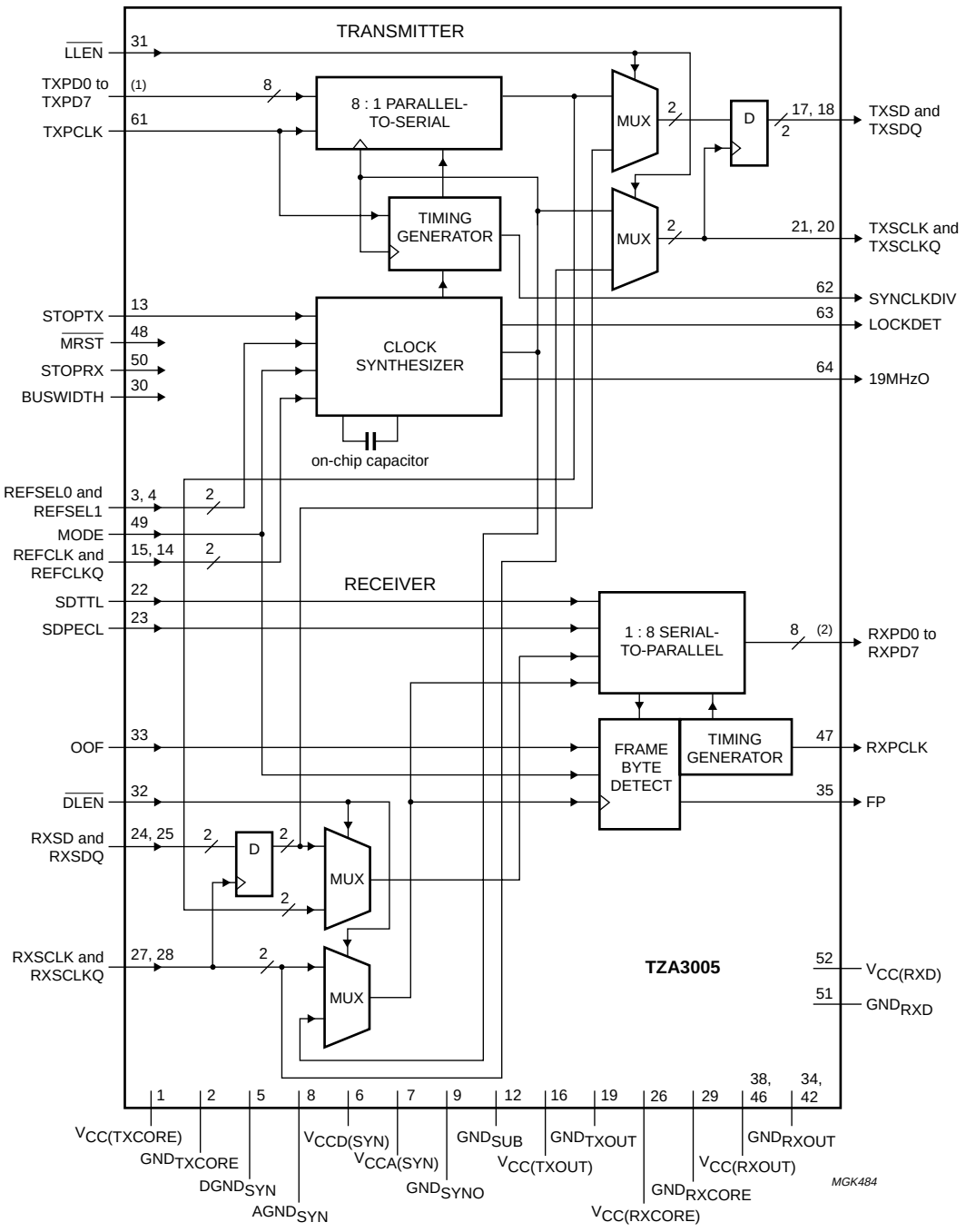
A high-frequency phase-locked loop is used for on-chip clock synthesis, which means a slower external transmit reference clock can be used. A 19.44, 38.88, 51.84 or 77.76 MHz reference clock can be used, in support of existing system clocking schemes. The TZA3005 performs SDH/SONET frame detection.

The low jitter PECL interface ensures that Bellcore, ANSI, and ITU-T bit-error rate requirements are satisfied. The TZA3005 comes in a compact QFP64 package.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3005H	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm	SOT393-1

BLOCK DIAGRAM



(1) Pins 53 to 60.

(2) Pins 36, 37, 39, 40, 41, 43, 44 and 45.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
$V_{CC(TXCORE)}$	1	S	supply voltage (transmitter core)
GND_{TXCORE}	2	S	ground (transmitter core)
REFSEL0	3	I	reference clock select input 0
REFSEL1	4	I	reference clock select input 1
$DGND_{SYN}$	5	S	digital ground (synthesizer)
$V_{CCD(SYN)}$	6	S	digital supply voltage (synthesizer)
$V_{CCA(SYN)}$	7	S	analog supply voltage (synthesizer)
$AGND_{SYN}$	8	S	analog ground (synthesizer)
GND_{SYNO}	9	S	ground (synthesizer output)
STOPSYN	10	I	test input : synthesizer section shut down
RSTRX	11	I	test input : reset receive logic
GND_{SUB}	12	S	ground (substrate)
STOPTX	13	I	test input : transmit section shut down
REFCLKQ	14	I	inverted reference clock input
REFCLK	15	I	reference clock input
$V_{CC(TXOUT)}$	16	S	supply voltage (transmitter output)
TXSD	17	O	serial data output
TXSDQ	18	O	inverted serial data output
GND_{TXOUT}	19	S	ground (transmitter output)
TXSCLKQ	20	O	inverted serial clock output
TXSCLK	21	O	serial clock output
SDTTL	22	I	TTL signal detect input
SDPECL	23	I	PECL signal detect input
RXSD	24	I	serial data input
RXSDQ	25	I	inverted serial data input
$V_{CC(RXCORE)}$	26	S	supply voltage (receiver core)
RXSCLK	27	I	serial clock input
RXSCLKQ	28	I	inverted serial clock input
GND_{RXCORE}	29	S	ground (receiver core)
BUSWIDTH	30	I	4/8 bus width select input
$\overline{LLEN}$	31	I	line loopback enable input (active LOW)
$\overline{DLEN}$	32	I	diagnostic loopback enable input (active LOW)
OOF	33	I	out of frame enable input
GND_{RXOUT}	34	S	ground (parallel output)
FP	35	O	frame pulse output
RXPD0	36	O	parallel data output 0
RXPD1	37	O	parallel data output 1
$V_{CC(RXOUT)}$	38	S	supply voltage (parallel output)
RXPD2	39	O	parallel data output 2
RXPD3	40	O	parallel data output 3

SYMBOL	PIN	TYPE(1)	DESCRIPTION
RXPD4	41	O	parallel data output 4
GND_{RXOUT}	42	S	ground (receiver output)
RXPD5	43	O	parallel data output 5
RXPD6	44	O	parallel data output 6
RXPD7	45	O	parallel data output 7
$V_{CC(RXOUT)}$	46	S	supply voltage (receiver output)
RXPCLK	47	O	receive parallel clock output
$\overline{MRST}$	48	I	master reset (active LOW)
MODE	49	I	serial data rate select STM1/STM4
STOPRX	50	I	receiver section shut down
GND_{RXD}	51	S	ground (receiver digital section)
$V_{CC(RXD)}$	52	S	supply voltage (receiver digital section)
TXPD0	53	I	parallel data input 0
TXPD1	54	I	parallel data input 1
TXPD2	55	I	parallel data input 2
TXPD3	56	I	parallel data input 3
TXPD4	57	I	parallel data input 4
TXPD5	58	I	parallel data input 5
TXPD6	59	I	parallel data input 6
TXPD7	60	I	parallel data input 7
TXPCLK	61	I	transmit parallel clock input
SYNCLKDIV	62	O	transmit byte/nibble clock output (synchronous)
LOCKDET	63	O	lock detect
19MHzO	64	O	19 MHz output reference clock

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply.

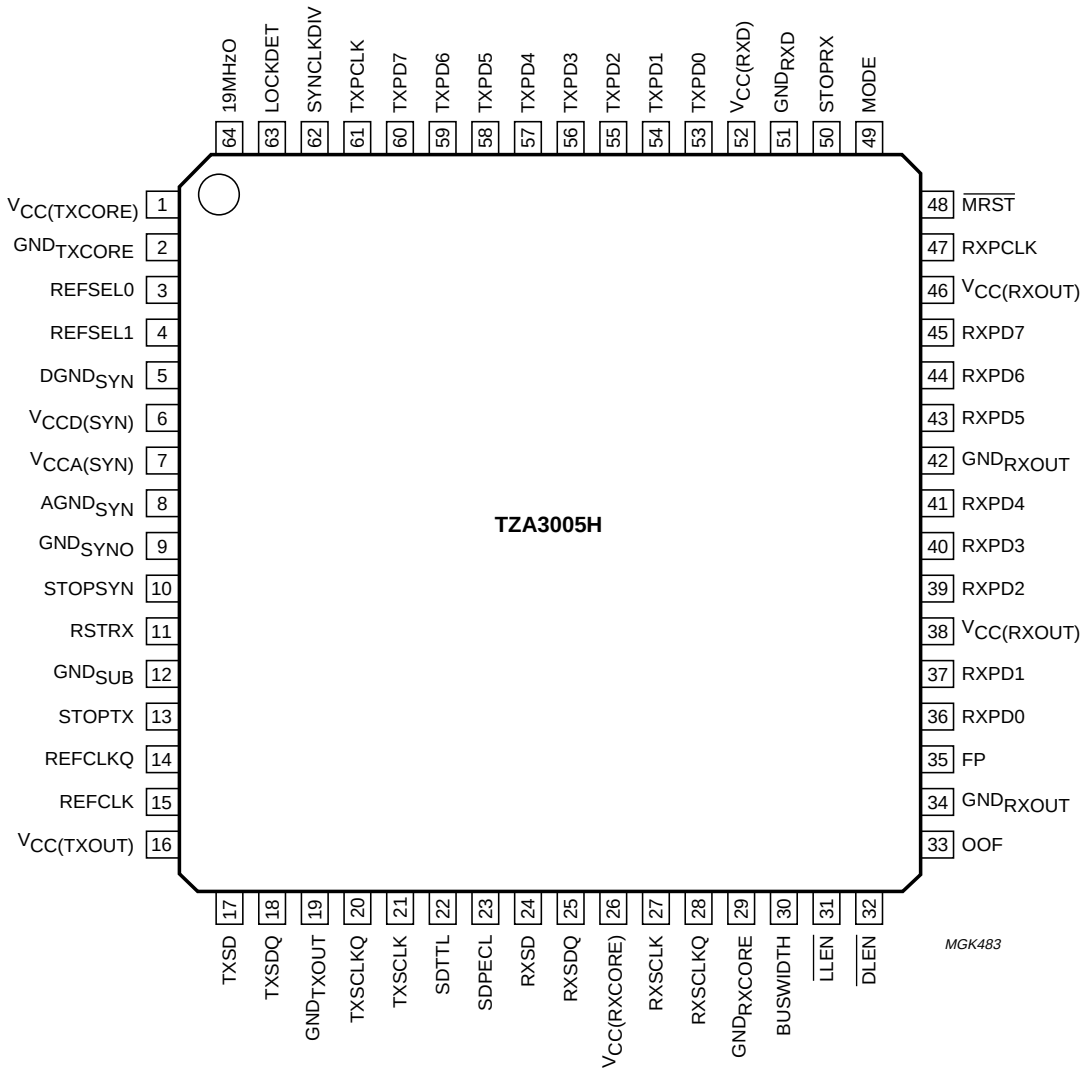


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Introduction

The TZA3005 transceiver implements SDH/SONET serialization/deserialization, transmission and frame detection/recovery functions. The block diagram in Fig.1 illustrates the basic operation of the chip. The TZA3005 can be used to implement the front-end of SONET equipment, which consists primarily of the serial transmit and receive interfaces. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry handles data stream management, framing, and clock distribution throughout the front-end.

The TZA3005 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

- Transmitter operations:
  - 4- or 8-bit parallel input
  - Parallel-to-serial conversion
  - Serial output
- Receiver operations:
  - Serial input
  - Frame detection
  - Serial-to-parallel conversion
  - 4- or 8-bit parallel output.

Internal clocking and control functions are transparent to the user. Details of data timing can be found in Figs 3 to 9.

Transmitter operation

The TZA3005 transceiver chip performs the serializing stage in the processing of a transmit STM1/OC3 or STM4/OC12 serial bitstream. It converts the byte serial 19.44, 38.88 or 77.76 Mbytes/s data stream to bit serial format at 155.52 or 622.08 Mbits/s. Diagnostic loopback is provided (transmitter to receiver). Line loopback is also provided (receiver to transmitter).

An integral frequency synthesizer, consisting of a phase-locked loop with a divider in the loop, can be used to generate a high-frequency bit clock from a 19.44, 38.88, 51.84 or 77.76 MHz reference frequency.

Clock synthesizer

The serial output clock is generated by the clock synthesizer (see Fig.1). This signal is phase synchronized with the input reference clock (REFCLK). Two output clock frequencies are available, synthesized from any of four SDH/SONET reference frequencies.

The MODE input is used to select the serial output clock frequency: 622.08 MHz for STM4/OC12 or 155.52 MHz for STM1/OC3 (see Table 1).

Table 1 Clock frequency options

MODE	OUTPUT CLOCK FREQUENCY	OPERATING MODE
1	622.08 MHz	STM4/OC12
0	155.52 MHz	STM1/OC3

Table 2 Suggested interface devices

MANUFACTURER	TYPE	DATA RATE (Mbits/s)	FUNCTION
Philips	TZA3004	622 or 155	clock recovery
	TZA3000	622	optical receiver
	TZA3001	622	laser driver
	SA5225	155	limiting amplifier
	SA5223	155	transimpedance amplifier
PMC-Sierra	PM5312	155 or 622	transport terminal transceiver
	PM5355	622	Saturn user network interface

The REFSEL0 and REFSEL1 inputs, in combination with the MODE input, select the ratio between the output clock frequency and the reference input frequency (see Table 3). This ratio is adjusted for each of the four options so that the reference frequency selected by REFSEL0 and REFSEL1 is the same for all operating modes.

To ensure the TXSCLK frequency is accurate enough to operate in a SONET system, the REFCLK input must be generated from a differential PECL crystal oscillator with a frequency accuracy better than 4.6 ppm for compliance with *"ITU G.813 (option 1)"*, or 20 ppm for *"ITU G.813 (option 2)"*.

The maximum value specified for reference clock jitter must be guaranteed over the a 12 kHz to 1 MHz bandwidth in order to comply with SONET jitter requirements (see Table 4).

The on-chip PLL contains a phase detector, a loop filter and a VCO. The phase detector compares the phases of the output and REFCLK input signals. The loop filter converts the phase detector output into a smooth DC voltage that is used to vary the VCO frequency.

The VCO control voltage generated by the loop filter is referenced to the average DC level in the output pulse train generated by the phase discriminator. The corner frequency is optimized to minimize output phase jitter.

Table 3 Reference frequency options

REFSEL0	REFSEL1	INPUT CLOCK FREQUENCY
0	0	19.44 MHz
0	1	38.88 MHz
1	0	51.84 MHz
1	1	77.76 MHz

Table 4 Reference jitter limits

MAXIMUM REFERENCE CLOCK JITTER IN 12 kHz TO 1 MHz BAND	OPERATING MODE
84 ps (p-p)	STM4/OC12
336 ps (p-p)	STM1/OC3

TIMING GENERATOR

The timing generator performs two functions. It provides a byte rate version of the TXSCLK along with a mechanism for phase aligning the incoming byte clock and the clock that loads the parallel-to-serial shift register.

The SYNCLKDIV output is a byte rate version of TXSCLK. For STM4/OC12, the SYNCLKDIV frequency is 77.76 or 155.52 MHz and for STM1/OC3, it is 19.44 or 38.88 MHz. SYNCLKDIV is intended for use as a byte speed clock for upstream multiplexing and overhead processing circuits. Using SYNCLKDIV for upstream circuits will ensure a stable frequency and phase relationship is maintained between the data entering and leaving the TZA3005.

For parallel-to-serial conversion, the parallel input data is transferred from the TXPCLK byte clock timing domain to the internally generated byte clock timing domain, which is phase aligned to TXPCLK.

The timing generator also produces a feedback reference clock for the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the reference clock REFCLK. The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the feedback reference clock with that of the reference clock (REFCLK). The modulus of the counter is a function of the reference clock frequency and the operating frequency.

PARALLEL-TO-SERIAL CONVERTER

The parallel-to-serial converter shown in Fig.1 contains two byte-wide registers. The first register latches the data from the parallel bus (TXPD0 to TXPD7) on the rising edge of TXPCLK. The second register is a parallel loading shift register which takes its input from the first register.

The parallel data transfer is controlled by an internally generated byte clock, which is phase aligned with the transmit serial clock (see Section "Timing generator"). The TXSCLK signal is used to shift the serial data out of the second register.

Receiver operation

The TZA3005 transceiver chip performs the first stage in the digital processing of a STM1/OC3 or STM4/OC12 serial bitstream. It converts the 155.52 or 622.08 Mbits/s data stream into a 19.44 or 77.76 Mbytes/s serial format. In nibble mode, a parallel data stream of 38.88 or 155.52 MHz is generated. Diagnostic (transmitter to receiver) and line (receiver to transmitter) loopback modes are provided.

FRAME AND BYTE BOUNDARY DETECTION

The frame and byte boundary detection circuitry searches the incoming data for three consecutive A1 bytes followed immediately by three consecutive A2 bytes. Framing

pattern detection is enabled and disabled by the Out-Of-Frame (OOF) input. Detection is enabled by a rising edge on OOF, and remains enabled while OOF is HIGH. It is disabled when a framing pattern is detected and OOF is no longer HIGH. When framing pattern detection is enabled, the framing pattern is used to locate byte and frame boundaries in the incoming data stream (Receive Serial Data (RXSD) or looped transmitter data). The timing generator block uses the located byte boundary to divide the incoming data stream into bytes for output on the parallel output data bus (RXPD0 to RXPD7). When a 48-bit pattern matching the framing pattern is detected, the frame boundary is signalled on the Frame Pulse (FP) output. When framing pattern detection is disabled, the byte boundary is frozen. Only framing patterns aligned to the fixed byte boundary are signalled on the FP output.

It is extremely unlikely that random data in an STM1/OC3 or STM4/OC12 data stream will replicate the 48-bit framing pattern. Therefore, the time taken to detect the beginning of the frame should be less than 250 µs (as specified in *"ITU G.783"*), even for extremely high bit error rates.

Once down-stream overhead circuitry has verified that frame and byte synchronization are correct, the OOF input can be set LOW to prevent the frame search process trying to synchronize to a mimic frame pattern.

SERIAL-TO-PARALLEL CONVERTER

A delay of between 1.5 and 2.5 byte periods (or 12 to 20 serial bit periods measured from the first bit of an incoming byte to the beginning of the parallel output of that byte) occurs in the serial-to-parallel converter. The variation in the delay depends on the alignment of the internal parallel load timing, which is synchronized to the data byte boundaries, with respect to the falling edge of RXPCLK, which is independent of the byte boundaries. RXPCLK is neither truncated nor extended during reframe sequences.

Transceiver pin descriptions

TRANSMITTER INPUT SIGNALS

Parallel data inputs (TXPD0 to TXPD7)

This is a 19.44, 38.88, 77.76 or 155.52 Mbytes/s TTL level word, aligned to the TXPCLK parallel input clock. TXPD7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). TXPD0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit transmitted). TXPD0 to TXPD7 are sampled on the rising edge of TXPCLK. If a 4-bit bus width is selected, TXPD7 is the most significant bit and TXPD4 is the least significant bit.

Parallel clock input (TXPCLK)

This is a 19.44, 38.88, 77.76 or 155.52 MHz nominally 50% duty factor TTL level input clock, to which TXPD0 to TXPD7 are aligned. TXPCLK is used to transfer the data on the inputs to a holding register in the parallel-to-serial converter.
The rising edge of TXPCLK samples TXPD0 to TXPD7. After a master reset, one rising edge of TXPCLK is required to fully initialize the internal data path.

RECEIVER INPUT SIGNALS

Receive Serial Data (RXSD and RXSDQ)

These differential PECL serial data input signals are normally connected to an optical receiver module or to the TZA3004 data and clock recovery unit, and are clocked by the RXSCLK and RXSCLKQ inputs.

Receive serial clock (RXSCLK and RXSCLKQ)

This differential PECL recovered clock signal is synchronized to the RXSD inputs. It is used by the receive section as the master clock for framing and deserialization functions.

Out-Of-Frame (OOF)

This TTL level indicator is used to enable framing pattern detection logic in the TZA3005. The framing pattern detection logic is enabled by a rising edge on OOF, and remains enabled until a frame boundary is detected or OOF goes LOW. OOF is an asynchronous signal with a minimum pulse width of one RXPCLK period (see Figs 3 and 9).

Signal Detect PECL (SDPECL)

This is a PECL signal with an internal pull-down resistor. It is active HIGH when SDTTL is at logic 0 and active LOW when SDTTL is at logic 1. This single-ended 10K PECL input is driven by the external optical receiver module to indicate a loss of received optical power (Loss of Signal). When SDPECL is inactive, the data on the serial data input pins (RXSD and RXSDQ) will be internally forced to a constant zero. When SDPECL is active, data on the RXSD and RXSDQ pins will be processed normally.

When SDTTL is to be connected to the optical receiver module instead of SDPECL, SDPECL should be tied HIGH to implement an active LOW signal detect, or left unconnected to implement an active HIGH signal detect.

Signal Detect TTL (SDTTL)

This is a TTL signal with an internal pull-up resistor. It is active HIGH when SDPECL is unconnected (logic 0), active LOW when SDPECL is at logic 1. This single-ended TTL input is driven by the external optical receiver module to indicate a loss of received optical power. When SDTTL is inactive, the data on RXSD and RXSDQ will be internally forced to a constant zero. When SDTTL is active, data on the RXSD and RXSDQ pins will be processed normally.

Table 5 SDPECL/SDTTL truth table

SDPECL	SDTTL	RXPD OUTPUT DATA
0 or floating	0	0
0 or floating	1 or floating	RXSD input data
1	0	RXSD input data
1	1 or floating	0

COMMON INPUT SIGNALS

Bus width selection (BUSWIDTH)

This TTL signal is used to select 4-bit or 8-bit operation for the transmit and receive parallel interfaces. LOW selects a 4-bit bus width. HIGH selects an 8-bit bus width.

Reference clock (REFCLK and REFCLKQ)

These differential PECL inputs supply the reference clock for the internal bit clock frequency synthesizer.

Diagnostic loopback enable ($\overline{DLEN}$)

This active LOW TTL input selects diagnostic loopback. When $\overline{DLEN}$ is HIGH, the TZA3005 uses the primary data (RXSD) and clock (RXSCLK) inputs. When LOW, the TZA3005 uses the diagnostic loopback clock and data from the transmitter.

Master reset ($\overline{MRST}$)

This is an active LOW TTL level reset input. SYNCLKDIV does not toggle during reset.

Line loopback enable ($\overline{LLEN}$)

This active LOW TTL input selects line loopback. When $\overline{LLEN}$ is LOW, the TZA3005 will route the data from the RXSD and RXSCLK inputs to the TXSD and TXSCLK outputs.

Reference select (REFSEL0 and REFSEL1)

This TTL signal is used to select the reference clock frequency (see Table 3).

Mode select (MODE)

This TTL signal is used to select the serial bit rate. LOW selects 155.52 Mbits/s. HIGH selects 622.08 Mbits/s.

Test inputs (STOPSYN, STOPTX, STOPRX and RSTRX)

These active HIGH TTL signals are used to test internal circuitry during production testing. All must be LOW during normal operation. Internal pull-down resistors will hold all four test pins LOW if not connected.

TRANSMITTER OUTPUT SIGNALS

Transmit clock outputs (TXSCLK and TXSCLKQ)

This differential PECL transmit serial clock output can be used to retime the TXSD signal. The clock will be 622.08 MHz or 155.52 MHz depending on the operating mode.

Transmit Serial Data (TXSD and TXSDQ)

These differential PECL serial data stream signals are normally connected to an optical transmitter module or to the TZA3001 laser driver.

Parallel clock (SYNCLKDIV)

This CMOS reference clock is generated by dividing the internal bit clock by eight (or by four when BUSWIDTH is LOW). It is normally used to coordinate byte-wide transfers between upstream logic and the TZA3005.

Lock detect (LOCKDET)

This is an active HIGH CMOS output. When active, it indicates that the transmit PLL is locked to the reference clock input.

RECEIVER OUTPUT SIGNALS

Parallel outputs (RXPD0 to RXPD7)

This is a 19.44, 38.88, 77.76 or 155.52 Mbytes/s parallel CMOS data bus aligned to the parallel output clock (RXPCLK). RXPD7 is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). RXPD0 is the least significant bit (corresponding to bit 8 of each PCM word, the last bit received). RXPD0 to RXPD7 are updated on the falling

edge of RXPCLK. When a 4-bit bus width is selected, TXPD7 is the most significant bit and bit 4 is the least significant bit.

19 MHz clock output (19MHzO)

This is a 19 MHz CMOS clock output from the clock synthesizer. It should be connected to the reference clock input of the external clock recovery function (such as the TZA3004).

Frame Pulse (FP)

This CMOS output detects frame boundaries in the incoming data stream (RXSD). When framing pattern detection is enabled (see Section “Out-Of-Frame (OOF)”), FP goes HIGH for one cycle of RXPCLK when a 48-bit sequence matching the framing pattern is detected on the RXSD inputs. When framing pattern detection is disabled, FP goes HIGH when, after byte alignment, the incoming data stream matches the framing pattern. FP is updated on the falling edge of RXPCLK.

Parallel output clock (RXPCLK)

This 19.44, 38.88, 77.76 or 155.52 MHz nominally 50% duty factor byte rate output clock (CMOS) is aligned to RXPD0 to RXPD7 byte serial output data.
RXPD0 to RXPD7 and FP are updated on the falling edge of RXPCLK.

Other operating modes

DIAGNOSTIC LOOPBACK

A transmitter-to-receiver loopback mode is available for diagnostic purposes. When $\overline{\text{DLEN}}$ is LOW, the differential serial data output from the transmitter is routed to the serial-to-parallel block in place of the normal data stream (RXSD), at the serial data rate.

LINE LOOPBACK

The line loopback circuitry consists of alternate clock and data output drivers. For the TZA3005, it selects the source of the data and clock signals output on TXSD and TXSCLK. When $\overline{\text{LLEN}}$ is HIGH, it selects data and clock signals from the parallel-to-serial converter block. When $\overline{\text{LLEN}}$ is LOW, it forces the output data multiplexer to select data and clock signals from the RXSD and RXSCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Diagnostic loopback and line loopback can be active at the same time.

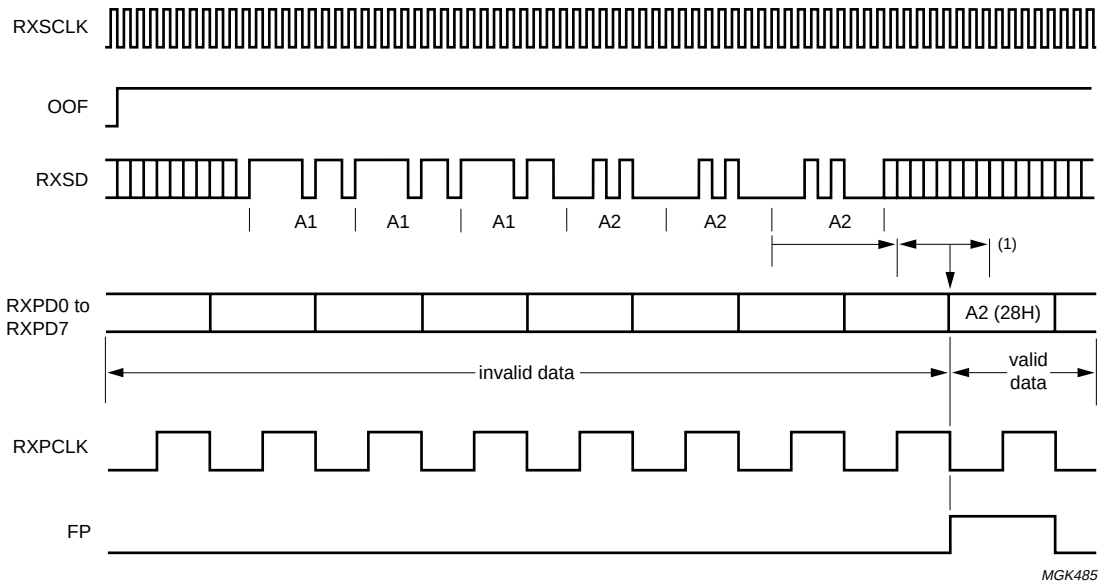
Receiver framing

A typical reframe sequence involving byte realignment is shown in Figure 3. Frame and byte boundary detection is enabled on the rising edge on OOF and remains enabled while OOF is HIGH. Boundaries are recognized on receipt of the third A2 byte, the first data byte to be reported with the correct byte alignment on the outgoing data bus (RXPD0 to RXPD7). FP goes HIGH for one RXPCLK cycle.

When interfacing with a section terminating device, OOF must remain HIGH for a full frame after the initial frame pulse. This is to allow the section terminating device to verify internally that frame and byte alignment are correct (see Fig.4). Since at least one framing pattern will have been detected since the rising edge of OOF, boundary detection will be disabled when OOF goes LOW.

The frame and byte boundary detection block is activated by a rising edge on OOF, and remains active until an FP pulse occurs AND OOF goes LOW (whichever occurs last). Figure 4 shows a typical OOF timing pattern when the TZA3005 is connected to a down stream section terminating device. OOF remains HIGH for one full frame after the first FP pulse. The frame and byte boundary detection block is active until OOF goes LOW.

Figure 5 shows frame and byte boundary detection activated on the rising edge of OOF, and deactivated by the first FP pulse after OOF goes LOW.



(1) The input-to-output delay will be between 1.5 and 2.5 cycles of RXPCLK.

Fig.3 Frame and byte detection.

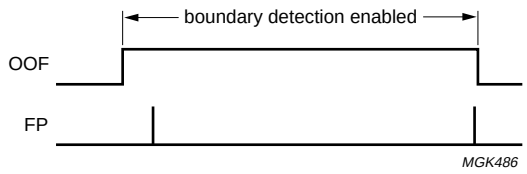


Fig.4 OOF operating time with PM5312 STTX or PM5355 SUNI-622.

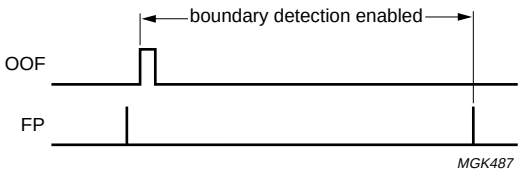


Fig.5 Alternate OOF timing.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	supply voltage	–0.5	+6.5	V
V_n	voltage on			
	any TTL input pin	–0.5	+5.5	V
	any PECL input pin	0	V_{CC}	V
$I_{o(sink)}$	CMOS output sink current	–	8	mA
$I_{o(source)}$	output source current			
	CMOS	–	8	mA
	high speed PECL	–	50	mA
P_{tot}	total power dissipation	–	1.3	W
T_{case}	case temperature under bias	–55	+100	°C
T_j	junction temperature under bias	–55	+125	°C
T_{stg}	storage temperature	–65	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient; note 1	55	K/W

Note

1. Measured using a standard test board. This value will vary (and could be as low as 33 K/W) depending on the number of board layers, copper area, copper sheet thickness and the proximity of surrounding components.

DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
General						
V_{CC}	supply voltage	note 1	3.0	–	5.5	V
P_{tot}	total power dissipation	outputs open; V_{CC} = 5 V	–	0.9	1.2	W
TTL Inputs						
V_{IH}	HIGH-level input voltage	$I_{IH} \leq 1$ mA at V_{IH} = 5.5 V	2.0	–	5.5	V
V_{IL}	LOW-level input voltage	–	0	–	0.8	V
I_{IH}	HIGH-level input current	V_I = 2.4 V	−10	–	+10	µA
		V_{CC} = 5.5 V; V_I = 5.5 V	−10	–	+10	µA
I_{IL}	LOW-level input current	V_I = 0.5 V	−10	–	+10	µA
CMOS Outputs						
V_{OH}	HIGH-level output voltage	V_{CC} = 3.0 V; I_{OH} = −1 mA	2.7	3.0	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 3.0 V; I_{OH} = 4 mA	–	0.1	+0.5	V
$I_{O(sc)}$	output short-circuit current	V_{CC} = 5.5 V; V_O = 0.5 V	–	–500	–200	mA
PECL I/O						
V_{IH}	HIGH-level input voltage	note 2	V_{CC} − 1.17	–	V_{CC} − 0.88	V
V_{IL}	LOW-level input voltage	note 2	V_{CC} − 1.81	–	V_{CC} − 1.48	V
V_{OH}	HIGH-level output voltage	terminated with 50 Ω to V_{CC} − 2.0 V	V_{CC} − 1.1	V_{CC} − 1.0	V_{CC} − 0.9	V
V_{OL}	LOW-level output voltage	terminated with 50 Ω to V_{CC} − 2.0 V	V_{CC} − 1.8	V_{CC} − 1.7	V_{CC} − 1.6	V
$\Delta V_{i(dif)}$	differential input voltage swing for differential PECL inputs	note 2	100	–	1300	mV
ΔV_o	serial output voltage swing	terminated with 50 Ω to V_{CC} − 2.0 V	600	–	1600	mV

Note

1. A single 5 V supply can be used for all V_{CC} pins. Alternatively, a 3.3 V supply can be used for $V_{CC(RXOUT)}$ and 5 V for the other supply pins. This reduces dissipation. Each supply line ($V_{CC(TXCORE)}$, $V_{CCD(SYN)}$, $V_{CCA(SYN)}$, $V_{CC(TXOUT)}$, $V_{CC(RXCORE)}$, $V_{CC(RXOUT)}$ and $V_{CC(RXD)}$) must be connected to V_{CC} via an EMI line filter.
2. The PECL inputs are high impedance. The transmission lines should be terminated externally using an appropriate termination.

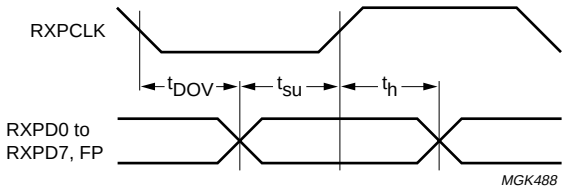
AC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
General						
$f_{c(VCO)}$	nominal VCO centre frequency		–	622.08	–	MHz
J_o	data output jitter	peak-to-peak value, in lock; note 1	–	–	0.06	UI
$REFCLK_{(tol)}$	reference clock frequency tolerance	required to meet SONET output frequency specification; note 1	–20	–	+20	ppm
δ	reference clock input duty factor		30	–	70	%UI
t_r, t_f	rise/fall time					
	reference clock	10 to 90%	–	–	2.0	ns
	PECL output	20% to 80%; 50 Ω load to V_{CC} – 2.0 V; 5 pF capacitor	–	220	450	ps
Receiver timing (see Figs. 6 and 7)						
δ	RXPCLK duty factor		40	50	60	%
t_{DOV}	data output valid time; RXPCLK LOW to RXPDn	valid propagation delay at STM1/OC3, 8-bit	–23.7	–	+21.7	ns
		valid propagation delay at STM1/OC3, 4-bit	–10.9	–	+8.9	ns
		valid propagation delay at STM4/OC12, 8-bit	–4.5	–	+2.5	ns
		valid propagation delay at STM4/OC12, 4-bit	tbf	–	tbf	ns
t_{su}	set-up time					
	RXPDn, FP to RXPCLK		4	–	–	ns
	RXSD/RXSDQ to RXSCLK/RXSCLKQ		400	–	–	ps
t_h	hold time					
	RXPDn, FP to RXPCLK		2	–	–	ns
	RXSD/RXSDQ to RXSCLK/RXSCLKQ		400	–	–	ps

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Transmitter timing (see Figs. 8 and 9)						
f_{clk}	TXSCLK clock frequency (nominal 155.52 or 622.08 MHz)		–	622.08	640	MHz
δ	duty factor					
	TXSCLK		40	50	60	%
	TXPCLK		33	50	67	%
t_{su}	set-up time					
	TXPDn to TXPCLK		1.5	–	–	ns
	TXSD to TXSCLK		400	–	–	ps
t_h	hold time					
	TXPDn to TXPCLK		1.0	–	–	ns
	TXSD to TXSCLK		400	–	–	ps
t_{DOV}	data input valid time	valid propagation delay TXSCLK LOW to TXSD	–	–	440	ps

Note

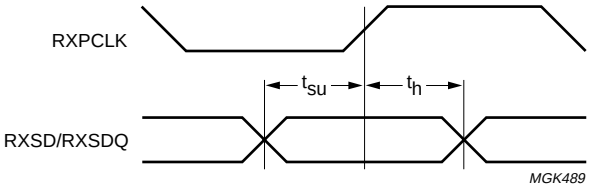
1. Jitter on REFCLK and REFCLKQ should be less than 84 ps (peak-to-peak) for STM4/OC12 operation or 336 ps (peak-to-peak) for STM1/OC3 operation, in a jitter frequency band from 12 kHz to 1 MHz.



Output propagation delay time of TTL outputs is the time in nanoseconds from the 50% point of the reference signal to the 30% or 70% point of the output.

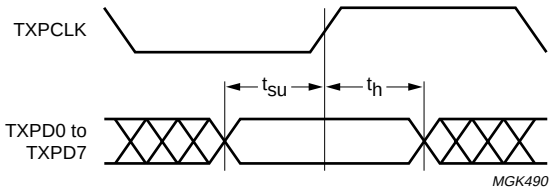
Maximum output propagation delays and duty cycles of TTL outputs are measured with a 15 pF load.

Fig.6 Receiver output timing.



Timing is measured from the cross-over point of the reference signal to the cross-over point of the input.

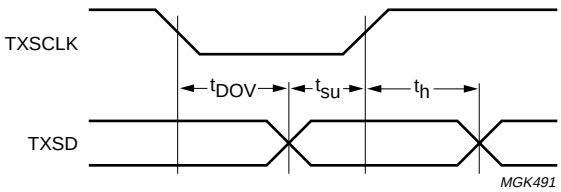
Fig.7 Receiver input timing.



When a set-up time is specified on TTL signals between an input and a clock, the set-up time in picoseconds from the 50% point of the input to the 50% point of the clock.

When a hold time is specified on TTL signals between an input and a clock, the hold time is the time in picoseconds from the 50% point of the clock to the 50% point of the input.

Fig.8 Transmitter input timing.



Timing is measured from the cross-over point of the reference signal to the cross-over point of the output.

Fig.9 Transmitter output timing.

APPLICATION INFORMATION

It is sometimes necessary to ‘forward clock’ data in an SDH/SONET system. When this is the case, the parallel data clock and the reference clock from which the high speed serial clock is synthesized will both originate from the same (usually TTL/CMOS) clock source. The following sections explain how to configure the TZA3005 to operated in this mode.

Clock control logic description

The timing control logic in the TZA3005 automatically generates an internal load signal with a fixed relationship to the reference clock. The logic takes into account the variation between the reference clock and the internal load signal over temperature and voltage.

The connections required to implement the design are shown in Fig.10, and the timing specifications are shown in Fig.11. The specified set-up and hold times must be met by the controller ASIC. It is recommended to latch the data on the falling edge of the reference clock in order to satisfy the appropriate specifications.

PECL output termination

The PECL outputs have to be terminated with 50 Ω to VCC – 2.0V. If this voltage is not available, a Thevenin termination can be used as shown in Fig.11.

Reference clock

Reference clock jitter must be minimized to ensure SONET jitter generation specifications are met. It may prove difficult to meet these specifications if a TTL source is used for the reference clock.

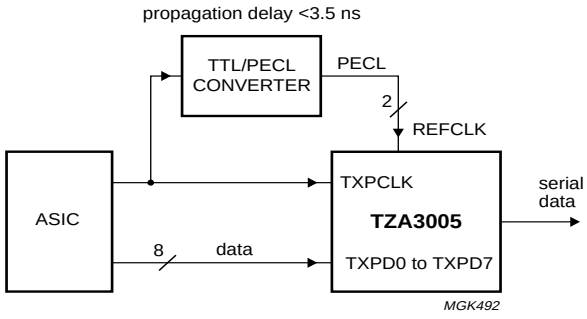


Fig.10 TZA3005 with data clocked by reference clock.

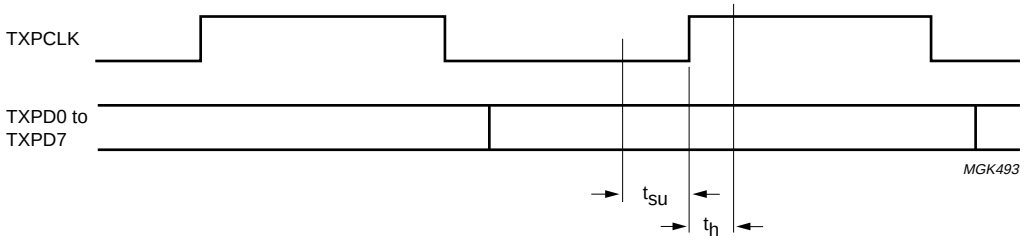


Fig.11 Data timing with respect to reference clock.

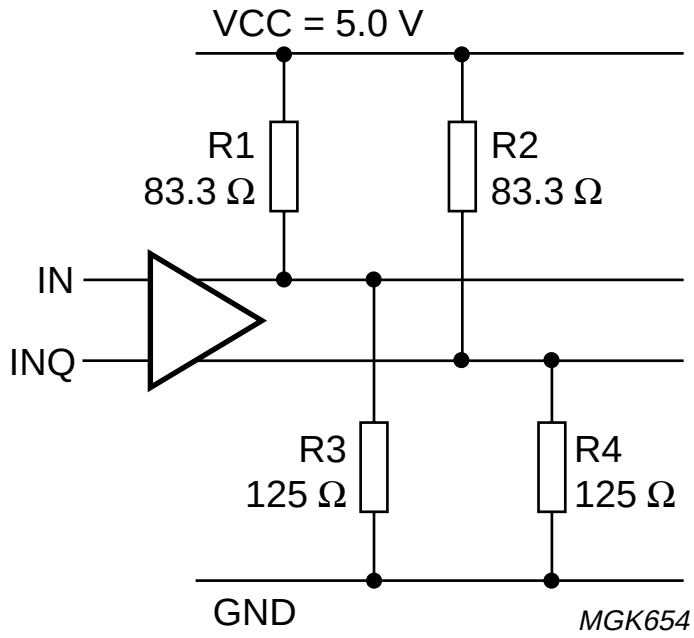


Fig.12 PECL output termination schemes.

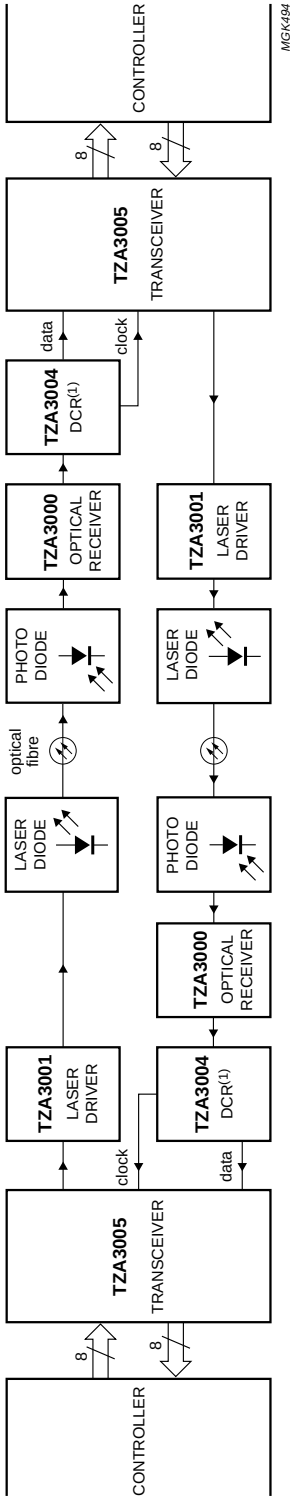
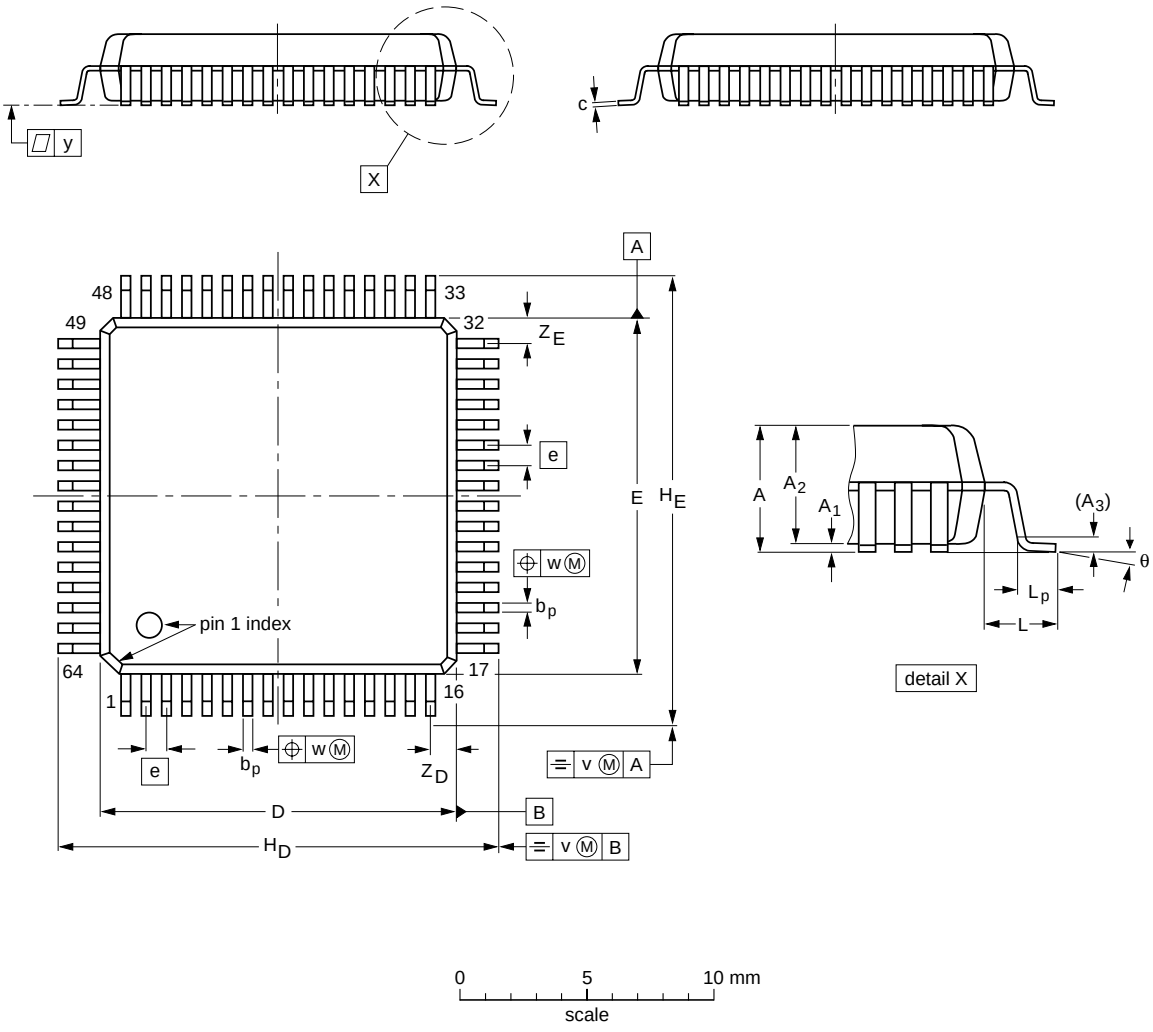


Fig.13 Application diagram.

(1) Data and Clock Recovery unit.

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.00	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.60	1.03 0.73	0.16	0.16	0.10	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT393-1		MS-022				~~96-05-21~~ 97-08-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands 427027/200/01/pp24 Date of release: 1997 Aug 05 Document order number: 9397 750 01745

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