

SWITCHING P-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2711GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

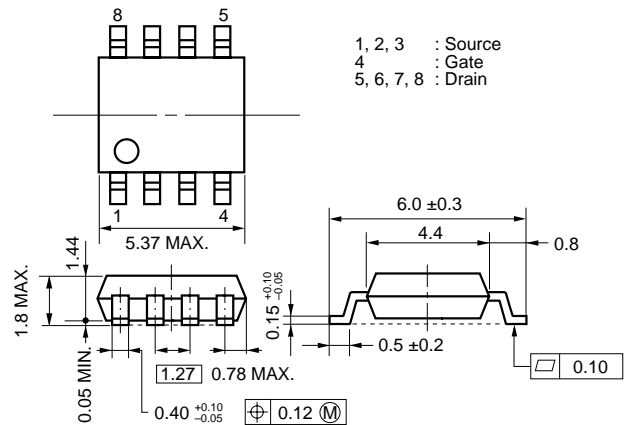
FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 9 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -6.5 \text{ A)}$
 $R_{DS(on)2} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -6.5 \text{ A)}$
 $R_{DS(on)3} = 20 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -6.5 \text{ A)}$
- Low C_{iss} : $C_{iss} = 2450 \text{ pF TYP.}$
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2711GR	Power SOP8

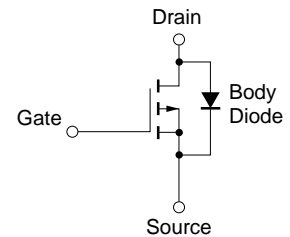
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise noted, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 13	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 52	A
Total Power Dissipation ^{Note2}	P_{T1}	2	W
Total Power Dissipation ^{Note3}	P_{T2}	2	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note4}	I_{AS}	-13	A
Single Avalanche Energy ^{Note4}	E_{AS}	16.9	mJ

EQUIVALENT CIRCUIT



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

3. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm), $PW = 10 \text{ sec}$

4. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -15 \text{ V}$, $R_G = 25 \Omega$, $L = 100 \mu\text{H}$, $V_{GS} = -20 \rightarrow 0 \text{ V}$

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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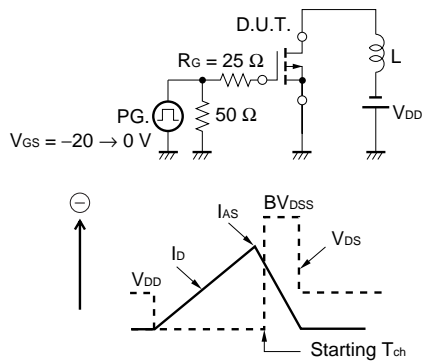
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ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless otherwise noted, All terminals are connected.)

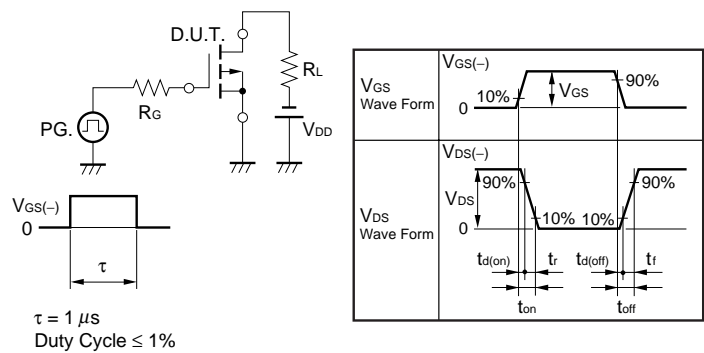
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{bss}	V _{DS} = -30 V, V _{GS} = 0 V			-1	μA
Gate Leakage Current	I _{gss}	V _{GS} = ±20 V, V _{DS} = 0 V			±100	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = -10 V, I _D = -1 mA	-1.0		-2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = -10 V, I _D = -6.5 A	10	22		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = -10 V, I _D = -6.5 A		7.4	9	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -6.5 A		10	15	mΩ
	R _{DS(on)3}	V _{GS} = -4.0 V, I _D = -6.5 A		12	20	mΩ
Input Capacitance	C _{iss}	V _{DS} = -10 V		2450		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		740		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		410		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = -15 V, I _D = -6.5 A		10		ns
Rise Time	t _r	V _{GS} = -10 V		15		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		230		ns
Fall Time	t _f			130		ns
Total Gate Charge	Q _G	V _{DD} = -24 V		57		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V		6.3		nC
Gate to Drain Charge	Q _{GD}	I _D = -13 A		19		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 13 A, V _{GS} = 0 V		0.81		V
Reverse Recovery Time	t _{rr}	I _F = 13 A, V _{GS} = 0 V		62		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		31		nC

Note Pulsed

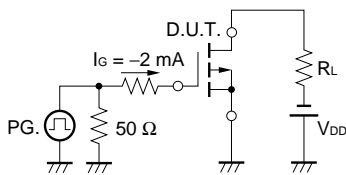
TEST CIRCUIT 1 AVALANCHE CAPABILITY



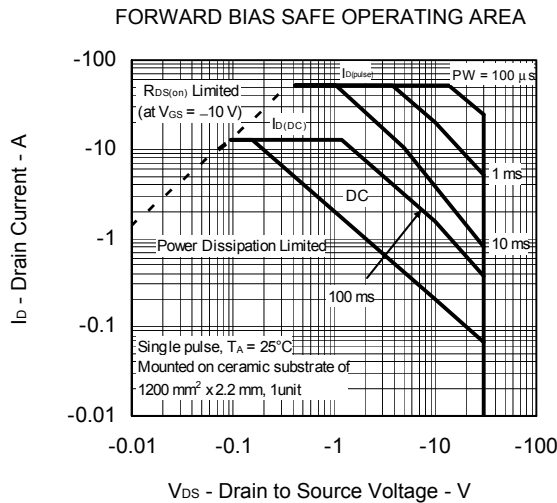
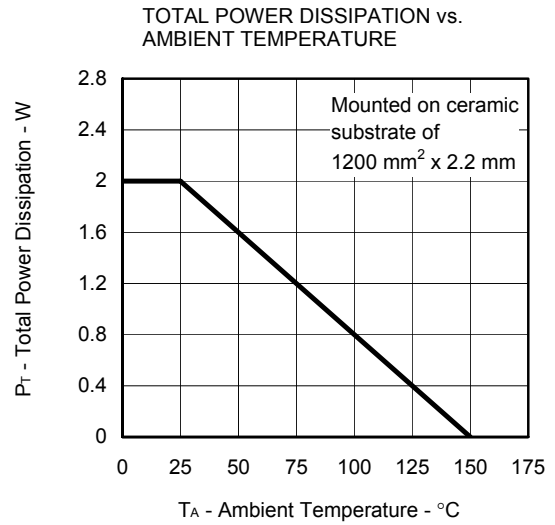
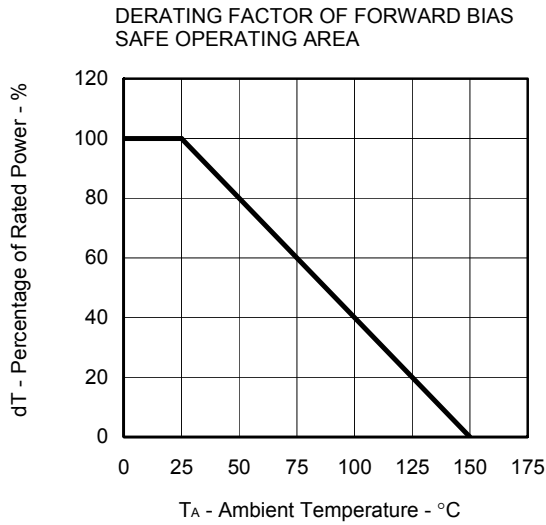
TEST CIRCUIT 2 SWITCHING TIME



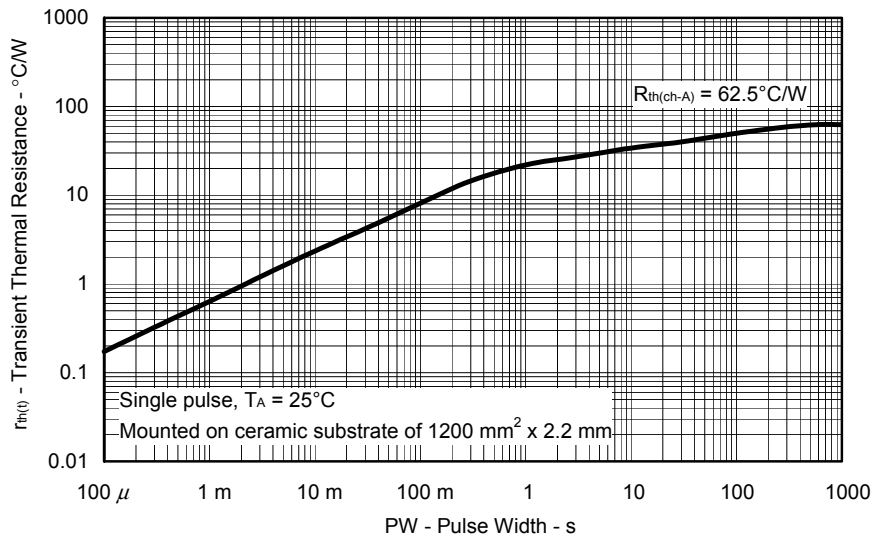
TEST CIRCUIT 3 GATE CHARGE



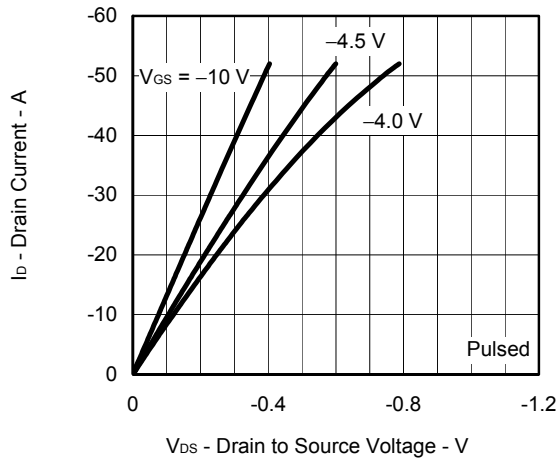
ELECTRICAL CHARACTERISTICS (T_A = 25°C)



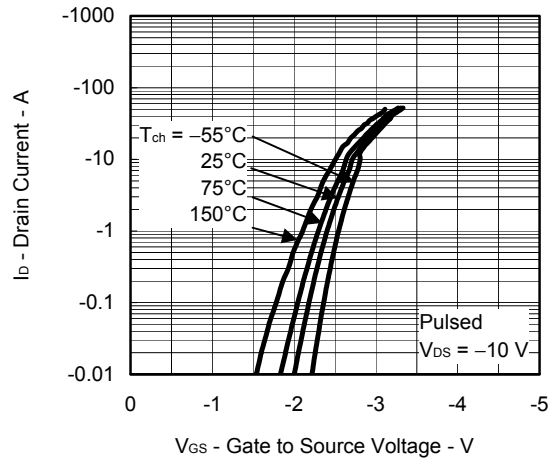
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



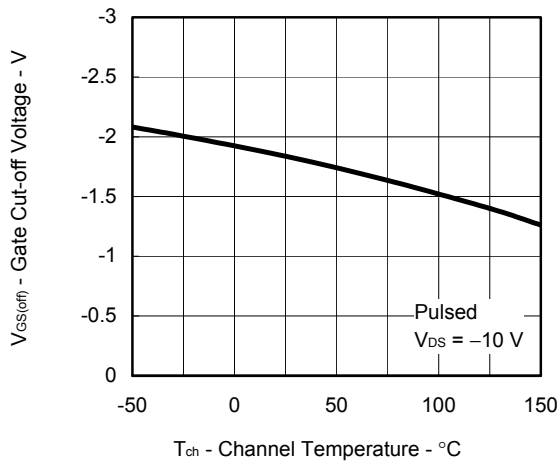
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



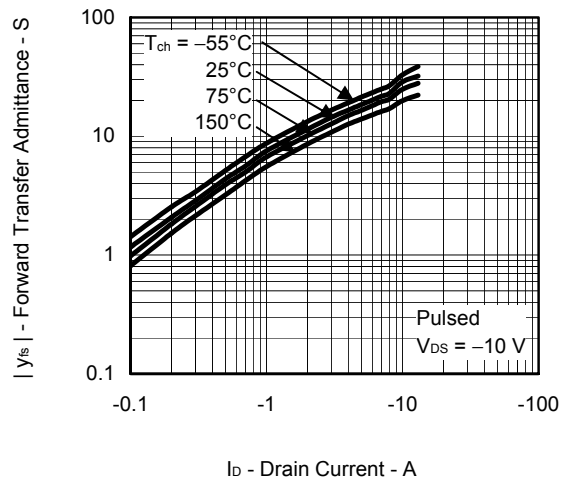
FORWARD TRANSFER CHARACTERISTICS



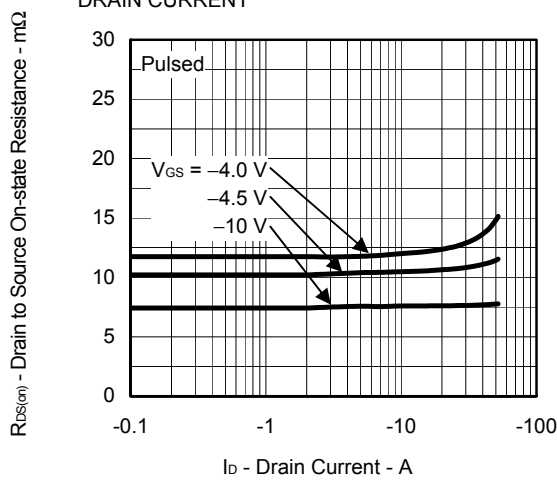
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



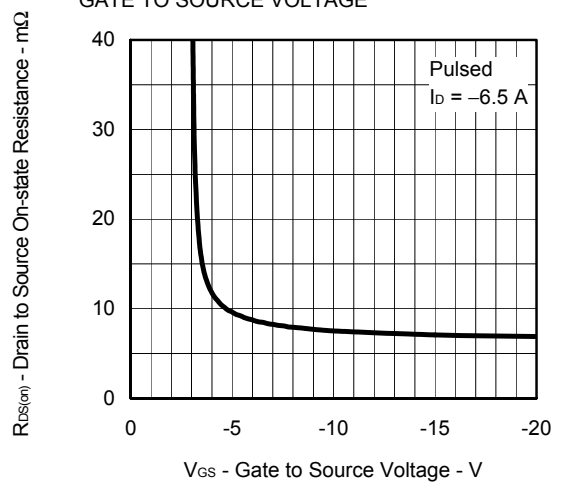
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

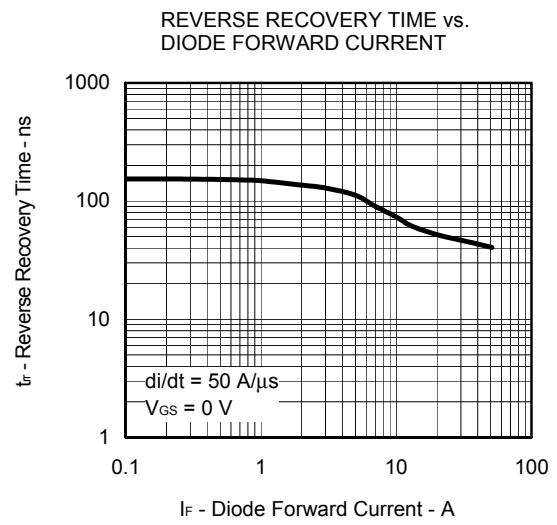
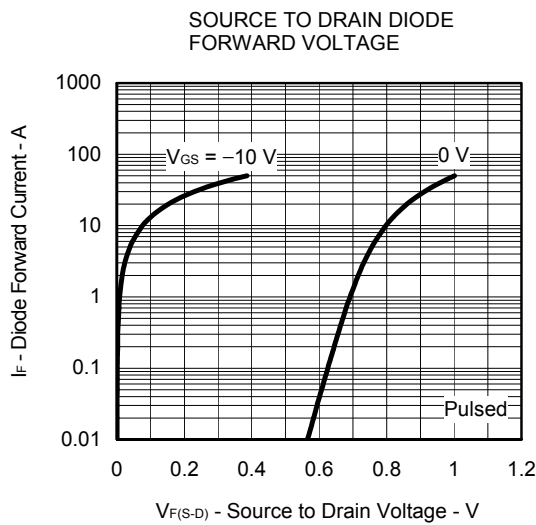
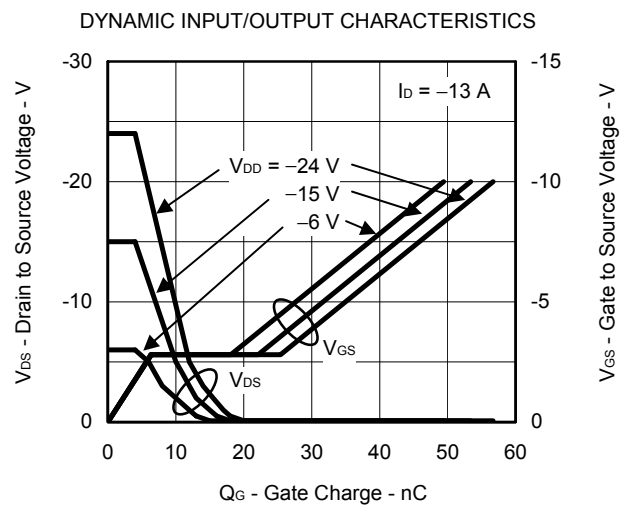
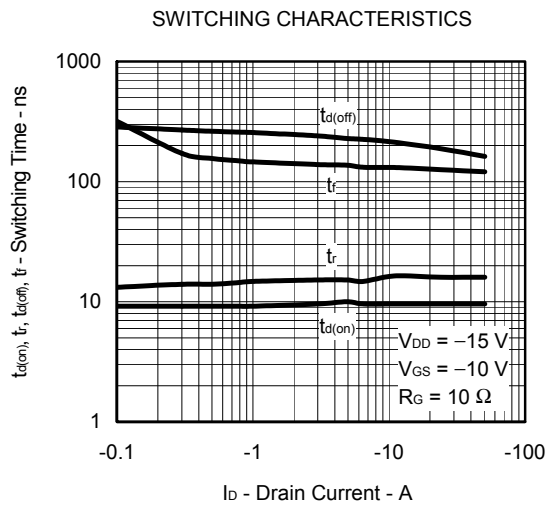
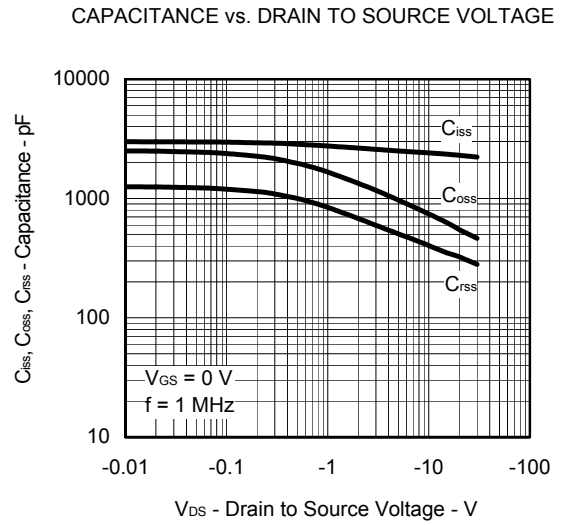
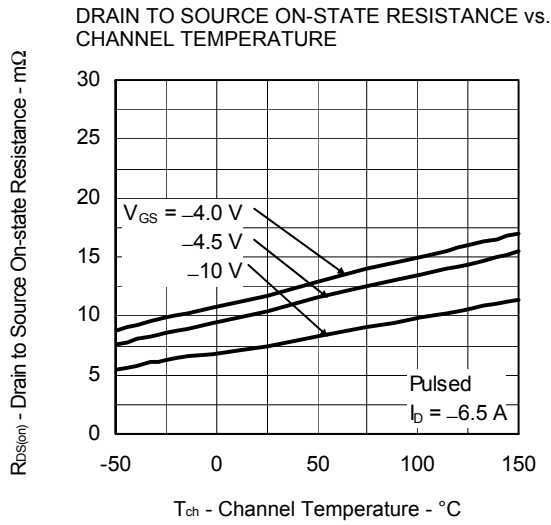


DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

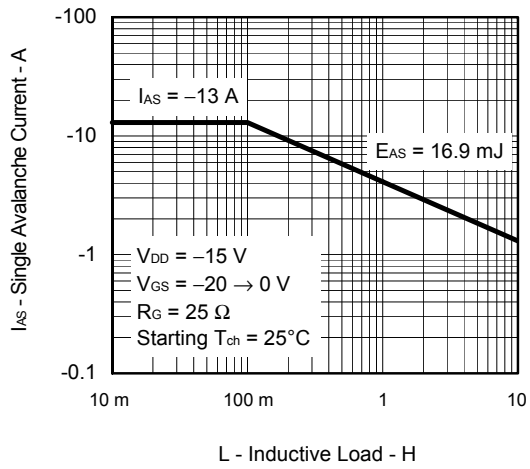


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

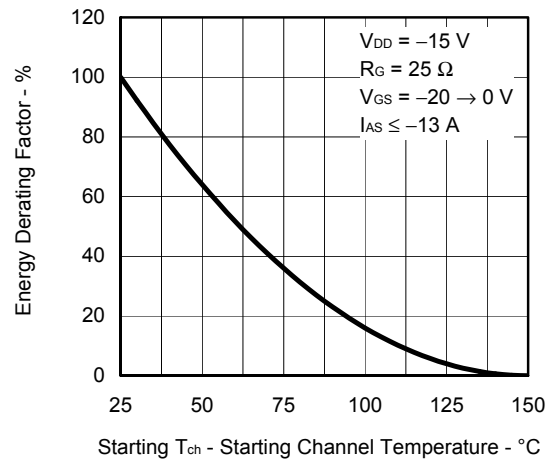




SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



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