DATA SHEET

MOS FIELD EFFECT TRANSISTOR
μPA2711GR

SWITCHING
P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2711GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

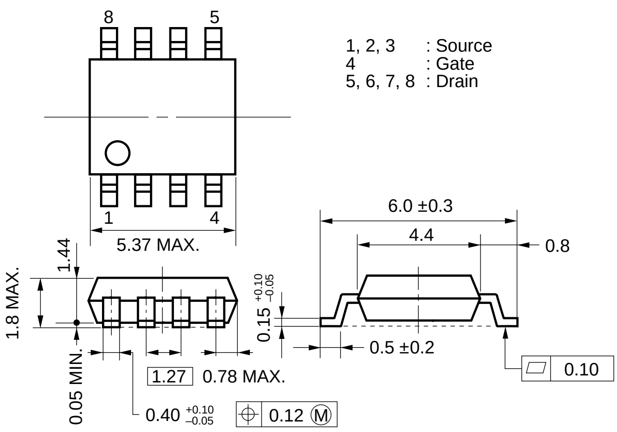
FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 9 mΩ MAX. (V_{GS} = –10 V, I_D = –6.5 A)
  $R_{DS(on)2}$ = 15 mΩ MAX. (V_{GS} = –4.5 V, I_D = –6.5 A)
  $R_{DS(on)3}$ = 20 mΩ MAX. (V_{GS} = –4.0 V, I_D = –6.5 A)
- Low C_{iss}: C_{iss} = 2450 pF TYP.
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2711GR	Power SOP8

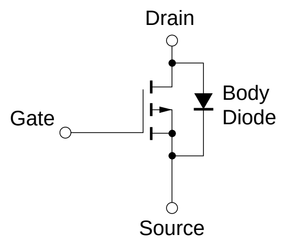
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, Unless otherwise noted, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC)	$I_{D(DC)}$	∓13	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓52	A
Total Power Dissipation Note2	P_{T1}	2	W
Total Power Dissipation Note3	P_{T2}	2	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to + 150	°C
Single Avalanche Current Note4	I_{AS}	–13	A
Single Avalanche Energy Note4	E_{AS}	16.9	mJ

EQUIVALENT CIRCUIT



Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%
2. Mounted on ceramic substrate of 1200 mm^2 x 2.2 mm
3. Mounted on a glass epoxy board (1 inch x 1 inch x 0.8 mm), PW = 10 sec
4. Starting T_{ch} = 25°C, V_{DD} = –15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = –20 → 0 V

Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

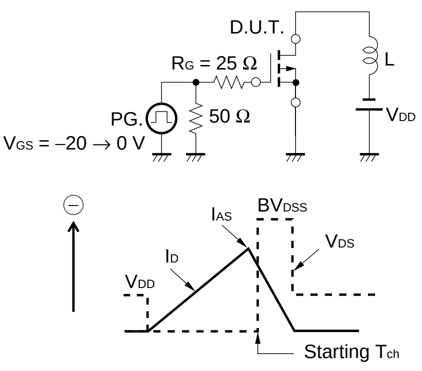
Document No. G15979EJ1V0DS00 (1st edition)
Date Published March 2004 NS CP(K)
Printed in Japan

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless otherwise noted, All terminals are connected.)

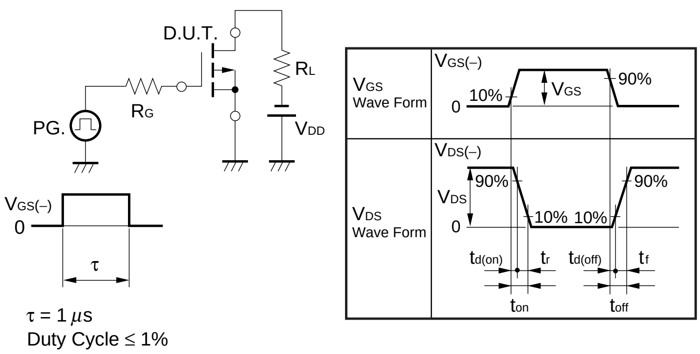
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓100	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0		–2.5	V
Forward Transfer Admittance Note	| y_{fs} |	V_{DS} = –10 V, I_D = –6.5 A	10	22		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –6.5 A		7.4	9	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –6.5 A		10	15	mΩ
	$R_{DS(on)3}$	V_{GS} = –4.0 V, I_D = –6.5 A		12	20	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V		2450		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		740		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		410		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –15 V, I_D = –6.5 A		10		ns
Rise Time	t_r	V_{GS} = –10 V		15		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		230		ns
Fall Time	t_f			130		ns
Total Gate Charge	Q_G	V_{DD} = –24 V		57		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		6.3		nC
Gate to Drain Charge	Q_{GD}	I_D = –13 A		19		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 13 A, V_{GS} = 0 V		0.81		V
Reverse Recovery Time	t_{rr}	I_F = 13 A, V_{GS} = 0 V		62		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 50 A/μs		31		nC

Note Pulsed

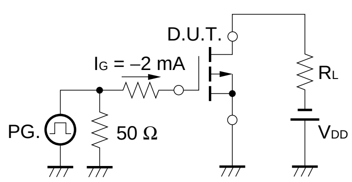
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

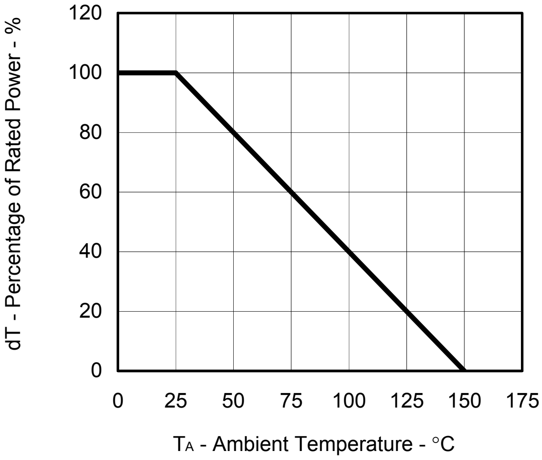


TEST CIRCUIT 3 GATE CHARGE

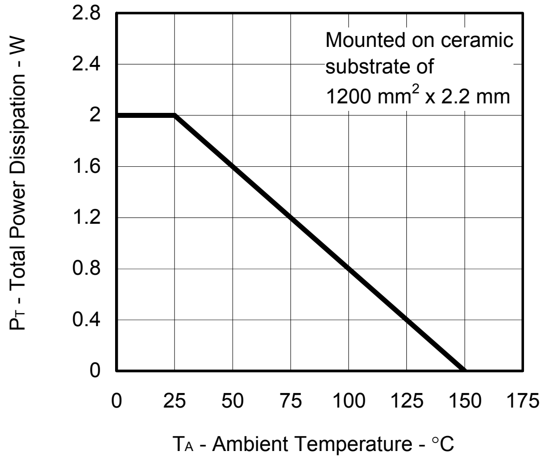


ELECTRICAL CHARACTERISTICS (T_A = 25°C)

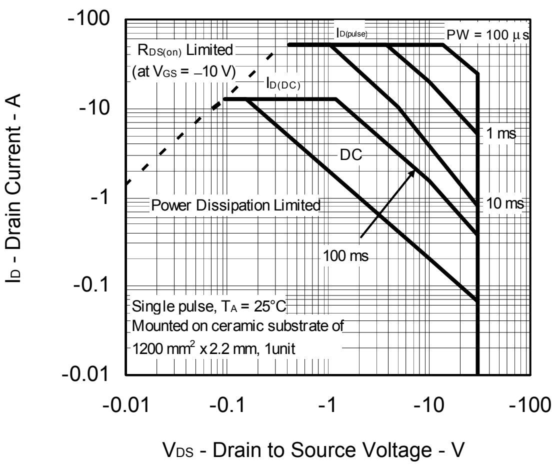
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



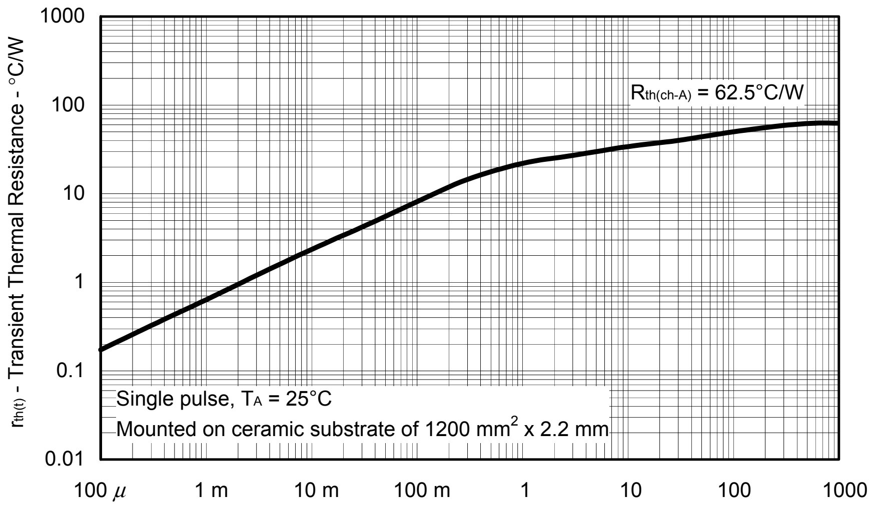
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



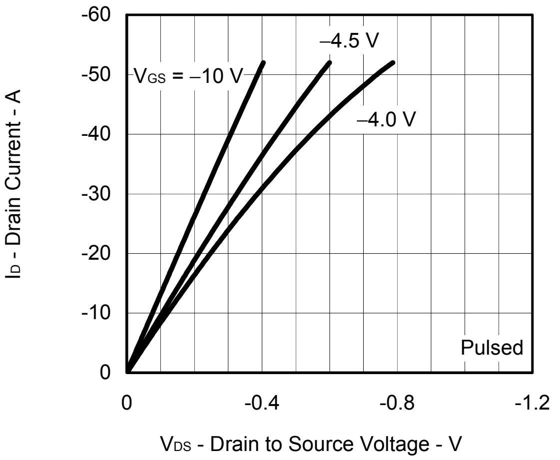
FORWARD BIAS SAFE OPERATING AREA



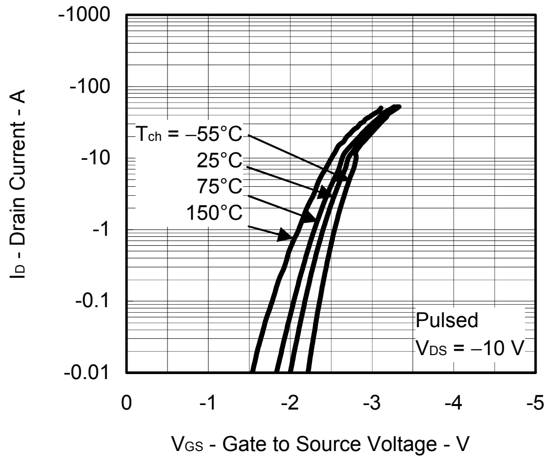
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



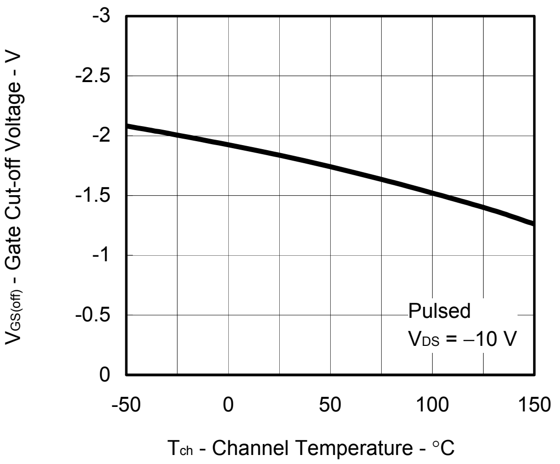
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



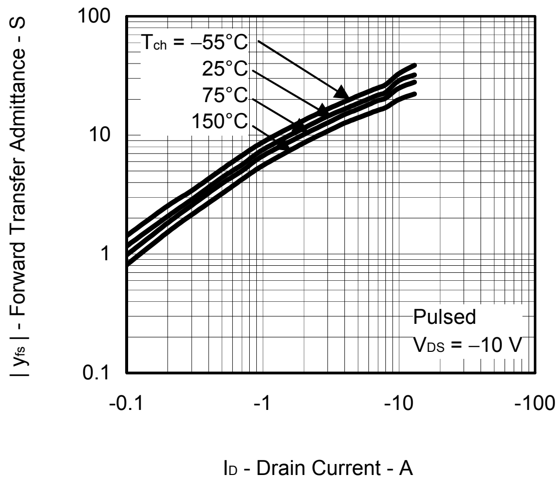
FORWARD TRANSFER CHARACTERISTICS



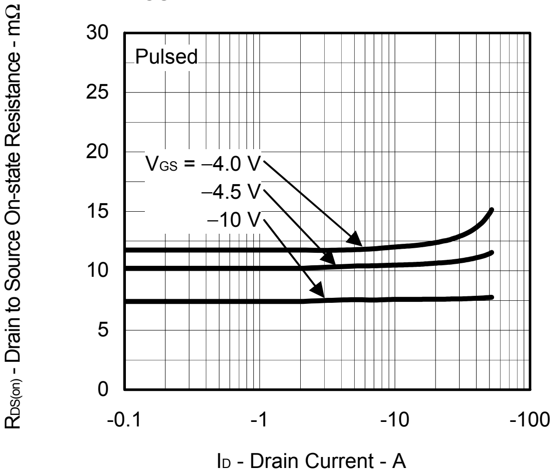
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



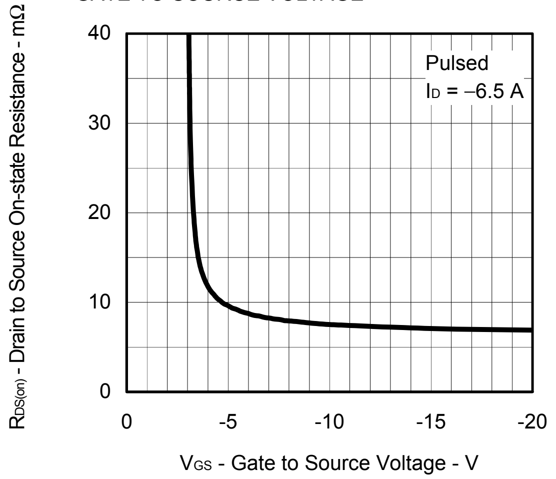
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



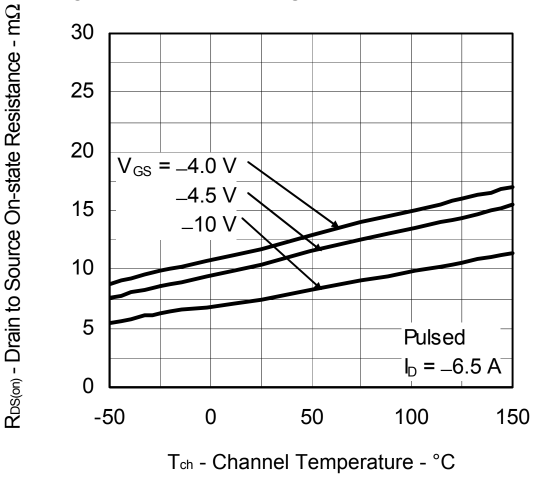
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



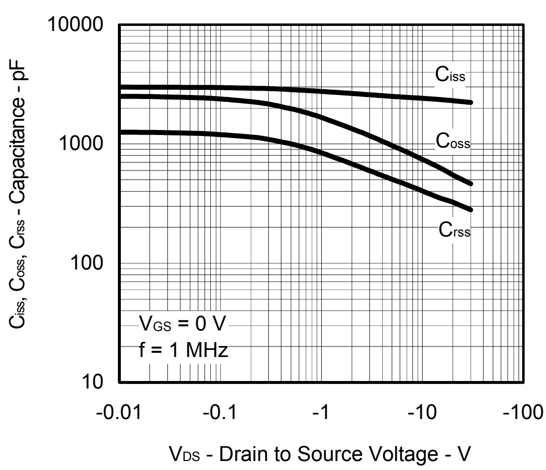
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



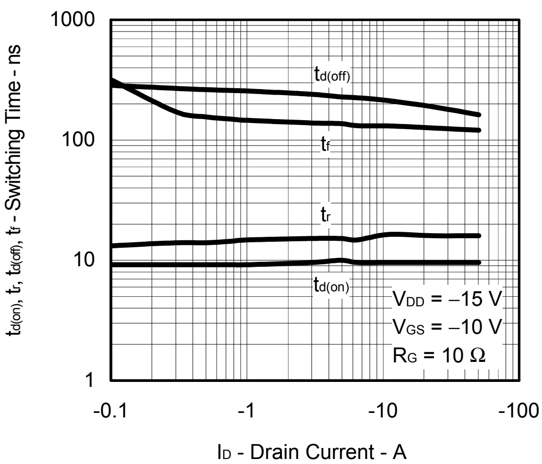
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



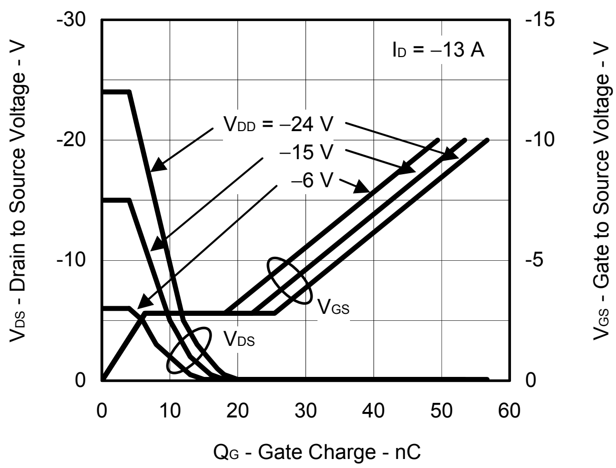
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



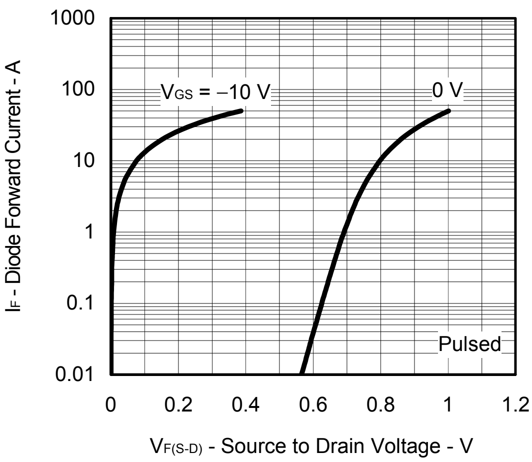
SWITCHING CHARACTERISTICS



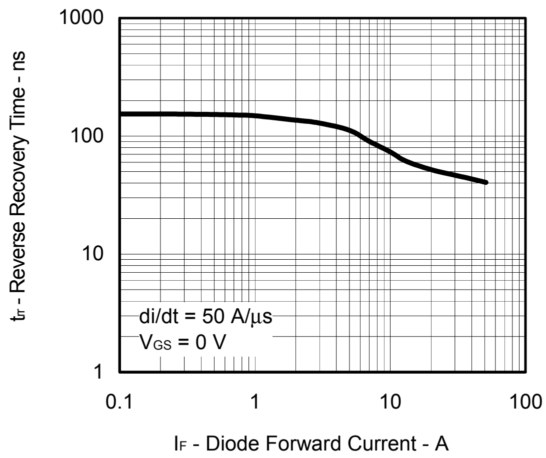
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



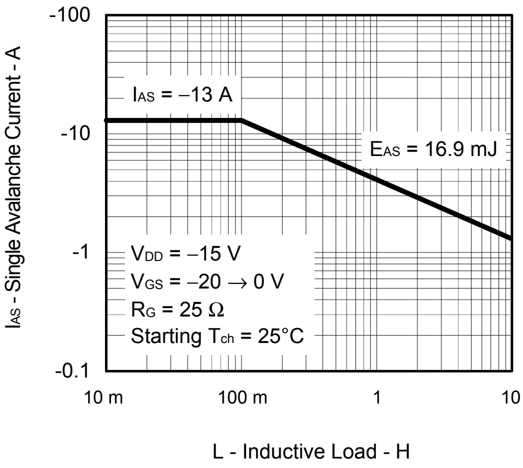
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR