1.0 Key Features

- Next-generation 0.15µm hybrid structured ASIC
- Platform for high-performance 1.5V/1.2V ASICs and FPGA-to-ASIC conversions
- NRE and production cost savings
- Significant time-to-market advantages
- Drop-in replacement for cost-reducing Xilinx® Virtex-II and Virtex-II Pro and Altera® APEX-II and Stratix designs
- 417K to 3.9M ASIC gates
- 210MHz system, 500MHz local clock speeds
- Low power consumption (0.055µW/MHz/gate @ 1.575V)
- 332Kbits to 4.8Mbits of block RAM memory
- Up to 5.6Mbits of memory when 50 percent of the logic sites are used for distributed memory
- 18Kbit initializable dual-port RAM blocks at speeds up to 330MHz
- Flexible I/O technology, any I/O standard assigned to any I/O pin
- Initializable distributed memory at speeds up to 210MHz
- Configurable signal, core and I/O power supply pin locations
- Supports LVTTL, LVCMOS, PCI33, PCI66, PCI-X 133, PCI-X 2.0, GTL/+, HSTL class 1, 2, 3, and 4, SSTL2 class 1 and 2, LVPECL (input), LVDS I/O standards
- 1.5V, 1.8V, 2.5V, and 3.3V capable I/O
- True 3.3V tolerance with no external resistor necessary
- Digital controlled impedance
- Built-in DDR support
- LVDS data rates to 1Gbps
- Up to 1346 user I/Os
- Comprehensive clock management circuitry
- Up to eight DLLs and eight PLLs
- Variety of package options
- Integrated high-fault coverage scan-test, memory BIST and JTAG

2.0 Product Description

Targeted at medium-density, high-speed, 1.5V and 1.2V ASIC applications and high-density FPGA-to-ASIC conversions, the XPressArray™-II 0.15µm hybrid structured ASIC is an innovative next-generation technology platform that reduces time-to-market for system-on-chip (SoC) applications while delivering significant NRE and unit cost savings.

XPressArray-II offers a true drop-in replacement for Xilinx Virtex-II, Virtex-II Pro, Altera APEX-II, and Stratix FPGAs, making it the industry's lowest cost ASIC conversion solution. The result is a simplified route to cost reductions for OEMs looking to combine the flexibility of FPGA prototyping with a path to an ASIC for final production.

Table 1 shows the seven bases of the AMIS XPressArray-II family. These bases offer between 417K and 3.9M gates. Configurable memory ranges from 332Kbits to 4.8Mbits, which increases to 5.6Mbits of memory with the addition of distributed configurable memory, assuming 50 percent of the logic sites are used for memory. Individual memories may be configured as single or dual port with asymmetrical port widths. The architecture also supports memory initialization.

Flexible I/O technology includes support for a comprehensive array of common standards and compatibility with 1.5V, 1.8V, 2.5V, and 3.3V I/O schemes. I/O power supply banking supports the operating voltage requirements of multiple I/O standards on the same device. Each XPressArray-II I/O may be configured to support LVTTL, LVCMOS, PCI33, PCI66, PCI-X 133, PCI-X 2.0, GTL/+, HSTL class 1, 2, 3, and 4, SSTL2 class 1 and 2, LVPECL input, and LVDS. I/Os support digital controlled impedance (DCI) on-chip termination. Dual data rate (DDR) support for high-speed memory interface is built in.

Table 1: XPressArray-II 0.15µm Hybrid Structured ASIC Family

		No Distributed RAM		50% Distributed RAM				
XPressArray-II Base	18K RAM Blocks	Bits(K)[1]	Gates(K)[2]	Bits(K)[1]	Gates(K)[2]	DLL	PLL	User I/Os
X2P376	18	332	417	415	209	2	4	376
X2P528	40	737	650	867	325	2	4	528
X2P680	57	1051	1203	1291	602	4	4	680
X2P846	101	1862	1629	2188	815	4	4	846
X2P998	145	2673	2196	3112	1098	4	4	998
X2P1148	189	3484	2902	4064	1451	8	8	1148
X2P1346	264	4866	3929	5652	1965	8	8	1346

(1) Usable 2RW RAM bits
(2) Usable 2-NAND equivalent logic gates

Comprehensive clock management circuitry features up to eight all digital delay-locked loops (DLLs) and a maximum of eight phase-locked loops (PLLs). High fault coverage is provided through integrated scan-test, memory BIST and JTAG support.

Package offerings include traditional plastic BGA and flip-chip BGA in 1.00mm and 1.27mm pitches. Because XPressArray-II devices consume significantly less power than equivalent FPGAs, lower cost plastic packaging can be used in most cases. Table 2 shows the supported package configurations. Packaging options exist to optimize individual conversions.

Table 2: XPressArray-II Package Options

Pins	Description	Pitch (mm)	Size (mm)	Max I/Os
256 FBGA	256 Fine Pitch Ball Grid Array	1.0	17x17	187
456 FBGA	456 Fine Pitch Ball Grid Array	1.0	23x23	344
484 FBGA	484 Fine Pitch Ball Grid Array	1.0	23x23	369
575 PBGA	575 Standard Ball Grid Array	1.27	31x31	423
672 FBGA	672 Fine Pitch Ball Grid Array	1.0	27x27	521
672 PBGA	672 Standard Ball Grid Array	1.27	35x35	514
672 FFBGA	672 Flip-Chip Fine Pitch Ball Grid Array	1.0	27x27	459
676 FBGA	676 Fine Pitch Ball Grid Array	1.0	27x27	500
724 PBGA	724 Standard Ball Grid Array	1.27	35x35	564
728 PBGA	728 Standard Ball Grid Array	1.27	35x35	531
780 FBGA	780 Fine Pitch Ball Grid Array	1.0	29x29	675
896 FFBGA	896 Flip-Chip Fine Pitch Ball Grid Array	1.0	31x31	639
956 PBGA	956 Standard Ball Grid Array	1.27	40x40	747
957 BFBGA	957 Flip-Chip Standard Pitch Ball Grid Array	1.27	40x40	699
1020 FBGA	1020 Fine Pitch Ball Grid Array	1.0	33x33	859
1148 FFBGA	1148 Flip-Chip Fine Pitch Ball Grid Array	1.0	35x35	819
1152 FFBGA	1152 Flip-Chip Fine Pitch Ball Grid Array	1.0	35x35	839
1508 FBGA	1508 Fine Pitch Ball Grid Array	1.0	40x40	1267
1517 FFBGA	1517 Flip-Chip Fine Pitch Ball Grid Array	1.0	40x40	1123
1696 FFBGA	1696 Flip-Chip Fine Pitch Ball Grid Array	1.0	42.5x42.5	1179
1704 FFBGA	1704 Flip-Chip Fine Pitch Ball Grid Array	1.0	42.5x42.5	1131

For FPGA conversions, rapid access to XPressArray-II technology can be achieved via AMI Semiconductor's NETRANS® conversion methodology. Alternatively, the availability of XPressArray-II synthesis libraries for leading commercial synthesizers allows conversion of FPGA designs to an ASIC by simply re-targeting from an FPGA library to an XPressArray-II library.

3.0 The Advantages of XPressArray-II

XPressArray-II technology is ideal for medium density ASIC applications requiring high-performance and low power, with 1.5V/1.2V operation. XPressArray-II devices are fabricated using a hybrid technology that integrates an established 0.15µm front-end process with a proven AMIS metal finishing technology, which is used to produce a customized back-end. The 0.15µm processing steps are common to multiple applications, reducing costs by allowing existing tooling to be utilized. At the same time, tooling and manufacturing costs are significantly lower for the metal finishing process than for traditional 0.15µm cell based processes. The result is that XPressArray-II delivers reduced cycle times and significant reductions in terms of both NRE and unit cost through manufacturing utilizing structured ASIC technology.

The XPressArray-II architecture offers a unique solution to the challenges of maintaining FPGA process compatibility while delivering ASIC technology with reasonable NREs and low piece price. Compared to equivalent FPGAs, XPressArray-II devices operate at the same voltage, offer higher densities, better performance and consume less power. Figure 1 compares volume pricing for FPGA, cell-based ASIC and XPressArray-II devices. Figure 2 compares power consumption of these devices.

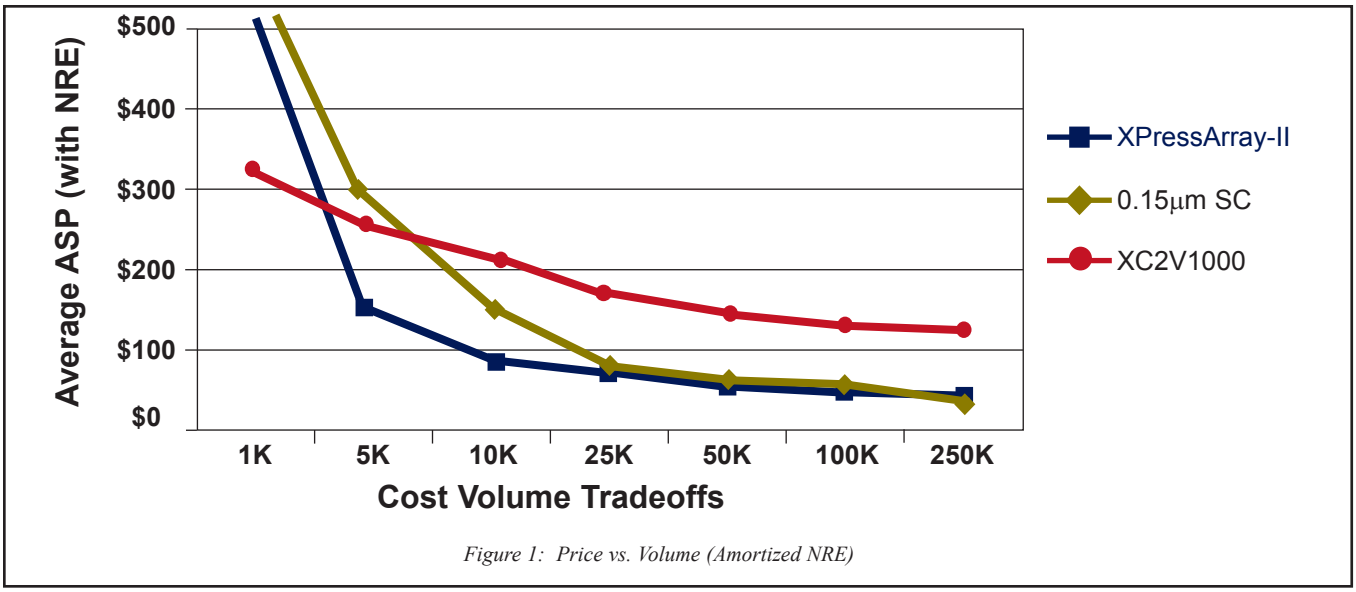

Figure 1: Price vs. Volume (Amortized NRE)

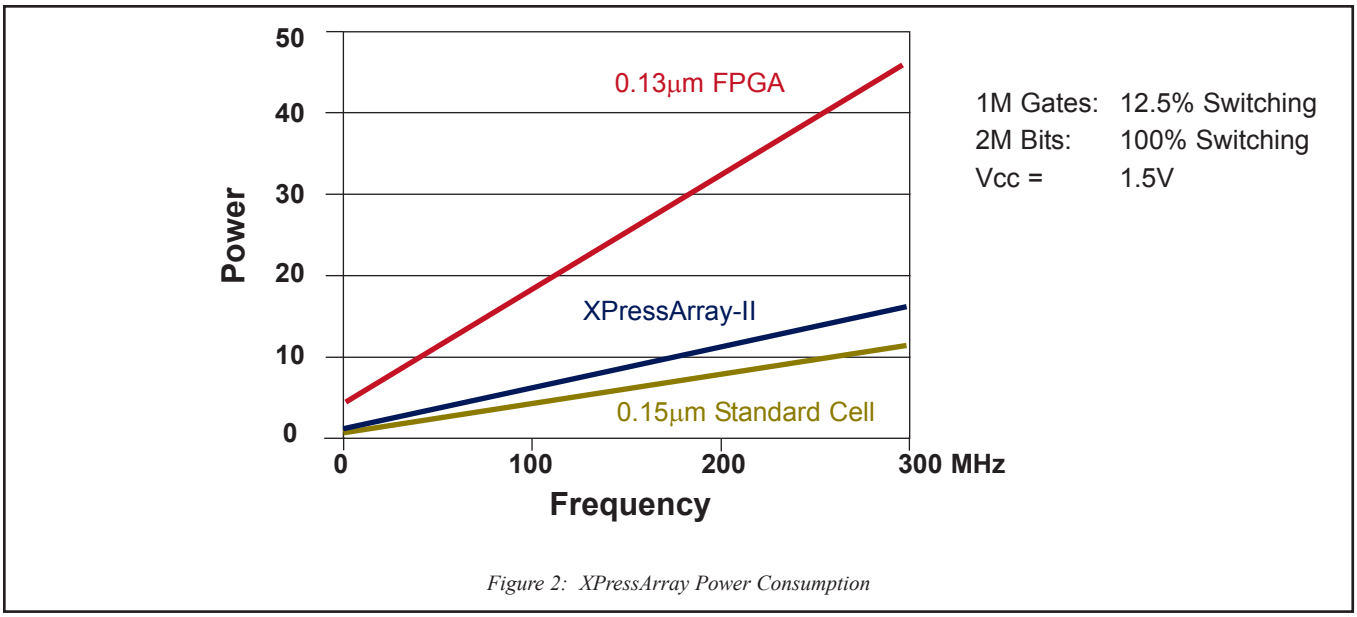

Figure 2: XPressArray Power Consumption

XPressArray-II provides a FPGA conversion platform combining advanced process capability with all of the key features of the Xilinx Virtex-II and Virtex-II Pro and Altera APEX-II and Stratix devices. Support for a comprehensive array of I/O standards, abundant configurable memory, high-density logic and advanced high-performance clock management, and frequency synthesis circuits round out the offering. XPressArray-II devices can be fabricated as pin-for-pin compatible FPGA drop-in replacements. Alternatively, multiple FPGAs can be combined into one XPressArray-II device, or die and package configurations can be optimized for specific requirements.

4.0 XPressArray-II Architecture

Figure 3 shows the XPressArray-II device architecture with embedded block RAMs, DCI, DDR support, DLLs, PLLs, and support for a full compliment of I/O standards.

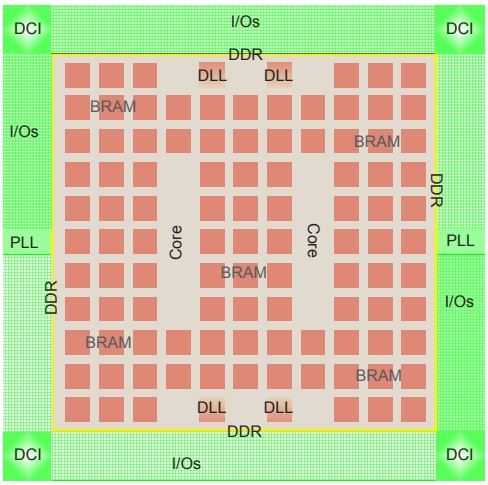

Figure 3: XPressArray-II Architecture

5.0 I/O Description

The XPressArray-II I/O ring is composed of uniform I/O cell sites and each site may be customized to support any I/O standard. The I/O power ring is divided into eight segments, making it compatible with the FPGA products and power supply rings built into the packages.

I/O cells are available for a wide variety of standards as listed in Table 3. I/O cells operate at 1.5V, 1.8V, 2.5V, and 3.3V. 3.3V tolerant I/Os are also available. Differential signaling standards typically require two pad sites. Signaling standards requiring a reference voltage typically share a common reference voltage within an I/O power ring segment, with the reference voltage being supplied through an I/O site from an off-chip source.

Figure 4 shows the architecture of the I/O cell. Included are programmable pull-up, pull-down resistors as well as a bus-hold latch to limit noise on tri-stated signal busses. Dedicated dual-data rate (DDR) flip-flops facilitate high-speed communications with I/O operating at up to 1Gbps using LVDS transceivers in conjunction with DLL/PLL clock management circuits.

Digital controlled impedance is available on many I/O standards to eliminate off-chip termination resistors. Figure 5 illustrates the termination schemes available on all XPressArray-II I/O cells.

Designers can use the DDR and DCI features of the XPressArray-II I/O cell for DDR SDRAM memory and parallel high-speed point-to-point interfaces.

Table 3: Supported I/O Standards

I/O Standard	VCCO	VCCAUX	Output Termination	Input Termination	Performance	Notes
LVTTL	3.3V		DCI Series Out 25Ω/50Ω		125MHz	2-24mA
LVCMOS33	3.3V		DCI Series Out 25Ω/50Ω		125MHz	2-24mA
LVCMOS25	2.5V		DCI Series Out 25Ω/50Ω		125MHz	2-24mA, 3.3V Tolerant
LVCMOS18	1.8V		DCI Series Out 25Ω/50Ω		125MHz	2-16mA, 3.3V Tolerant
LVCMOS15	1.5V		DCI Series Out 25Ω/50Ω		125MHz	2-16mA, 3.3V Tolerant
PCI33_3	3.3V				33MHz	
PCI66	3.3V				66MHz	
PCI-X 133	3.3V				133MHz	
PCI-X 2.0 Mode 1	3.3V				133MHz	
PCI-X 2.0 Mode 2	1.5V	3.3V		DCI Split Parallel in 114Ω	266/533Mbps	
GTL	N/A		DCI Parallel Out 50Ω		100MHz	
GTL+	N/A		DCI Parallel Out 50Ω		200MHz	
SSTL2 Class I	2.5V		DCI Parallel Out 25Ω	DCI Split Parallel in 100Ω	400Mbps	
SSTL2 Class II	2.5V		DCI Parallel Out 25Ω	DCI Split Parallel in 100Ω	400Mbps	
HSTL18 Class I	1.8V			DCI Split Parallel in 100Ω	500Mbps	
HSTL18 Class II	1.8V			DCI Split Parallel in 100Ω	500Mbps	
HSTL18 Class III	1.8V			DCI Parallel in 50Ω	500Mbps	
HSTL18 Class IV	1.8V	3.3V		DCI Parallel in 50Ω	500Mbps	
HSTL15 Class I	1.5V			DCI Split Parallel in 100Ω	500Mbps	
HSTL15 Class II	1.5V			DCI Split Parallel in 100Ω	500Mbps	
HSTL15 Class III	1.5V			DCI Parallel in 50Ω	500Mbps	
HSTL15 Class IV	1.5V	3.3V		DCI Parallel in 50Ω	500Mbps	
LVPECL (input)	3.3V			100Ω Differential Input	1Gbps	
LVDS33	3.3V			100Ω Differential Input	1Gbps	
LVDS25	2.5V			100Ω Differential Input	1Gbps	

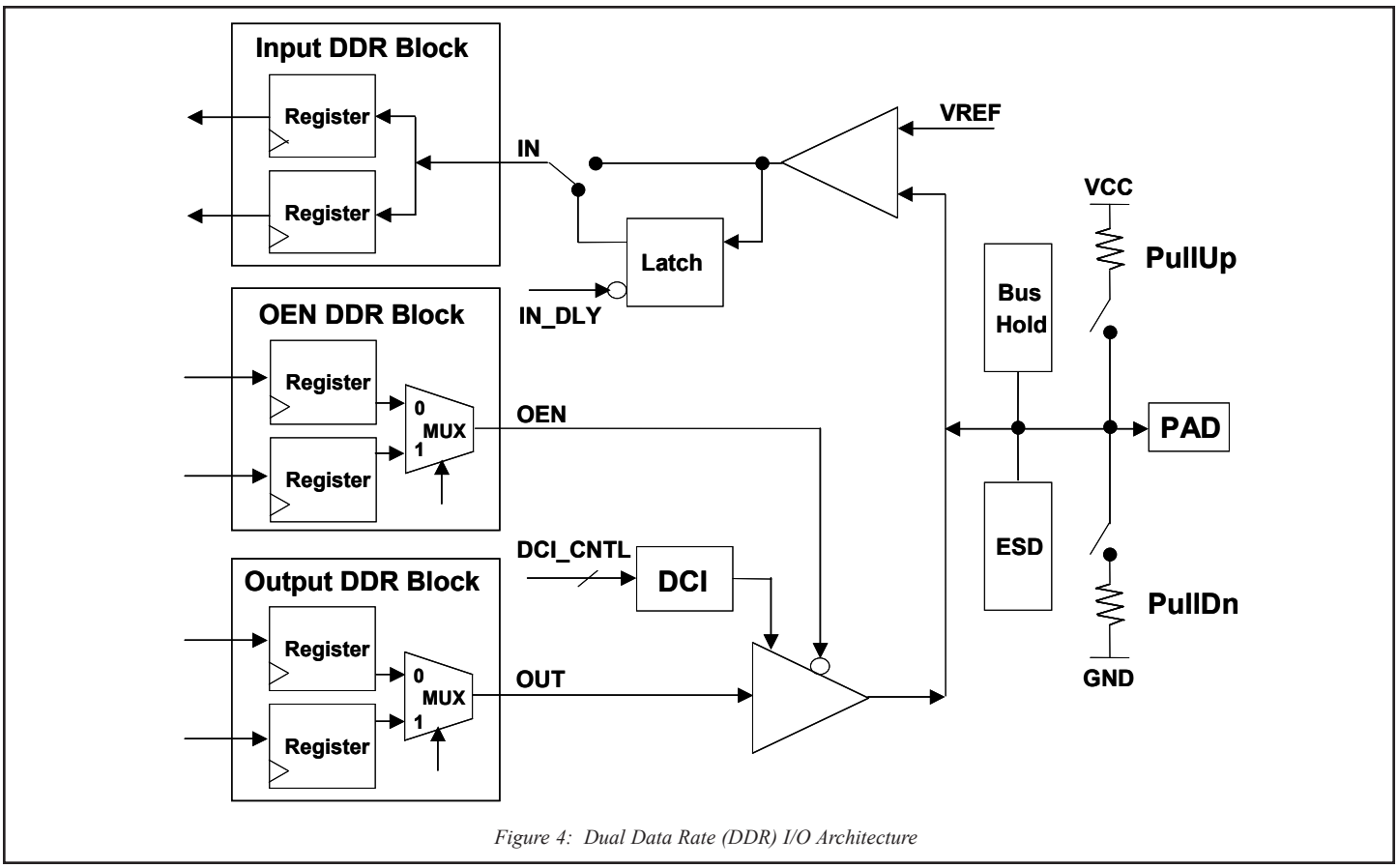

Figure 4: Dual Data Rate (DDR) I/O Architecture

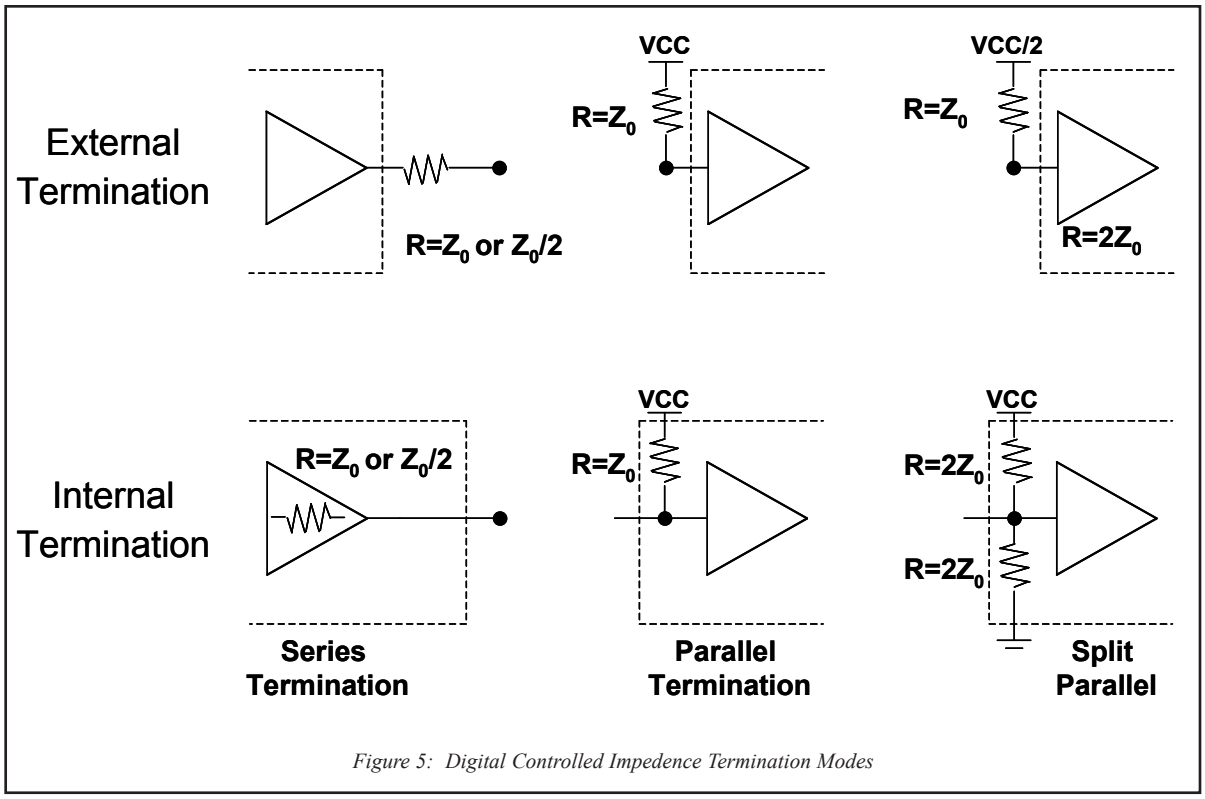

Figure 5: Digital Controlled Impedence Termination Modes

6.0 Memory Description

The XPressArray-II architecture supports abundant embedded block RAM as well as distributed RAM constructed from the structured ASIC logic fabric.

The XPressArray-II 18K embedded dual-port memory block provides drop-in replacement features for FPGA memories. Each memory is individually port configurable as 512x36, 1024x18, 2048x9, 4096x4, 8192x2, and 16384x1 as shown in Table 4. This fully synchronous memory supports read before write, write before read and write without read operational modes. XPressArray-II embedded RAM blocks may be configured as single-port (1RW), 2-port (1R1W) or true dual-port (2RW). Each RAM bit is initializable by a late metal mask option.

The XPressArray-II logic fabric is specifically designed to support distributed memories to replace FPGA memories created from LUTs. Pre-designed distributed memories are available in a range of sizes from 16x1 through 32x32 in 2-port (1R1W) configurations as shown in Table 5. Additional sizes and configurations, such as 2-read, 1-write (2R1W) configurations can also be constructed. Fully synchronous and synchronous-write, asynchronous read modes are available. Like the block RAM, each bit is initializable by a late metal mask option.

Table 4: Block RAM Configurations

Name	Port A Depth	Port A Data Width	Port A Parity Width	Port B Depth	Port B Width	Port B Parity Width
ra16_1_1_c	16,384	1	N/A	16,384	1	N/A
ra16_1_2_c	16,384	1	N/A	8,192	2	N/A
ra16_1_4_c	16,384	1	N/A	4,096	4	N/A
ra16_1_9_c	16,384	1	N/A	2,048	8	1
ra16_1_18_c	16,384	1	N/A	1,024	16	2
ra16_1_36_c	16,384	1	N/A	512	32	4
ra16_2_2_c	8,192	2	N/A	8,192	2	N/A
ra16_2_4_c	8,192	2	N/A	4,096	4	N/A
ra16_2_9_c	8,192	2	N/A	2,048	8	1
ra16_2_18_c	8,192	2	N/A	1,024	16	2
ra16_2_36_c	8,192	2	N/A	512	32	4
ra16_4_4_c	4,096	4	N/A	4,096	4	N/A
ra16_4_9_c	4,096	4	N/A	2,048	8	1
ra16_4_18_c	4,096	4	N/A	1,024	16	2
ra16_4_36_c	4,096	4	N/A	512	32	4
ra16_9_9_c	2,048	8	1	2,048	8	1
ra16_9_18_c	2,048	8	1	1,024	16	2
ra16_9_36_c	2,048	8	1	512	32	4
ra16_18_18_c	1,024	16	2	2,048	8	2
ra16_18_36_c	1,024	16	2	1,024	16	4
ra16_36_36_c	512	32	4	512	32	4

Table 5: Predefined Distributed RAMs

Name	Depth	Width
xram16x1pc	16	1
xram16x2pc	16	2
xram16x4pc	16	4
xram16x8pc	16	8
xram16x10pc	16	10
xram16x16pc	16	16
xram16x18pc	16	18
xram16x32pc	16	32
xram32x1pc	32	1
xram32x2pc	32	2
xram32x4pc	32	4
xram32x8pc	32	8
xram32x10pc	32	10
xram32x16pc	32	16
xram32x18pc	32	18
xram32x32pc	32	32

7.0 Delay-Locked Loop (DLL) Description

XPressArray-II devices employ clock tree synthesis, enabling an unlimited number of clock and reset signals to be routed. Synthesized clock trees deliver high speed clock signals with minimal skew and power.

The XPressArray-II DLL (Figure 6) is an all digital clock management function embedded into the XPressArray-II bases. DLLs may be used to minimize clock insertion delay, perform basic clock frequency synthesis and generate phase shifts. The DLL provides both coarse and fine-grained phase shifting with dynamic phase shift control. The quadrature clock generation features deliver accurate clock phases at the load, compensating for clock tree delays across the full range of temperature and voltage. In clock divider and clock doubling applications, duty cycle correction is available. A robust real-time lock detection circuit completes the DLL.

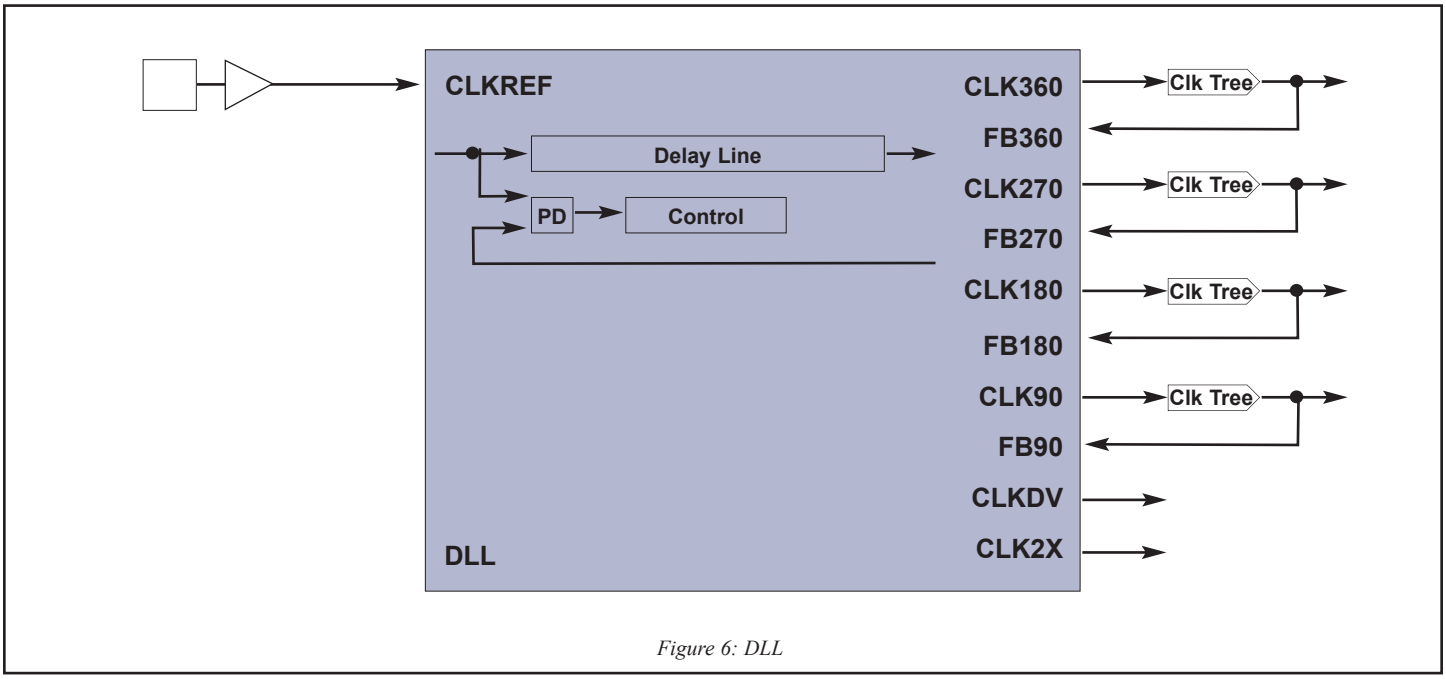

Figure 6: DLL

8.0 Phased-Locked Loop (PLL) Description

PLLs are embedded into the XPressArray-II bases to perform advanced clock frequency synthesis operations, minimize clock insertion delay and generate phase taps. Each PLL can be configured as a general purpose or LVDS PLL.

Figure 7 shows the general purpose PLL configuration. All dividers have a range of 1 to 2049. In normal mode, as shown in Figure 8, the PLL performs classical "M over N" frequency synthesis application. When the output frequency is an integer multiple or division of the input frequency precise phase control allows fine adjustment of the phase relationship of the output to the input. In this example, locations B and C are phase controlled with respect to A. The phase relationship of A and D is inferred.

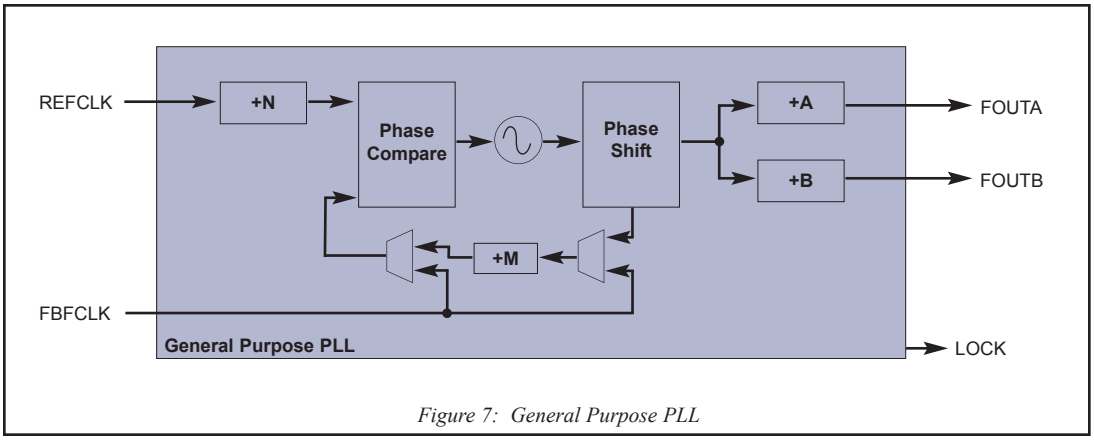

Figure 7: General Purpose PLL

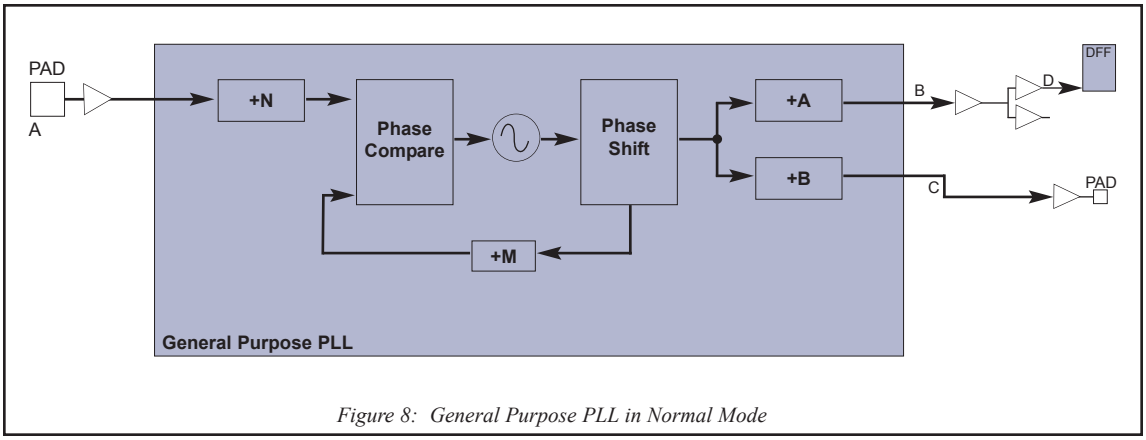

Figure 8: General Purpose PLL in Normal Mode

Figure 9 shows the general purpose PLL used in zero delay mode. This mode supports integer multiply or divide for both outputs. Locations A and B are phased matched.

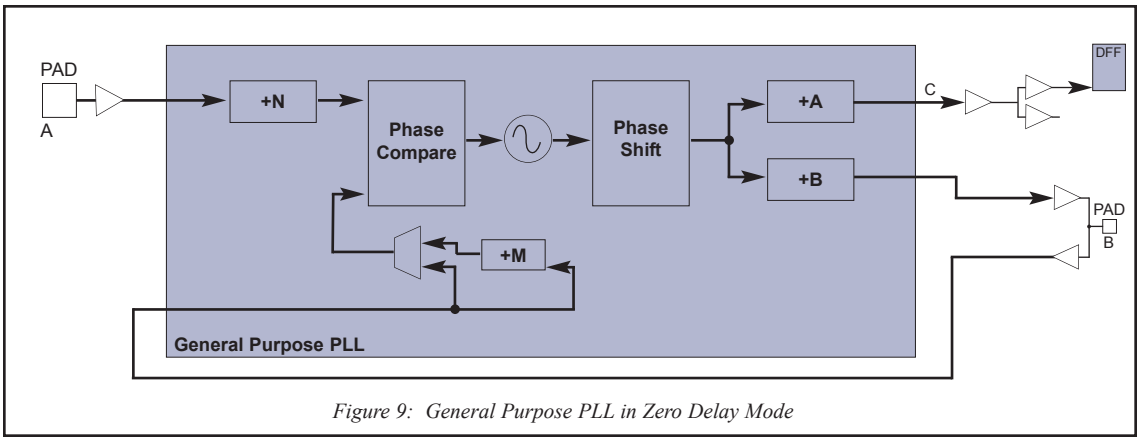

Figure 9: General Purpose PLL in Zero Delay Mode

Figure 10 shows the general purpose PLL used in external feedback mode. This mode supports integer multiply or divide for both outputs. Locations A and B are phase matched.

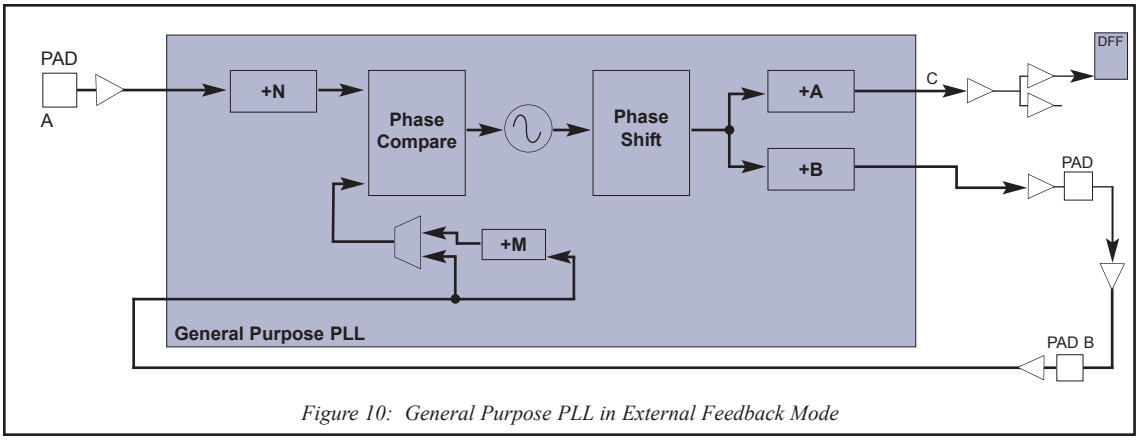

Figure 10: General Purpose PLL in External Feedback Mode

Figure 11 shows the general purpose PLL used in clock tree mode. This mode supports integer multiply or divide for both outputs. Locations A and B are phase matched, C is phase controlled with respect to D.

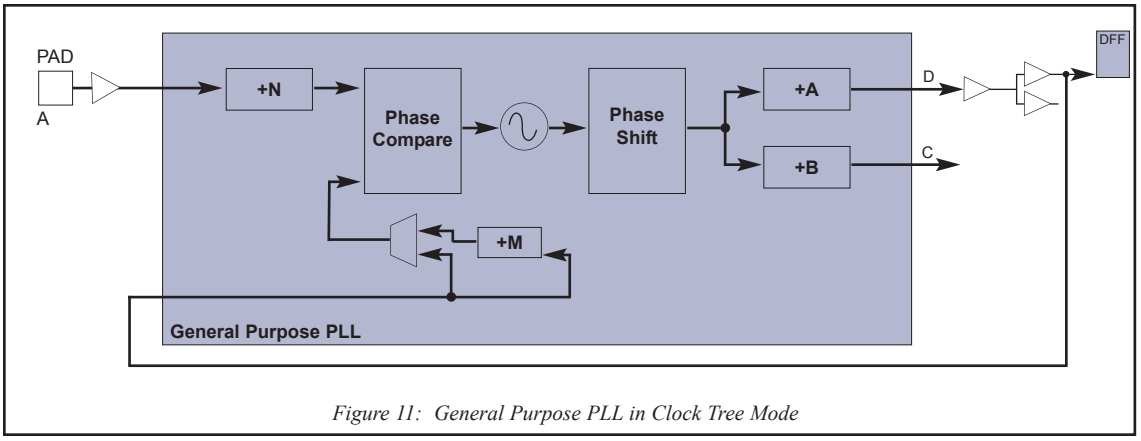

Figure 11: General Purpose PLL in Clock Tree Mode

Figure 12 shows the LVDS PLL configuration which supports high-speed serial I/O applications. The reference divider supports a range of 1 to 2049 while the feedback divider is limited to a range of 1 to 33. The PLL contains integral test hardware to facilitate silicon testing and in-circuit PLL tuning. The PLL requires a dedicated power and ground pad pair.

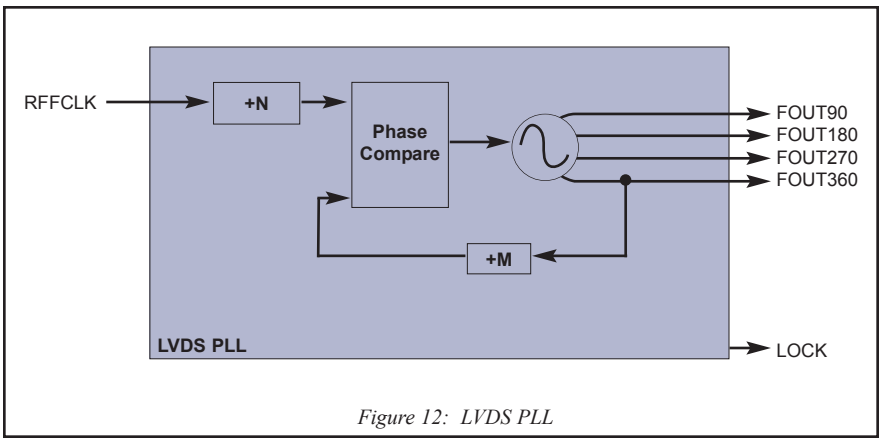

Figure 12: LVDS PLL

9.0 RTL Hand-Off Flow

XPressArray-II synthesis libraries are available for leading commercial synthesizers, including Synplicity® Synplify ASIC and Synopsys® Design Compiler.

With the RTL hand-off flow, you can submit your RTL description, scripts and timing constraints to AMIS. AMIS will check, synthesize, layout, and achieve timing closure on your design. Typically if Synplify Pro was used for the FPGA design, then Synplify ASIC will be used for the ASIC design. Likewise if FPGA DC was used, then Design Compiler is used for the ASIC re-synthesis.

10.0 NETRANS® Conversion Flow

XPressArray-II devices are fully supported by AMI Semiconductor's proven NETRANS flow. AMIS has over 19 years experience using NETRANS to convert over 1700 FPGA and third party ASIC designs to AMIS ASICs.

Inputs to the NETRANS flow include the netlist, test benches and timing constraints. Over 70 different device types and netlist formats are supported.
Mapping libraries are fully verified by a process which includes formal verification of each primitive function.

11.0 Electrical Specifications

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Internal Supply Voltage*	-0.4	1.7	V
V_{CCO}	I/O Supply Voltage			
	3.3V I/O	-0.4	3.7	V
	2.5V I/O	-0.4	2.8	V
	1.8V I/O	-0.4	2.0	V
	1.5V I/O	-0.4	1.7	V
V_{CCAUX}	I/O Auxiliary Supply Voltage			
	3.3V I/O	-0.4	3.7	V
	2.5V I/O	-0.4	2.5	V
V_{IN}, V_{OUT}	DC Input, Output	-0.4	V_{CCO}+0.4	V
T_J	Junction Temperature	-45	130	°C

* 1.2V characterization available upon request.

Table 7: Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Internal Supply Voltage*	1.425	1.575	V
V_{CCO}	I/O Supply Voltage			
	3.3V I/O	3.135	3.465	V
	2.5V I/O	2.375	2.625	V
	1.8V I/O	1.710	1.890	V
	1.5V I/O	1.425	1.575	V
V_{CCAUX}	I/O Auxiliary Supply Voltage			
	3.3V I/O	3.135	3.465	V
	2.5V I/O	2.375	2.625	V
V_{IN}, V_{OUT}	DC Input, Output	-0.3	V_{CCO}+0.3	V
T_J	Junction Temperature	-40	125	°C

* 1.2V characterization available upon request.

Table 8: DC Characteristics

Symbol	Parameter	Min.	Max.	Units
I_{DD}	Quiescent V_{DD} Supply Voltage		10	mA
I_L	Input or Output Leadage Current	-10	10	µA
C_{IN}	Input Pad Capacitance		4	pF
I_{RPU}	Pad Pull-up Current	-10	-250	µA
I_{RPD}	Pad Pull-down Current	10	250	µA

Table 9: DLL Specifications

Parameter	Value
Operating Modes	• Clock Tree • Zero Delay Buffer • External Feedback • Quadrature Shift • Basic Frequency Shift
Low/High Frequency Operation	Combined
Control Inputs	DCC (Duty Cycle Correction), TIMELOCK
Available Outputs	CLK90, CLK180, CLK270, CLK360, CLKDV, CLK2X, LOCK, VALIDCLK
Frequency Range	25-300MHz
Clock Doubler Frequency Range	50-500MHz
Clock Divider Range	1.6-16 in 0.5 steps, 16-32 in 1.0 steps
Duty Cycle Correction Resolution	45-55%
Fine Quadrature Phase Shift Range	+/- 64 taps (@ Typical 1 Tap = 70ps)
Clock Tree Delay Compensation	Yes
Output Clock Jitter CLKO (Peak-to-Peak)	+/- 175ps
Output Clock Jitter CLK90, CLK180, CLK270 (Peak-to-Peak)	+/- 250ps
Output Clock Jitter CLK2X (Peak-to-Peak)	+/- 325ps
Output Clock Jitter CLKDV (Integer Division, Peak-to-Peak)	+/- 250ps
Output Clock Jitter CLKDV (Non-integer Division, Peak-to-Peak)	+/- 400ps
Output Clock Phase Offset (Between all Quadratures)	+/- 250ps
Lock Time	180us @ 20MHz 40us @ >60MHz

Table 10: PLL Specifications

Parameter	General Purpose Mode	LVDS Mode
Operating Modes	• Normal with Phase Shift • Zero Delay Buffer • External Feedback • Clock Tree	• LVDS
Input Frequency Range	1.5-620MHz	1.5-620MHz
Input Duty Cycle	40-60%	40-60%
Input Jitter (Peak-to-Peak)	2% of input period	2% of input period
PFD Frequency Range	1-50MHz	1-50MHz
VCO Frequency Range	200-500MHz	200-1000MHz
Output Frequency Range	1-500MHz	1-800MHz
Output Duty Cycle	45-55%	45-55%
Output Period Jitter (Peak-to-Peak)	200ps	175ps
Reference Divider	1-2049	1-2049
Feedback Divider	1-2049	1-33
Post Dividers	1-2049	N/A
Phase Shift Resolution	$1/[F_{vco}*5]$	$1/[F_{vco}*5]$
Phase Shift Range	0-360°	0-360°
Available Outputs	FOUTA, FOUTB	FOUT90, FOUT180, FOUT270, FOUT360

Electrical specifications subject to change without notice.

12.0 FPGA Cross Reference

Table 11: Altera Stratix Cross Reference

FPGA Part	Package	Utilization I/O Base	100% Logic Base	50% RAM Base	100% RAM Base
EP1S10	F484	X2P376	X2P376	X2P528	X2P680
EP1S10	B672	X2P528	X2P376	X2P528	X2P680
EP1S10	F672	X2P528	X2P376	X2P528	X2P680
EP1S10	F780	X2P528	X2P376	X2P528	X2P680
EP1S20	F484	X2P376	X2P376	X2P680	X2P846
EP1S20	B672	X2P528	X2P376	X2P680	X2P846
EP1S20	F672	X2P528	X2P376	X2P680	X2P846
EP1S20	F780	X2P680	X2P376	X2P680	X2P846
EP1S25	B672	X2P528	X2P376	X2P680	X2P846
EP1S25	F672	X2P528	X2P376	X2P680	X2P846
EP1S25	F780	X2P680	X2P376	X2P680	X2P846
EP1S25	F1020	X2P846	X2P376	X2P680	X2P846
EP1S30	F780	X2P680	X2P376	X2P846	X2P1148
EP1S30	B956	X2P846	X2P376	X2P846	X2P1148
EP1S30	F1020	X2P846	X2P376	X2P846	X2P1148
EP1S40	F780	X2P680	X2P528	X2P846	X2P1148
EP1S40	B956	X2P846	X2P528	X2P846	X2P1148
EP1S40	F1020	X2P846	X2P528	X2P846	X2P1148
EP1S40	F1508	X2P998	X2P528	X2P846	X2P1148
EP1S60	B956	X2P846	X2P528	X2P998	X2P1346
EP1S60	F1020	X2P846	X2P528	X2P998	X2P1346
EP1S60	F1508	X2P1148	X2P528	X2P998	X2P1346
EP1S80	B956	X2P846	X2P680	X2P1346	NONE
EP1S80	F1020	X2P998	X2P680	X2P1346	NONE
EP1S80	F1508	X2P1346	X2P680	X2P1346	NONE

Table 12: Altera APEX-II Cross Reference

FPGA Part	Package	Utilization I/O Base	100% Logic Base	50% RAM Base	100% RAM Base
EP2A15	F672	X2P528	X2P376	X2P376	X2P376
EP2A15	B724	X2P528	X2P376	X2P376	X2P376
EP2A25	F672	X2P528	X2P376	X2P376	X2P376
EP2A25	B724	X2P680	X2P376	X2P376	X2P376
EP2A40	F672	X2P528	X2P376	X2P376	X2P376
EP2A40	B724	X2P680	X2P376	X2P376	X2P376
EP2A40	F1020	X2P846	X2P376	X2P376	X2P376
EP2A70	B724	X2P680	X2P680	X2P376	X2P376
EP2A70	F1508	X2P1148	X2P680	X2P376	X2P376

Table 13: Altera Cyclone-II Cross Reference

FPGA Part	Package	Utilization I/O Base	100% Logic Base	50% RAM Base	100% RAM Base
EP2C8	F256	X2P376	X2P376	X2P376	X2P376
EP2C20	F256	X2P376	X2P376	X2P376	X2P376
EP2C20	F484	X2P376	X2P376	X2P376	X2P376
EP2C35	F484	X2P376	X2P376	X2P376	X2P528
EP2C35	F672	X2P528	X2P376	X2P376	X2P528
EP2C50	F672	X2P376	X2P680	X2P376	X2P680
EP2C50	F896	X2P528	X2P680	X2P376	X2P680
EP2C70	F672	X2P528	X2P680	X2P528	X2P846
EP2C70	F896	X2P680	X2P680	X2P528	X2P846

Table 14: Xilinx Virtex-II Cross Reference

Utilization			100% Logic Base	50% RAM Base	100% RAM Base
FPGA Part	Package	I/O Base			
XC2V40	FG256	X2P376	X2P376	X2P376	X2P376
XC2V80	FG256	X2P376	X2P376	X2P376	X2P376
XC2V250	FG256	X2P376	X2P376	X2P376	X2P528
XC2V250	FG456	X2P376	X2P376	X2P376	X2P528
XC2V500	FG256	X2P376	X2P376	X2P376	X2P528
XC2V500	FG456	X2P376	X2P376	X2P376	X2P528
XC2V1000	FG256	X2P376	X2P376	X2P528	X2P528
XC2V1000	FG456	X2P376	X2P376	X2P528	X2P528
XC2V1000	BG575	X2P376	X2P376	X2P528	X2P528
XC2V1000	FF896	X2P528	X2P376	X2P528	X2P528
XC2V1500	BG575	X2P528	X2P376	X2P528	X2P680
XC2V1500	FG676	X2P528	X2P376	X2P528	X2P680
XC2V1500	FF896	X2P680	X2P376	X2P528	X2P680
XC2V2000	BG575	X2P528	X2P376	X2P528	X2P680
XC2V2000	FG676	X2P528	X2P376	X2P528	X2P680
XC2V2000	FF896	X2P680	X2P376	X2P528	X2P680
XC2V2000	BF957	X2P680	X2P376	X2P528	X2P680
XC2V3000	FG676	X2P528	X2P376	X2P680	X2P846
XC2V3000	BG728	X2P680	X2P376	X2P680	X2P846
XC2V3000	BF957	X2P846	X2P376	X2P680	X2P846
XC2V3000	FF1152	X2P846	X2P376	X2P680	X2P846
XC2V4000	BF957	X2P846	X2P528	X2P846	X2P998
XC2V4000	FF1152	X2P846	X2P528	X2P846	X2P998
XC2V4000	FF1517	X2P998	X2P528	X2P846	X2P998
XC2V6000	BF957	X2P846	X2P680	X2P846	X2P998
XC2V6000	FF1152	X2P846	X2P680	X2P846	X2P998
XC2V6000	FF1517	X2P1148	X2P680	X2P846	X2P998
XC2V8000	FF1152	X2P846	X2P680	X2P846	X2P998
XC2V8000	FF1517	X2P1148	X2P680	X2P846	X2P998

Table 15: Xilinx Virtex-II Pro Cross Reference

Utilization			100% Logic Base	50% Logic Base	100% RAM Base
FPGA Part	Package	I/O Base			
XC2VP2	FG256	X2P376	X2P376	X2P376	X2P376
XC2VP2	FG456	X2P376	X2P376	X2P376	X2P376
XC2VP2	FF672	X2P376	X2P376	X2P376	X2P376
XC2VP4	FG256	X2P376	X2P376	X2P376	X2P528
XC2VP4	FG456	X2P376	X2P376	X2P376	X2P528
XC2VP4	FF672	X2P528	X2P376	X2P376	X2P528
XC2VP7	FG456	X2P376	X2P376	X2P528	X2P528
XC2VP7	FF672	X2P528	X2P376	X2P528	X2P528
XC2VP7	FF896	X2P528	X2P376	X2P528	X2P528
XC2VP20	FG676	X2P528	X2P376	X2P680	X2P846
XC2VP20	FF896	X2P680	X2P376	X2P680	X2P846
XC2VP20	FF1152	X2P680	X2P376	X2P680	X2P846
XC2VP30	FG676	X2P528	X2P528	X2P846	X2P998
XC2VP30	FF896	X2P680	X2P528	X2P846	X2P998
XC2VP30	FF1152	X2P680	X2P528	X2P846	X2P998
XC2VP40	FG676	X2P528	X2P680	X2P846	X2P1148
XC2VP40	FF1148	X2P846	X2P680	X2P846	X2P1148
XC2VP40	FF1152	X2P680	X2P680	X2P846	X2P1148
XC2VP50	FF1148	X2P846	X2P680	X2P998	X2P1346
XC2VP50	FF1152	X2P846	X2P680	X2P998	X2P1346
XC2VP50	FF1517	X2P998	X2P680	X2P998	X2P1346
XC2VP70	FF1517	X2P998	X2P680	X2P1148	None
XC2VP70	FF1704	X2P1148	X2P680	X2P1148	None
XC2VP100	FF1696	X2P1346	X2P846	X2P1346	None
XC2VP105	FF1704	X2P1148	X2P846	X2P1346	None
XC2VP125	FF1696	X2P1346	X2P998	None	None
XC2VP125	FF1704	X2P1148	X2P998	None	None

Table 16: Xilinx Spartan-3 Cross Reference

Utilization			100% Logic Base	50% RAM Base	100% RAM Base
FPGA Part	Package	I/O Base			
XC3S200	FT256	X2P376	X2P376	X2P376	X2P376
XC3S400	FT256	X2P376	X2P376	X2P376	X2P376
XC3S400	FG456	X2P376	X2P376	X2P376	X2P376
XC3S1000	FT256	X2P376	X2P376	X2P376	X2P528
XC3S1000	FG456	X2P376	X2P376	X2P376	X2P528
XC3S1000	FG676	X2P528	X2P376	X2P376	X2P528
XC3S1500	FG456	X2P376	X2P376	X2P376	X2P528
XC3S1500	FG676	X2P528	X2P376	X2P376	X2P528
XC3S2000	FG900	X2P680	X2P376	X2P528	X2P680
XC3S2000	FG676	X2P528	X2P376	X2P528	X2P680
XC3S4000	FG900	X2P680	X2P528	X2P680	X2P846
XC3S4000	FG1156	X2P846	X2P528	X2P680	X2P846
XC3S5000	FG900	X2P680	X2P680	X2P680	X2P846
XC3S5000	FG1156	X2P846	X2P680	X2P680	X2P846