

**AO4932**
**Asymmetric Dual N-Channel Enhancement Mode Field Effect Transistor**
**SRFET™**
**General Description**

The AO4932 uses advanced trench technology to provide excellent  $R_{DS(ON)}$  and low gate charge. The two MOSFETs make a compact and efficient switch and synchronous rectifier combination for use in DC-DC converters. A monolithically integrated Schottky diode in parallel with the synchronous MOSFET to boost efficiency further. Standard Product AO4932 is Pb-free (meets ROHS & Sony 259 specifications).

**Features**
**FET1**

$V_{DS}$  (V) = 30V  
 $I_D$  = 9A  
 $R_{DS(ON)}$  < 15.8m $\Omega$   
 $R_{DS(ON)}$  < 19.6m $\Omega$

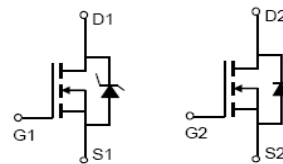
**FET2**

$V_{DS}$ (V) = 30V  
 $I_D$ =9A ( $V_{GS}$  = 10V)  
 <15.8m $\Omega$  ( $V_{GS}$  = 10V)  
 <23m $\Omega$  ( $V_{GS}$  = 4.5V)

**UIS TESTED!**  
*R<sub>g</sub>, C<sub>iss</sub>, C<sub>oss</sub>, C<sub>rss</sub> Tested*



**SRFET™**  
 Soft Recovery MOSFET:  
 Integrated Schottky Diode


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	Max FET1	Max FET2	Units
Drain-Source Voltage	$V_{DS}$	30	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 20$	V
Continuous Drain Current <sup>AF</sup>	$I_{DSM}$	$T_A=25^\circ\text{C}$	9.0	A
		$T_A=70^\circ\text{C}$	7.2	
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	40	40	A
Avalanche Current <sup>C</sup>	$I_{AR}$	16	16	A
Repetitive avalanche energy $L=0.3\text{mH}$ <sup>C</sup>	$E_{AR}$	38	38	mJ
Power Dissipation	$P_{DSM}$	$T_A=25^\circ\text{C}$	2.0	W
		$T_A=70^\circ\text{C}$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	-55 to 150	$^\circ\text{C}$

**Thermal Characteristics FET1**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JL}$	32	40	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead <sup>C</sup>				

**Thermal Characteristics FET2**

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	48	62.5	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JL}$	32	40	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead <sup>C</sup>				

FET1 Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=1\text{mA}, V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $T_J=125^\circ\text{C}$		0.01 5	0.1 10	mA
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 12\text{V}$			0.1	$\mu\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.5	1.8	2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=4.5\text{V}, V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=9\text{A}$ $T_J=125^\circ\text{C}$		13 20.2	15.8 25.2	m $\Omega$
		$V_{GS}=4.5\text{V}, I_D=7\text{A}$		16	19.6	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}, I_D=9\text{A}$		64		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$		0.4	0.6	V
$I_S$	Maximum Body-Diode + Schottky Continuous Current				4.5	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		1450	1885	pF
$C_{oss}$	Output Capacitance			224		pF
$C_{rss}$	Reverse Transfer Capacitance			92		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		1.6	3.0	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, I_D=9\text{A}$		24	31	
$Q_g(4.5\text{V})$	Total Gate Charge			12.0	16	nC
$Q_{gs}$	Gate Source Charge			3.9		nC
$Q_{gd}$	Gate Drain Charge			4.2		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}, V_{DS}=15\text{V}, R_L=1.7\Omega,$ $R_{GEN}=3\Omega$		5.5		ns
$t_r$	Turn-On Rise Time			4.7		ns
$t_{D(off)}$	Turn-Off Delay Time			24.0		ns
$t_f$	Turn-Off Fall Time			4.0		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=9\text{A}, dI/dt=300\text{A}/\mu\text{s}$		10	12	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=9\text{A}, dI/dt=300\text{A}/\mu\text{s}$		6.8		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

F: The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.

Rev 2: June 2007

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FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

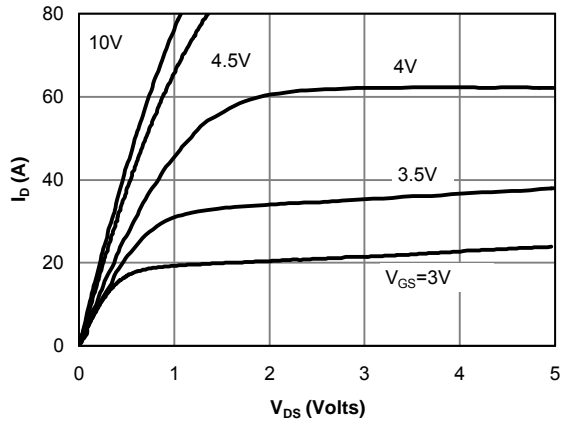


Figure 1: On-Region Characteristics

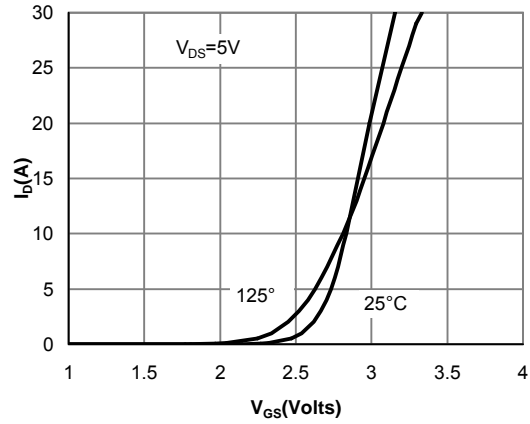


Figure 2: Transfer Characteristics

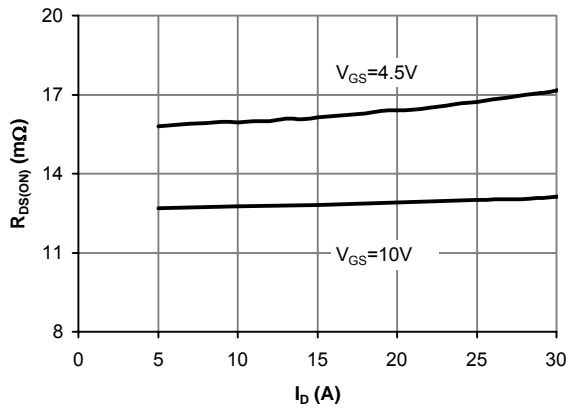


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

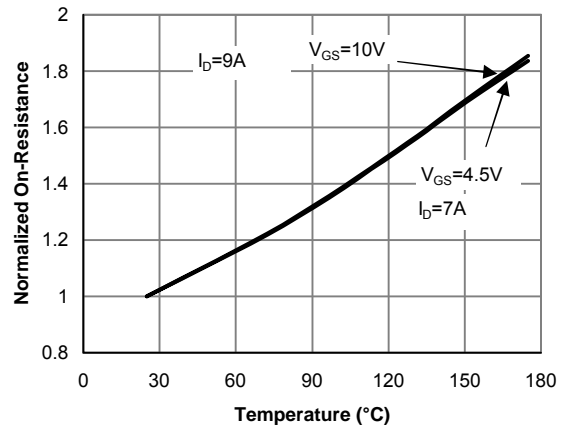


Figure 4: On-Resistance vs. Junction Temperature

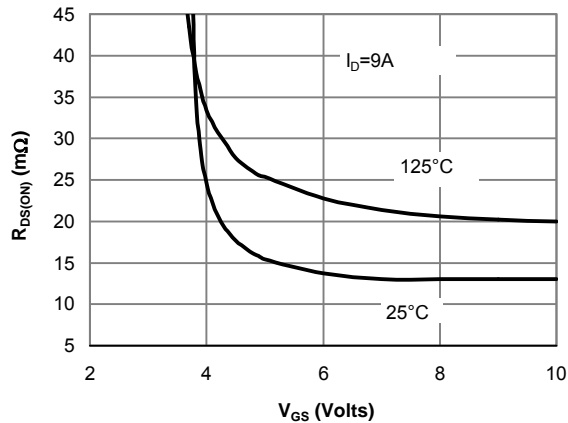


Figure 5: On-Resistance vs. Gate-Source Voltage

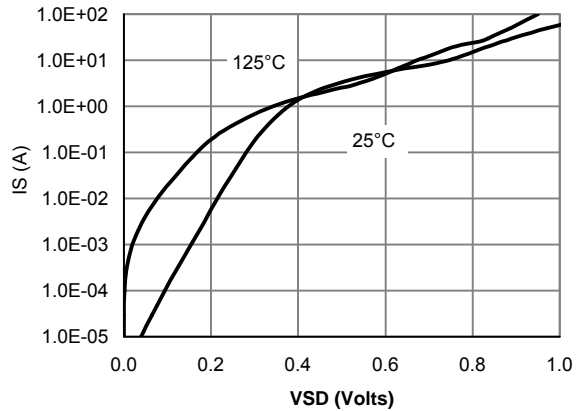


Figure 6: Body-Diode Characteristics

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

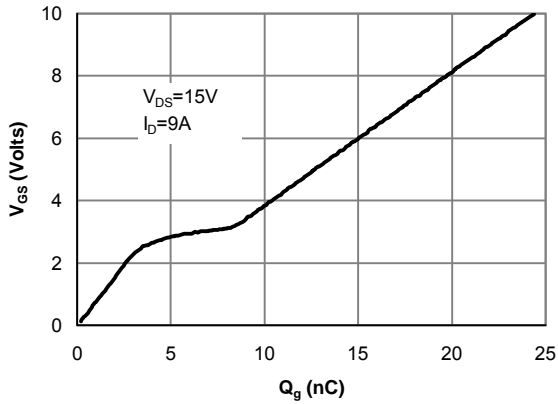


Figure 7: Gate-Charge Characteristics

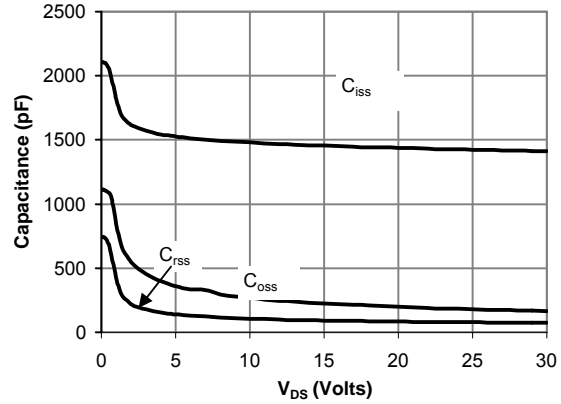


Figure 8: Capacitance Characteristics

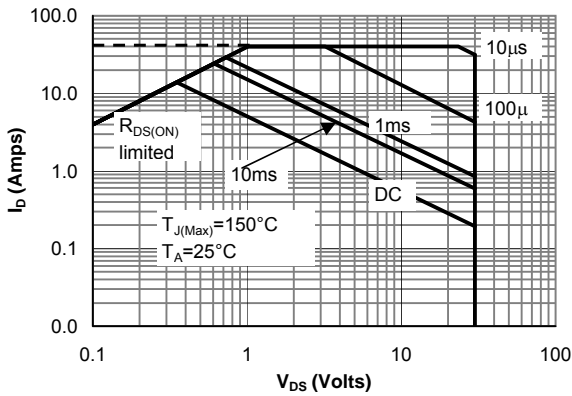


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

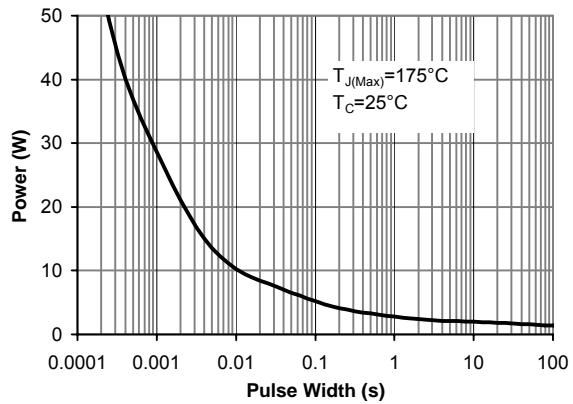


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

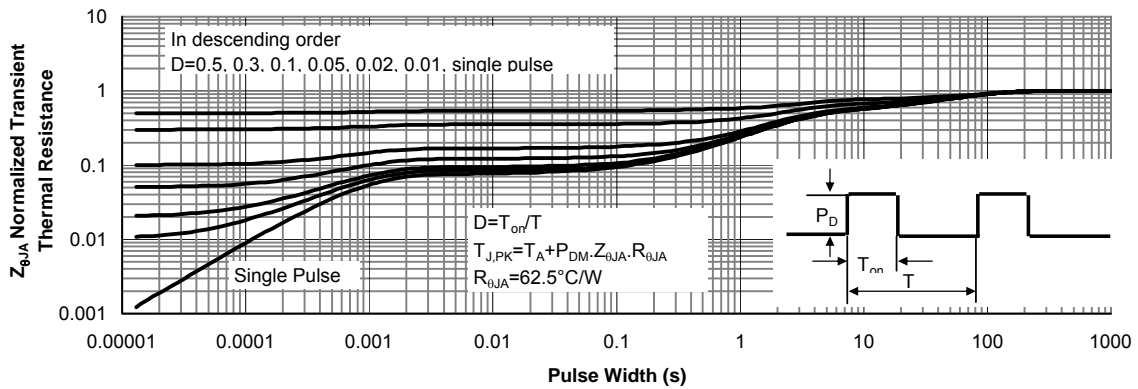


Figure 11: Normalized Maximum Transient Thermal Impedance (Note E)

FET1 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

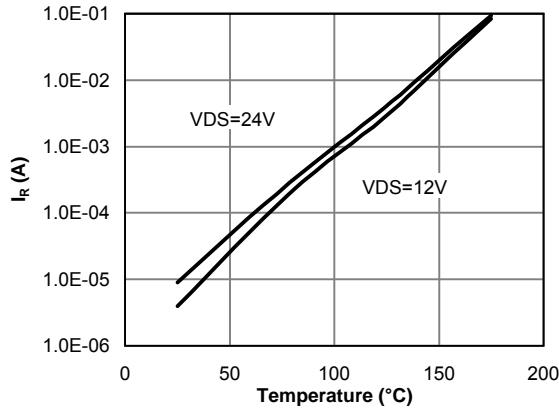


Figure 12: Diode Reverse Leakage Current vs. Junction Temperature

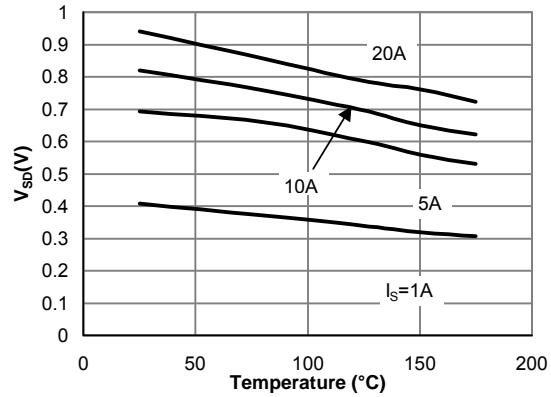


Figure 13: Diode Forward voltage vs. Junction Temperature

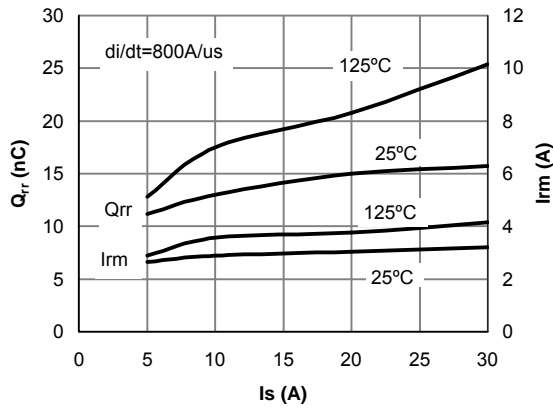


Figure 14: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

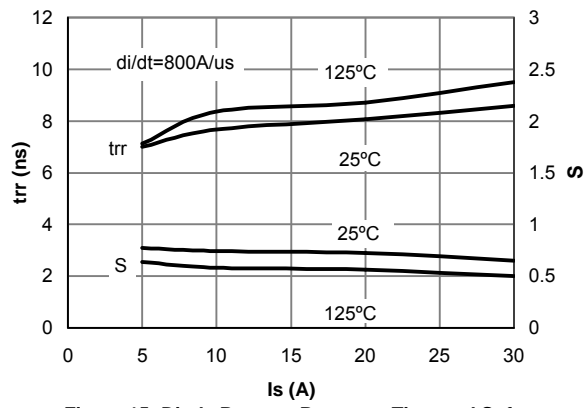


Figure 15: Diode Reverse Recovery Time and Soft Coefficient vs. Conduction Current

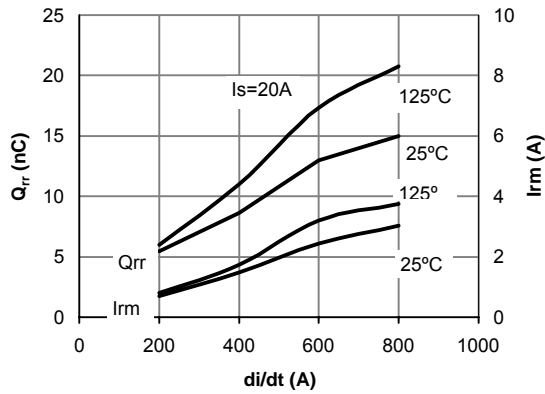


Figure 16: Diode Reverse Recovery Charge and Peak Current vs. di/dt

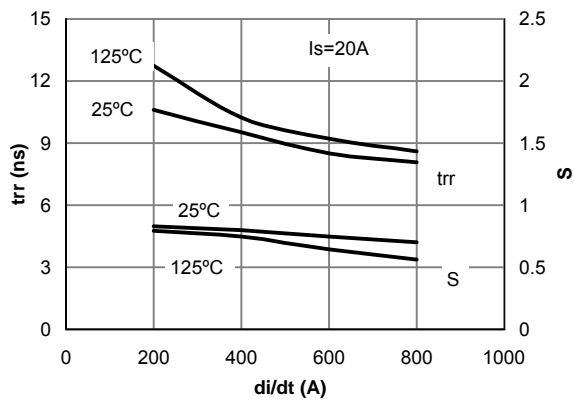


Figure 17: Diode Reverse Recovery Time and Soft Coefficient vs. di/dt

FET2 Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$ , $V_{GS}=0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1.3	1.7	2.3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=9\text{A}$ $T_J=125^\circ\text{C}$		13 19	15.8 23	m $\Omega$
		$V_{GS}=4.5\text{V}$ , $I_D=7\text{A}$		18.6	23	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=9\text{A}$		23		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.75	1	V
$I_S$	Maximum Body-Diode Continuous Current				3	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=15\text{V}$ , $f=1\text{MHz}$		955	1250	pF
$C_{oss}$	Output Capacitance			145		pF
$C_{riss}$	Reverse Transfer Capacitance			112		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		0.5	0.85	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $I_D=9\text{A}$		17	22	nC
$Q_g(4.5\text{V})$	Total Gate Charge			9	11.7	nC
$Q_{gs}$	Gate Source Charge			3.4		nC
$Q_{gd}$	Gate Drain Charge			4.7		nC
$t_{D(on)}$	Turn-On Delay Time			5		ns
$t_r$	Turn-On Rise Time	$V_{GS}=10\text{V}$ , $V_{DS}=15\text{V}$ , $R_L=1.7\Omega$ , $R_{GEN}=3\Omega$		6		ns
$t_{D(off)}$	Turn-Off Delay Time			19		ns
$t_f$	Turn-Off Fall Time			4.5		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=9\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		16.7	20	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=9\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		6.7		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C. The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to lead  $R_{\theta JL}$  and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

F. The current rating is based on the  $t_s \leq 10\text{s}$  thermal resistance rating.

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FET2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

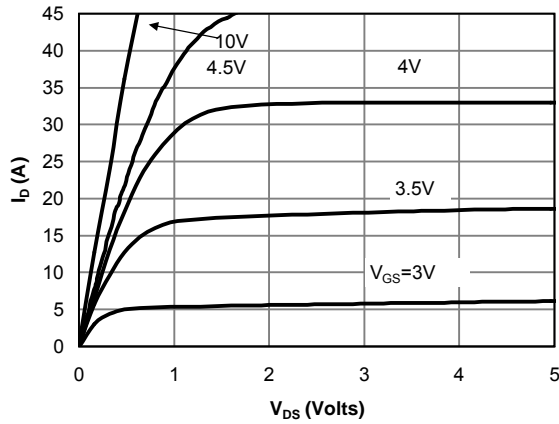


Figure 1: On-Region Characteristics

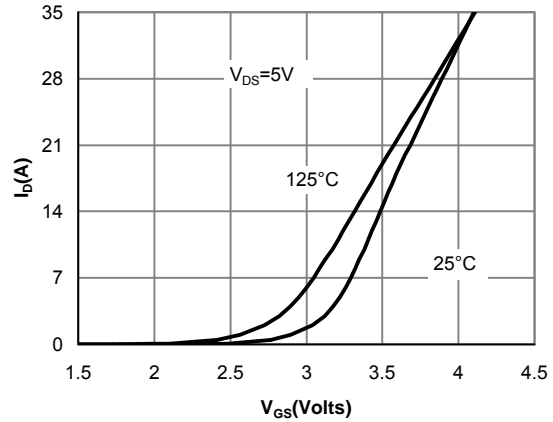


Figure 2: Transfer Characteristics

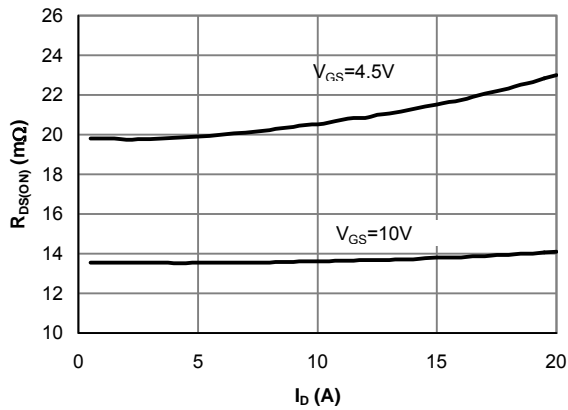


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

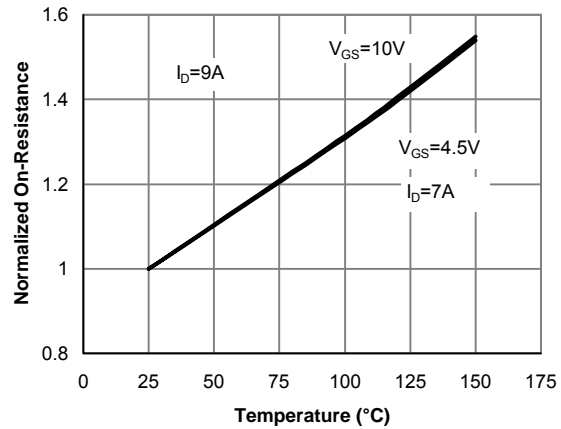


Figure 4: On-Resistance vs. Junction Temperature

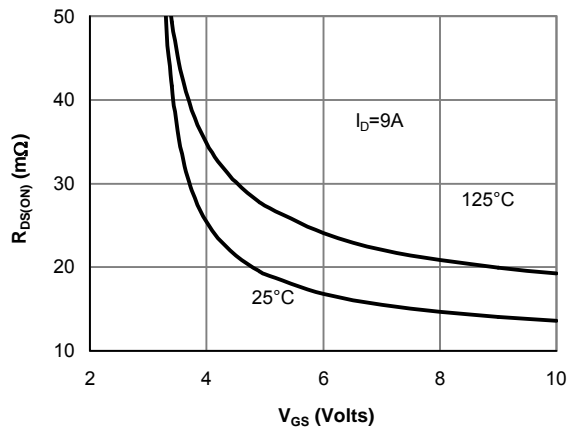


Figure 5: On-Resistance vs. Gate-Source Voltage

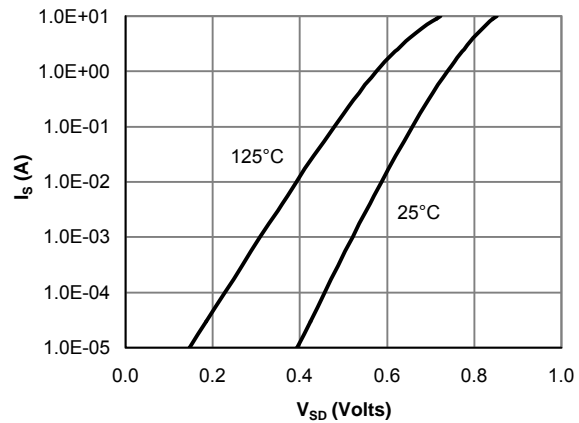


Figure 6: Body-Diode Characteristics

FET2 TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

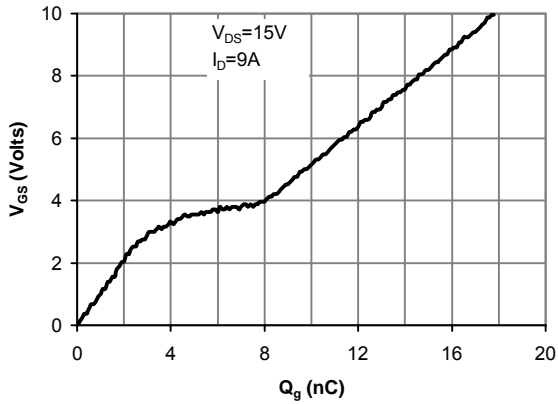


Figure 7: Gate-Charge Characteristics

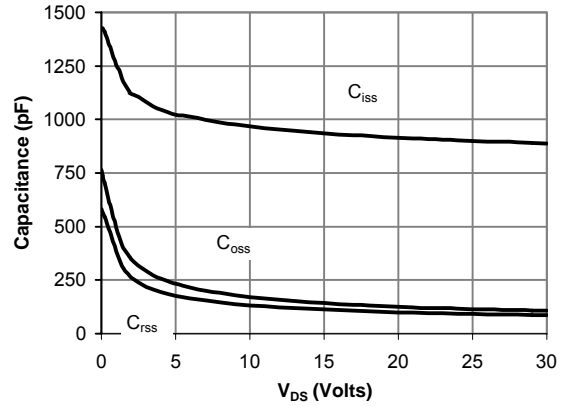


Figure 8: Capacitance Characteristics

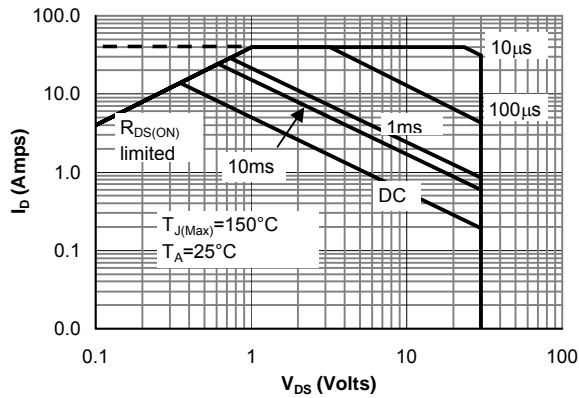


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

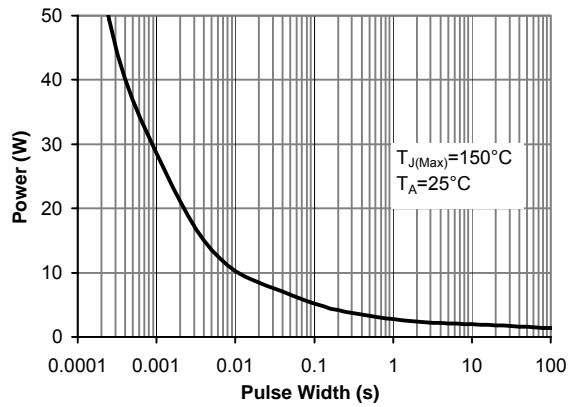


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

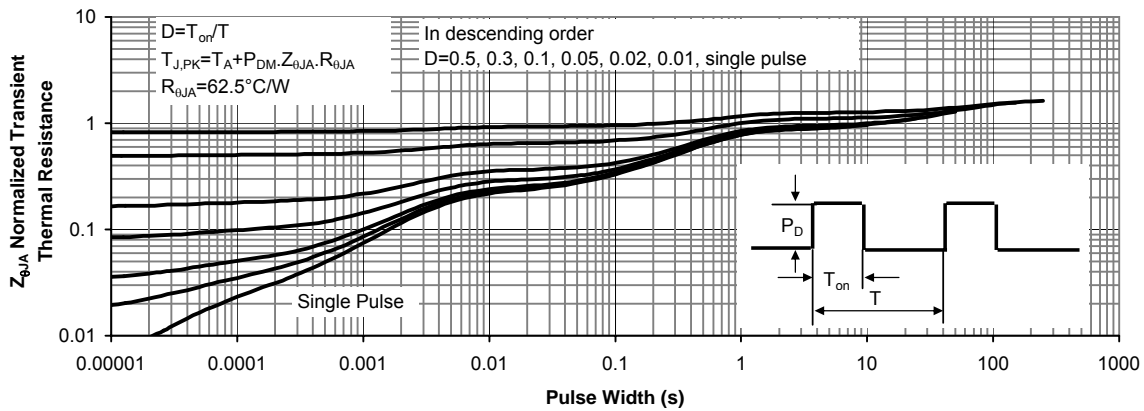


Figure 11: Normalized Maximum Transient Thermal Impedance