FAIRCHILD SEMICONDUCTOR®

October 2007

FSFR-Series / FSFR2100
Fairchild Power Switch (FPS™) for Half-Bridge Resonant Converter

Features

- Variable Frequency Control with 50% Duty Cycle for Half-bridge Resonant Converter Topology
- High Efficiency through Zero Voltage Switching (ZVS)
- Internal Super-FETs with Fast-Recovery Type Body Diode (t_{rr}=120ns)
- Fixed Dead Time (350ns) Optimized for MOSFETs
- Up to 300kHz Operating Frequency
- Pulse Skipping for Frequency Limit (Programmable) at Light-Load Condition
- Remote On/Off Control Using Control Pin
- Protection Functions: Over-Voltage Protection (OVP), Overload Protection (OLP), Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD)

Applications

- PDP TV and LCD TV
- Desktop PC and Server
- Adapter
- Telecom Power
- Audio Power

Description

FSFR-series is a highly integrated power switch family specially designed for high-efficiency half-bridge resonant converters. Offering everything necessary to build a reliable and robust resonant converter, the FSFR-series simplifies designs and improves productivity, while improving performance. The FSFR-series combines power MOSFETs with fast-recovery type body diodes, a high-side gate-drive circuit, an accurate current controlled oscillator, frequency limit circuit, soft-start, and built-in protection functions. The high-side drive circuit has a common-mode noise cancellation capability, which guarantees stable operation with excellent noise immunity. The fast-recovery body diode of the MOSFETs improves reliability against abnormal operation conditions, while minimizing the effect of the reverse recovery. Using the zero-voltage-switching (ZVS) technique dramatically reduces the switching losses and the efficiency is significantly improved. The ZVS also reduces the switching noise noticeably, which allows a small-sized EMI filter.

The FSFR-series can be applied to various resonant converter topologies such as series resonant, parallel resonant, and LLC resonant converters.

Related Resources

AN4151 — Half-bridge LLC Resonant Converter Design using FSFR-series Fairchild Power Switch (FPS™)

Ordering Information

Part Number	Package	Operating Temperature	$R_{DS(ON\_MAX)}$	Maximum Output Power without Heatsink (V_{IN}=350~400V) (1,2)	Maximum Output Power with Heatsink (V_{IN}=350~400V)(1,2)
FSFR2100	9-SIP	-40 to +85°C	0.38Ω	200W	450W
FSFR2000(3)	9-SIP	-40 to +85°C	0.67Ω	160W	350W
FSFR1900(3)	9-SIP	-40 to +85°C	0.85Ω	140W	300W
FSFR1800(3)	9-SIP	-40 to +85 ºC	0.95Ω	120W	260W

Notes:
1. The junction temperature can limit the maximum output power.
2. Maximum practical continuous power in an open-frame design at 50°C ambient.
3. Preliminary part design. Contact a Fairchild representative for availability.

All packages are lead free per JEDEC: J-STD-020B standard.

Application Circuit Diagram

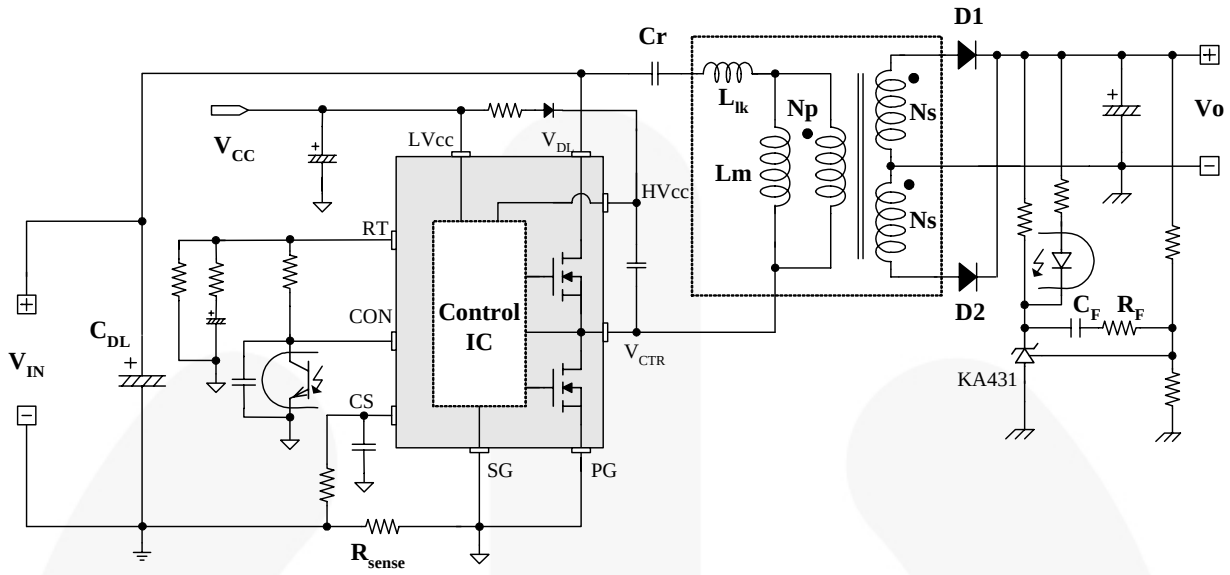


Figure 1. Typical Application Circuit (LLC Resonant Half-bridge Converter)

Block Diagram

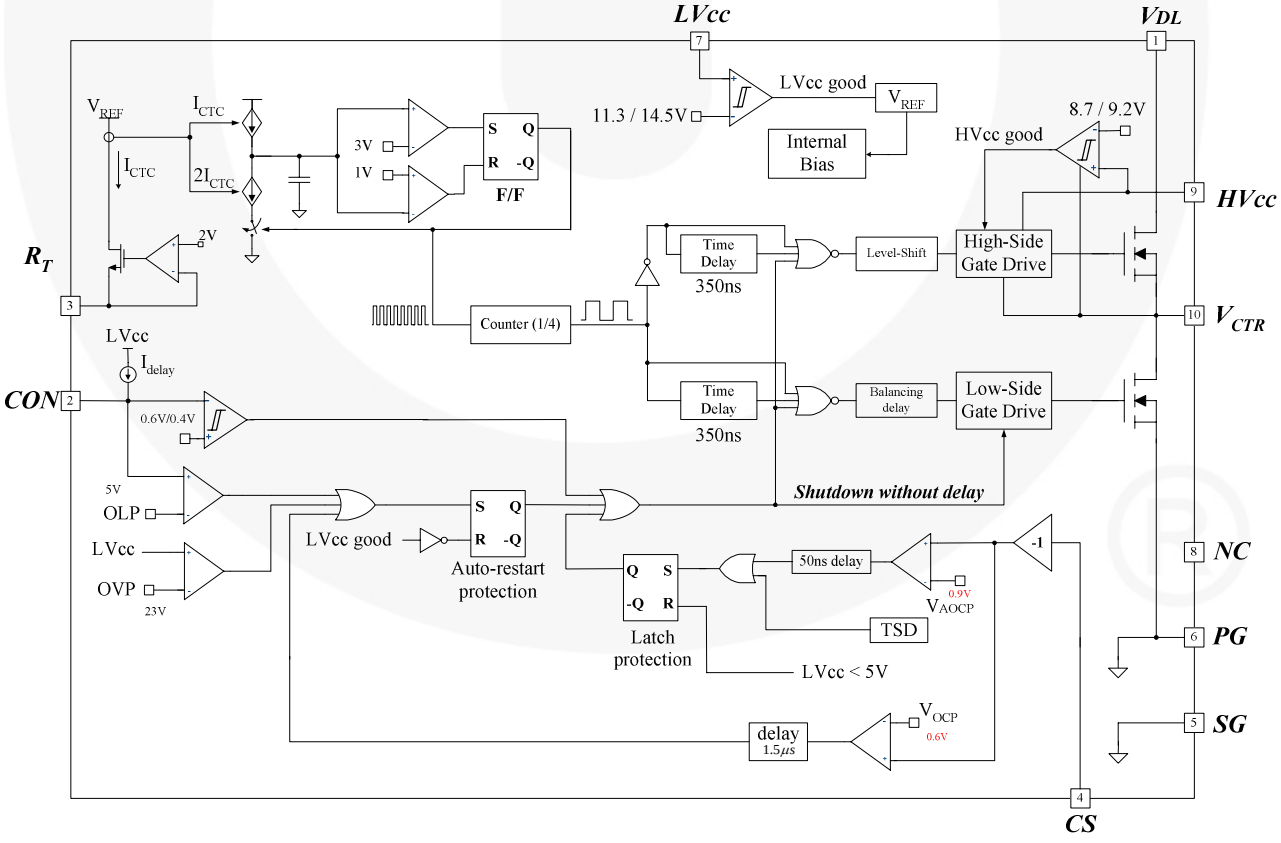


Figure 2. Internal Block Diagram

Pin Assignments

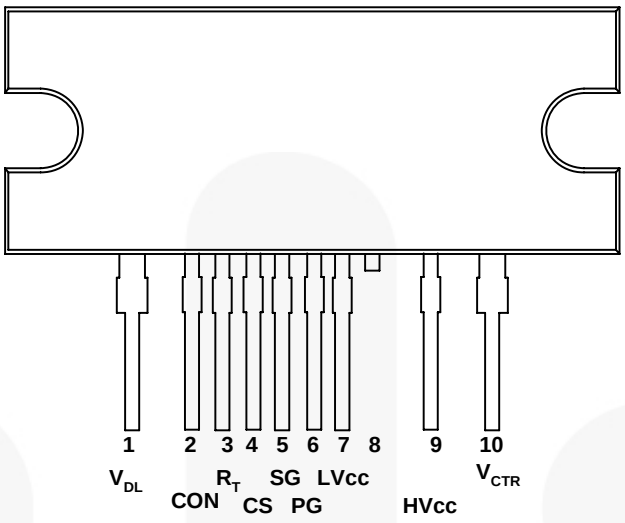


Figure 3. Package Diagram

Pin Definitions

Pin #	Name	Description
1	V_{DL}	This pin is the drain of the high-side MOSFET. It is typically connected to the input DC link voltage.
2	CON	This pin is for enable/disable and protection. When the voltage of this pin is above 0.6V, the IC operation is enabled. When the voltage of this pin drops below 0.4V, gate drive signals for both MOSFETs are disabled. When the voltage of this pin increases above 5V, protection is triggered.
3	R_T	This pin programs the switching frequency. Typically, an opto-coupler is connected to control the switching frequency for the output voltage regulation.
4	CS	This pin senses the current flowing through the low-side MOSFET. Typically, negative voltage is applied on this pin.
5	SG	This pin is the control ground.
6	PG	This pin is the power ground. This pin is connected to the source of the low-side MOSFET.
7	LVcc	This pin is the supply voltage of the control IC.
8	NC	No connection.
9	HVcc	This pin is the supply voltage of the high-side drive circuit IC.
10	V_{CTR}	This pin is the drain of the low-side MOSFET. Typically, a transformer is connected to this pin.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A=25°C unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{DS}	Maximum Drain-to-source Voltage (V_{DL}-V_{CTR} and V_{CTR}-PG)		600		V
LVcc	Low-side Supply Voltage		-0.3	25.0	V
HVcc to V_{CTR}	High-side V_{CC} Pin to Low-side Drain Voltage		-0.3	25.0	V
HVcc	High-side Floating Supply Voltage		-0.3	625.0	V
V_{CON}	Control Pin Input Voltage		-0.3	L-V_{CC}	V
V_{CS}	Current Sense (CS) Pin Input Voltage		-5.0	1.0	V
V_{RT}	R_T Pin Input Voltage		-0.3	5.0	V
dV_{CTR}/dt	Allowable Low-side MOSFET Drain Voltage Slew Rate			50	V/ns
P_D	Total Power Dissipation(4)			12	W
T_J	Operating Junction Temperature			+150	°C
T_A	Operating Ambient Temperature		-40	+85	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
MOSFET Section					
V_{DGR}	Drain Gate Voltage (R_{GS}=1MΩ)		600		V
V_{GS}	Gate Source (GND) Voltage			±30	V
I_{DM}	Drain Current Pulsed			33	A
I_D	Continuous Drain Current	T_C=25℃		11	A
		T_C=100℃		7	

Note:
4. Per MOSFET when both MOSFETs are conducting.

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ_{JC}	Junction-to-Case Center Thermal Impedance (Both MOSFETs Conducting)	10.44	ºC/W

Electrical Characteristics

T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Specifications			Unit
			Min.	Typ.	Max.	
MOSFET Section						
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D=200μA, T_A=25°C	600			V
		I_D=200μA, T_A=125°C		650		V
$R_{DS(ON)}$	On-State Resistance	V_{GS}=10, ID=5.5A		0.32	0.38	Ω
T_{rr}	Body Diode Reverse Recovery Time[5]			120		ns
Supply Section						
I_{LK}	Offset Supply Leakage Current	H-Vcc=VC=600V			50	μA
I_QHV_{CC}	Quiescent H-Vcc Supply Current	(H-VCCUV+) - 0.1V		50	120	μA
I_QLV_{CC}	Quiescent L-Vcc Supply Current	(L-VCCUV+) - 0.1V		100	200	μA
I_OHV_{CC}	Operating H-Vcc Supply Current (RMS Value)	F_{OSC}=100KHz, V_{CON} > 0.6V		6	9	mA
		No switching, V_{CON} < 0.4V		100	200	μA
I_OLV_{CC}	Operating L-Vcc Supply Current (RMS Value)	F_{OSC}=100KHz, V_{CON} > 0.6V		7	11	mA
		No switching, V_{CON} < 0.4V		2	4	mA
UVLO Section						
$LV_{CC}UV+$	L-Vcc Supply Under-voltage Positive Going Threshold (L-Vcc start)		13.0	14.5	16.0	V
$LV_{CC}UV-$	L-Vcc Supply Under-voltage Negative Going Threshold (L-Vcc stop)		10.2	11.3	12.4	V
$LV_{CC}UVH$	L-Vcc Supply Under-voltage Hysteresis			3.2		V
$HV_{CC}UV+$	H-Vcc Supply Under-voltage Positive Going Threshold (H-Vcc start)		8.2	9.2	10.2	V
$HV_{CC}UV-$	H-Vcc Supply Under-voltage Negative Going Threshold (H-Vcc stop)		7.8	8.7	9.6	V
$HV_{CC}UVH$	H-Vcc Supply Under-voltage Hysteresis			0.5		V
Oscillator & Feedback Section						
V_{CONDIS}	Control Pin Disable Threshold Voltage		0.36	0.40	0.44	V
V_{CONEN}	Control Pin Enable Threshold Voltage		0.54	0.60	0.66	V
V_{RT}	V-I Converter Threshold Voltage	R_T=5.2KΩ	1.5	2.0	2.5	V
F_{OSC}	Output Oscillation Frequency		94	100	106	KHz
DC	Output Duty Cycle		48	50	52	%
F_{SS}	Internal Soft-Start Initial Frequency	F_{SS}=F_{OSC}+40kHz, R_T=5.2KΩ		140		KHz
T_{SS2}	Internal Soft-Start Time		2	3	4	ms

Note:

5. This parameter, although guaranteed, is not tested.

Continued on the following page…

Electrical Characteristics (Continued)

T_A=25°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Specifications			Unit
			Min	Typ	Max	
Protection Section						
I_{OLP}	OLP Delay Current	V_{CON}=4V	3.6	4.8	6.0	μA
V_{OLP}	OLP Protection Voltage	V_{CON} > 3.5V	4.5	5.0	5.5	V
V_{OVP}	L-Vcc Over-Voltage Protection	L-Vcc > 21V	21	23	25	V
V_{AOCP}	AOCP Threshold Voltage	ΔV/Δt=-1V/μs	-1.0	-0.9	-0.8	V
T_{BAO}	AOCP Blanking Time[6]	V_{CS} < V_{OCP}; ΔV/Δt=-1V/us		50		ns
V_{OCP}	OCP Threshold Voltage	(V/(t=-1V/μs; V_{FB}=L_Vcc	-0.64	-0.58	-0.52	V
T_{BO}	OCP Blanking Time[6]	V_{CS} < V_{OCP}; ΔV/Δt=-1V/μs; V_{FB}=L_V_{CC}	1.0	1.5	2.0	μs
T_{DA}	Delay Time (Low Side) Detecting from V_{AOCP} to Switch Off[6]	ΔV/Δt=-1V/μs		250	400	ns
T_{SD}	Thermal Shutdown Temperature[6]		110	130	150	°C
I_{SU}	Protection Latch Sustain L-Vcc Supply Current	L-Vcc=7.5V		100	150	μA
V_{PRSET}	Protection Latch Reset L-Vcc Supply Voltage		5			V
Dead-Time Control Section						
D_T	Dead Time[7]			350		ns

Notes:
6. These parameters, although guaranteed, are not tested in production.
7. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

Typical Performance Characteristics

These characteristic graphs are normalized at T_A=25ºC.

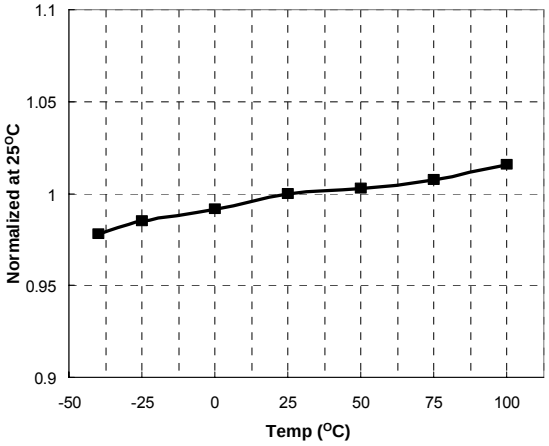


Figure 4. Low-side MOSFET Duty Cycle vs. Temp.

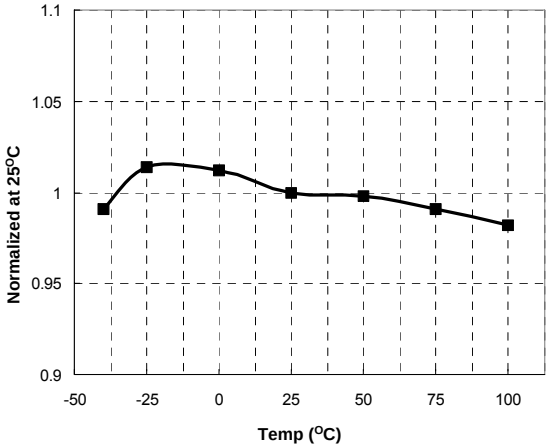


Figure 5. Switching Frequency vs. Temp.

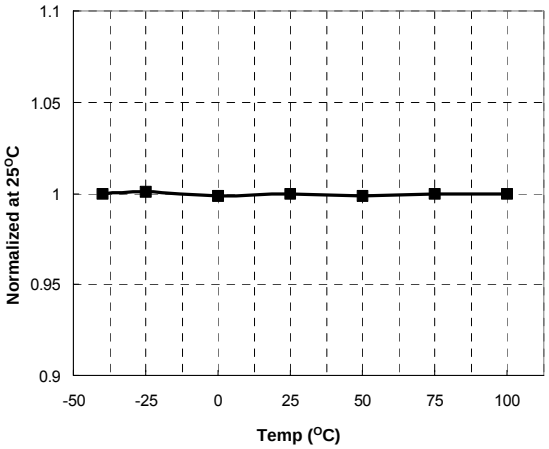


Figure 6. High-side V_{CC} (H-Vcc) Start vs. Temp.

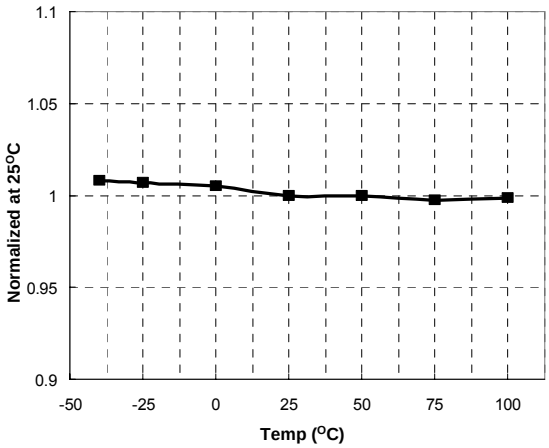


Figure 7. High-side V_{CC} (H-Vcc) Stop vs. Temp.

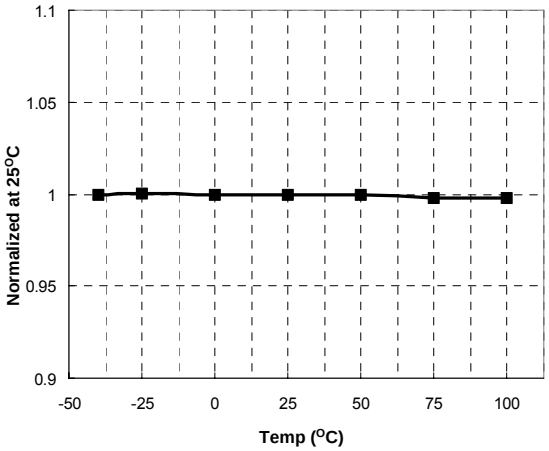


Figure 8. Low-side V_{CC} (L-Vcc) Start vs. Temp.

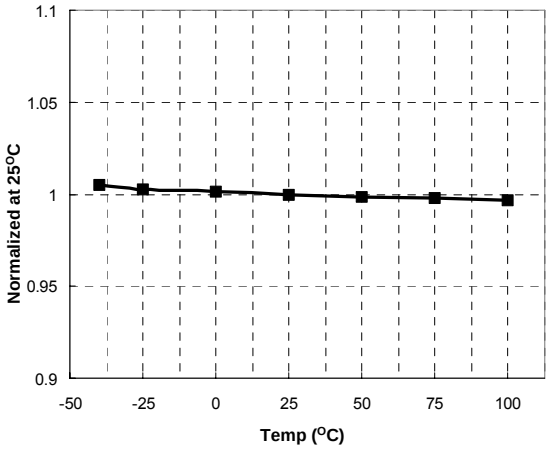


Figure 9. Low-side V_{CC} (L-Vcc) Stop vs. Temp.

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A=25ºC.

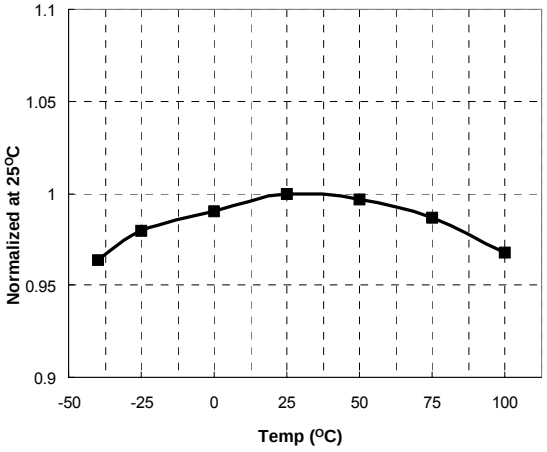


Figure 10. OLP Delay Current vs. Temp.

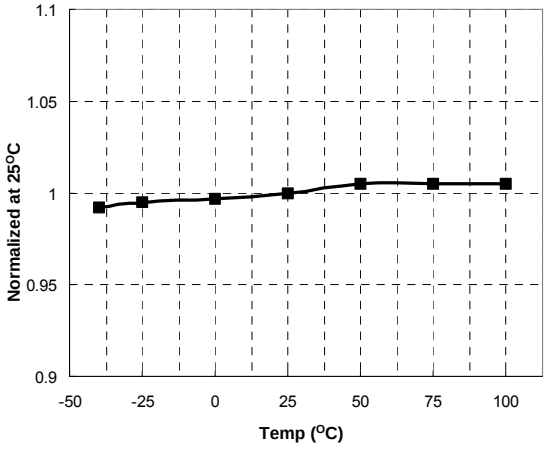


Figure 11. OLP Protection Voltage vs. Temp.

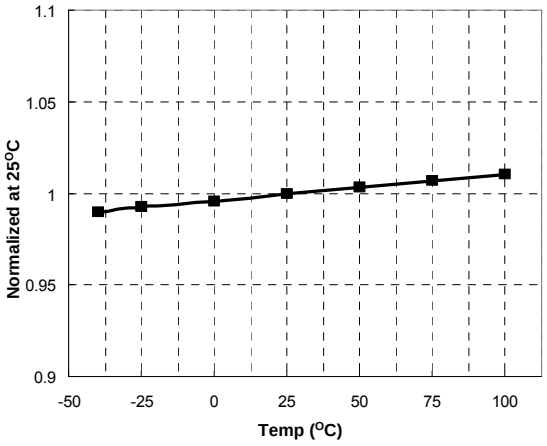


Figure 12. L-Vcc OVP Voltage vs. Temp.

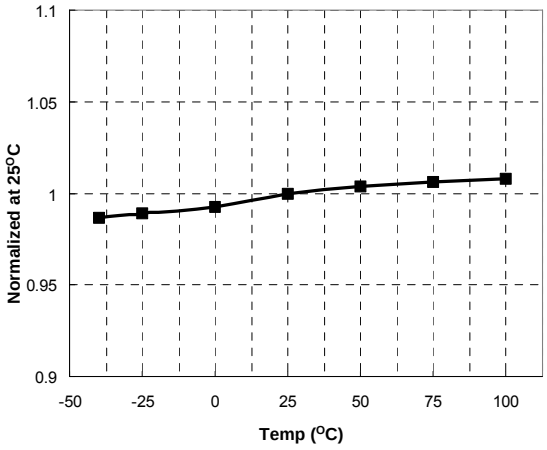


Figure 13. V-I Converter Voltage vs. Temp.

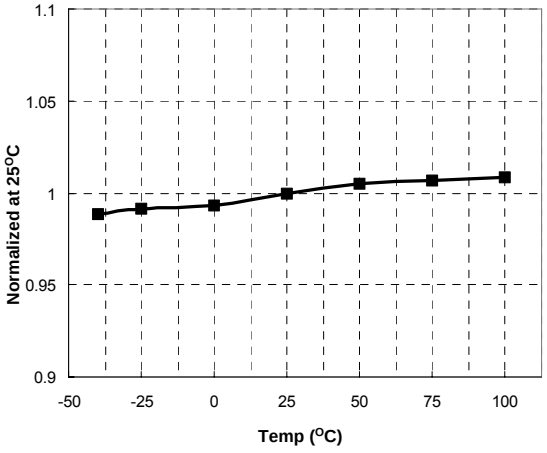


Figure 14. CON Pin Enable Voltage vs. Temp.

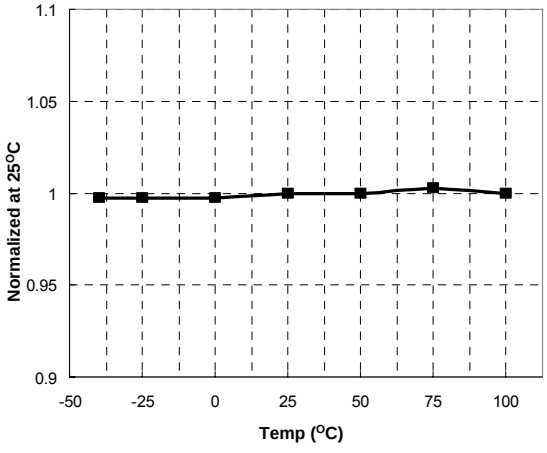


Figure 15. Current Limit vs. Temp.

Functional Description

1. Basic Operation: FSFR-series is designed to drive high-side and low-side MOSFETs complementarily with 50% duty cycle. A fixed dead time of 350ns is introduced between consecutive transitions, as shown in Figure 16.

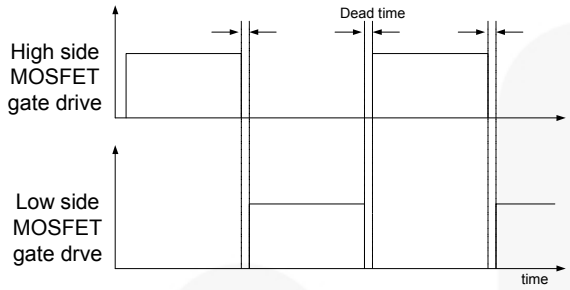


Figure 16. MOSFETs Gate Drive Signal

2. Internal Oscillator: FSFR-series employs a current-controlled oscillator, as shown in Figure 17. Internally, the voltage of R_T pin is regulated at 2V and the charging/discharging current for the oscillator capacitor, C_T, is obtained by copying the current flowing out of R_T pin (I_{CTC}) using a current mirror. Therefore, the switching frequency increases as I_{CTC} increases.

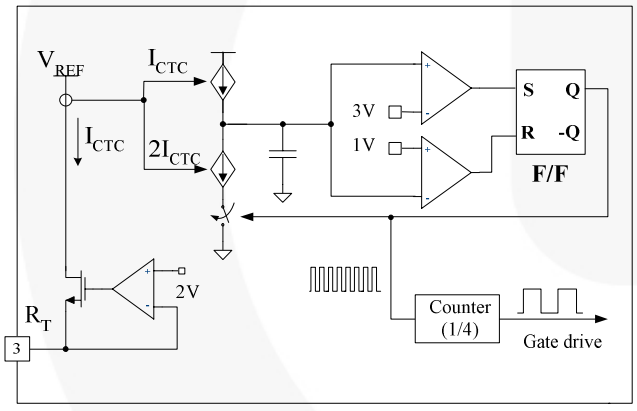


Figure 17. Current Controlled Oscillator

3. Frequency Setting: Figure 18 shows the typical voltage gain curve of a resonant converter, where the gain is inversely proportional to the switching frequency. The output voltage can be regulated by modulating the switching frequency. Figure 19 shows the typical circuit configuration for R_T pin, where the opto-coupler transistor is connected to the R_T pin to modulate the switching frequency.

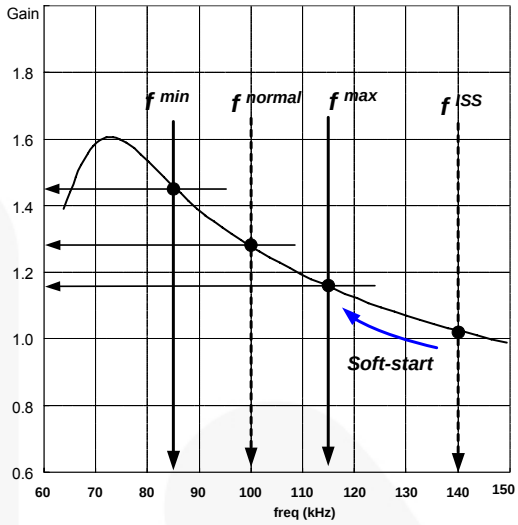


Figure 18. Resonant Converter Typical Gain Curve

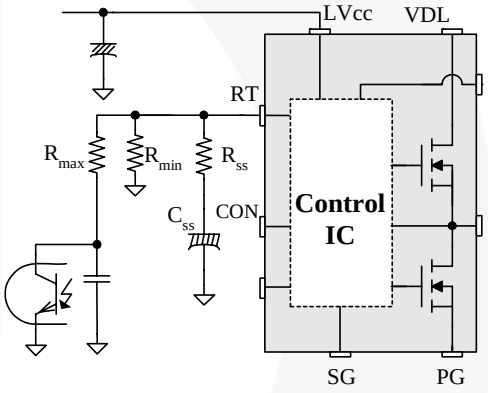


Figure 19. Frequency Control Circuit

The minimum switching frequency is determined as:

$$f^{\min} = \frac{5.2k\Omega}{R_{\min}} \times 100(kHz) \quad (1)$$

Assuming the saturation voltage of opto-coupler transistor is 0.2V, the maximum switching frequency is determined as:

$$f^{\max} = \left(\frac{5.2k\Omega}{R_{\min}} + \frac{4.68k\Omega}{R_{\max}}\right) \times 100(kHz) \quad (2)$$

To prevent excessive inrush current and overshoot of output voltage during start-up, increase the voltage gain of the resonant converter progressively. Since the voltage gain of the resonant converter is inversely proportional to the switching frequency, the soft-start is implemented by sweeping down the switching frequency from an initial high frequency (f^{ISS}) until the output voltage is established. The soft-start circuit is made by connecting R-C series network on the R_T pin, as shown in Figure 19. FSFR-series also has an internal soft-start for 3ms to reduce the current overshoot during the initial

cycles, which adds 40kHz to the initial frequency of the external soft-start circuit, as shown in Figure 20. Thus, the initial frequency of the soft-start is given as:

$$f^{ISS} = (\frac{5.2k\Omega}{R_{\min}} + \frac{5.2k\Omega}{R_{SS}}) \times 100 + 40\ (kHz) \quad (3)$$

It is typical to set the initial frequency of soft-start 2~3 times the resonant frequency (f_O) of the resonant network.

The soft-start time is determined by the RC time constant as:

$$T_{SS} = R_{SS} \cdot C_{SS} \quad (4)$$

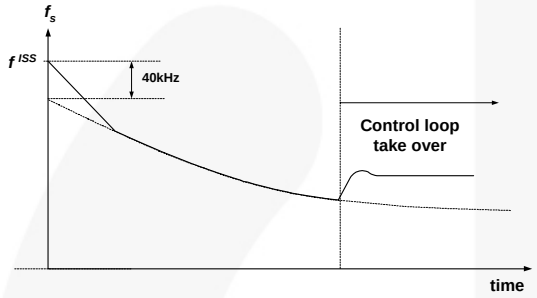


Figure 20. Frequency Sweeping of Soft-start

4. Control Pin: The FSFR-series has a control pin that can be used for protection, cycle skipping, and remote on/off. Figure 21 shows the internal block diagram for control pin.

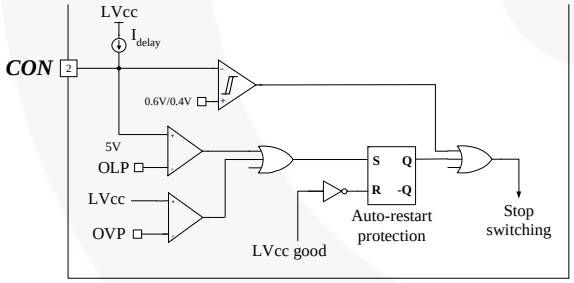


Figure 21. Internal Block of Control Pin

Protection: When the control pin voltage exceeds 5V, protection is triggered. Detailed applications are described in the protection section.

Pulse Skipping: FSFR-series stops switching when the control pin voltage drops below 0.4V and resumes switching when the control pin voltage rises above 0.6V. To use pulse-skipping, the control pin should be connected to the opto-coupler collector pin. The frequency that causes pulse skipping is given as:

$$f^{SKIP} = \left(\frac{5.2k\Omega}{R_{\min}} + \frac{4.16k\Omega}{R_{\max}}\right) x100(kHz) \quad (5)$$

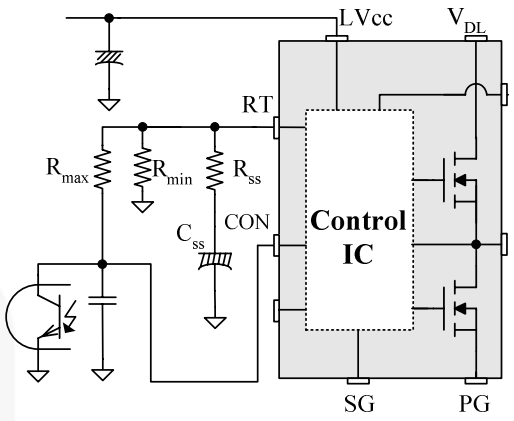


Figure 22. Control Pin Configuration for Pulse Skipping

Remote On / Off: When an auxiliary power supply is used for standby, the main power stage using FSFR-series can be shut down by pulling down the control pin voltage, as shown in Figure 23. R1 and C1 are used to ensure soft-start when switching resumes.

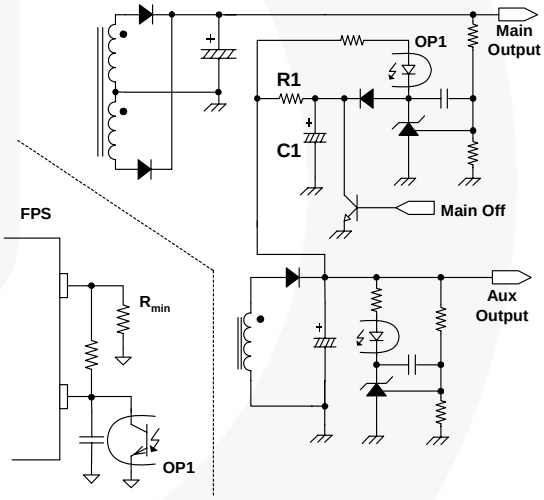


Figure 23. Remote On / Off Circuit

5. Protection Circuits: The FSFR-series has several self-protective functions, such as Overload Protection (OLP), Over-Current Protection (OCP), Abnormal Over-Current Protection (AOCP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). OLP, OCP, and OVP are auto-restart mode protections, while AOCP and TSD are latch-mode protections, as shown in Figure 24.

Auto-restart Mode Protection: Once a fault condition is detected, switching is terminated and the MOSFETs remain off. When LVcc falls to the LVcc stop voltage of 11V, the protection is reset. The FPS resumes normal operation when LVcc reaches the start voltage of 14V.

Latch-Mode Protection: Once this protection is triggered, switching is terminated and the MOSFETs remain off. The latch is reset only when LVcc is discharged below 5V.

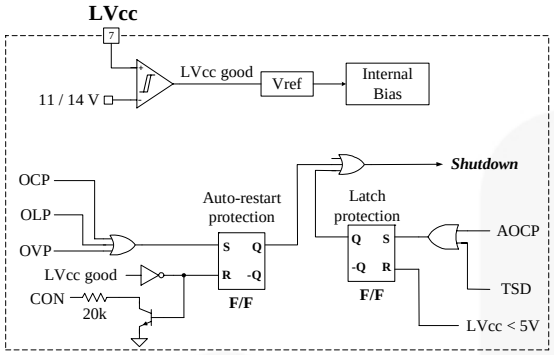


Figure 24. Protection Blocks

Current Sensing Using Resistor: FSFR-series senses drain current as a negative voltage, as shown in Figure 25 and Figure 26. Half-wave sensing allows low power dissipation in the sensing resistor while full-wave sensing has less switching noise in the sensing signal.

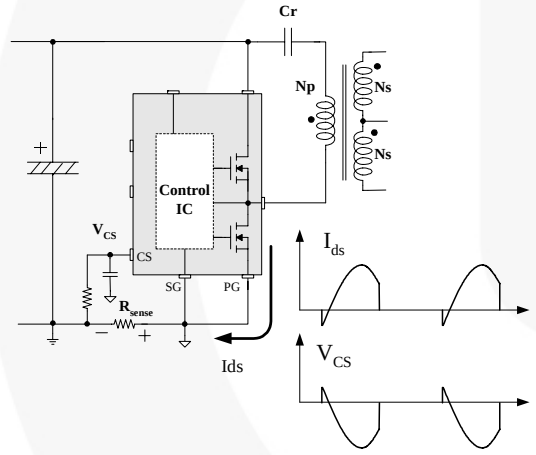


Figure 25. Half-wave Sensing

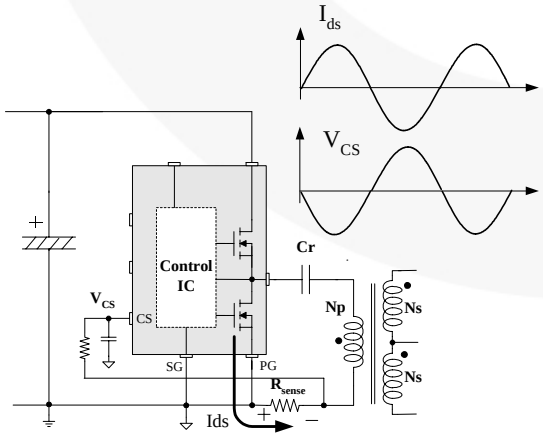


Figure 26. Full-wave Sensing

Current Sensing Using Resonant Capacitor Voltage: For high-power applications, current sensing using a resistor may not be available due to the severe power dissipation in the resistor. In that case, indirect current sensing using the resonant capacitor voltage can be a good alternative because the amplitude of the resonant capacitor voltage (V_{Cr}^{p-p}) is proportional to the resonant current in the primary side (I_p^{p-p}) as:

$$V_{Cr}^{p-p} = \frac{I_p^{p-p}}{2\pi f_s C_r} \quad (6)$$

To minimize power dissipation, a capacitive voltage divider is generally used for capacitor voltage sensing, as shown in Figure 27.

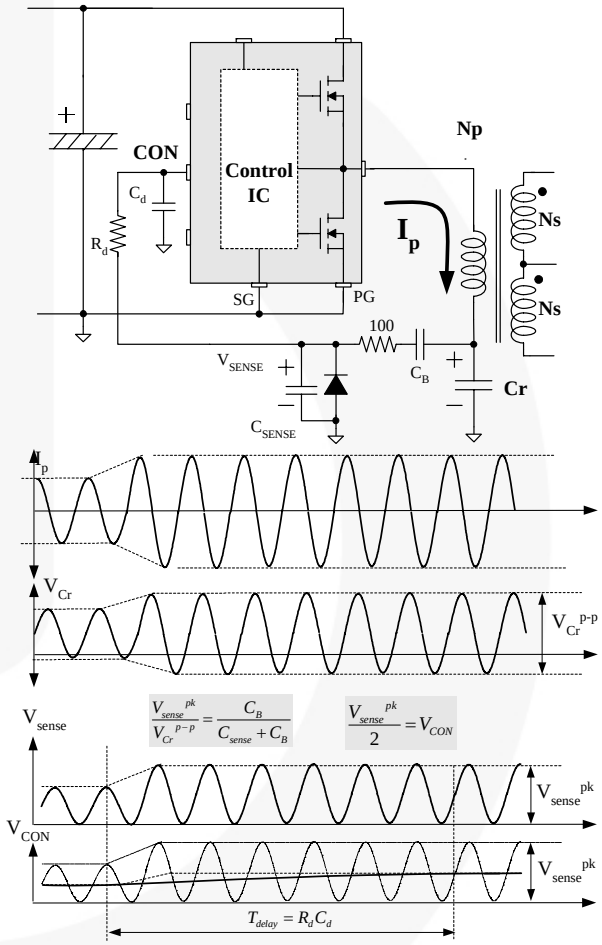


Figure 27. Current Sensing Using Resonant Capacitor Voltage

5.1 Over-Current Protection (OCP): When the sensing pin voltage drops below -0.6V, OCP is triggered and MOSFETs remain off. This protection has a shutdown time delay of 1.5μs to prevent premature shutdown during start-up.

5.2 Abnormal Over-Current Protection (AOCP): If the secondary rectifier diodes are shorted, large current with extremely high di/dt can flow through the MOSFET before OCP or OLP is triggered. AOCP is triggered without shutdown delay when the sensing pin voltage drops below -0.9V. This protection is latch mode and reset when LVcc is pulled down below 5V.

5.3 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the power supply. However, even when the power supply is in the normal condition, the overload situation can occur during the load transition. To avoid premature triggering of protection, the overload protection circuit should be designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Figure 27 shows a typical overload protection circuit. By sensing the resonant capacitor voltage on the control pin, the overload protection can be implemented. Using RC time constant, shutdown delay can be also introduced. The voltage obtained on the control pin is given as:

$$V_{CON} = \frac{C_B}{2(C_B + C_{sense})} V_{Cr}^{p-p} \quad (7)$$

where V_{Cr}^{p-p} is the amplitude of the resonant capacitor voltage.

5.4 Over-Voltage Protection (OVP): When the LVcc reaches 23V, OVP is triggered. This protection is used when auxiliary winding of the transformer to supply V_{CC} to FPS is utilized.

5.5 Thermal Shutdown (TSD): The MOSFETs and the control IC in one package makes it easy for the control IC to detect the abnormal over-temperature of the MOSFETs. If the temperature exceeds approximately 130°C, the thermal shutdown triggers.

Typical Application Circuit (Half-bridge LLC Resonant Converter)

Application	FPS™ Device	Input Voltage Range	Rated Output Power	Output Voltage (Rated Current)
LCD TV	FSFR2100	400V (20ms hold-up time)	192W	24V-8A

Features

- High efficiency (>94% at $400V_{DC}$ input)
- Reduced EMI noise through zero-voltage-switching (ZVS)
- Enhanced system reliability with various protection functions

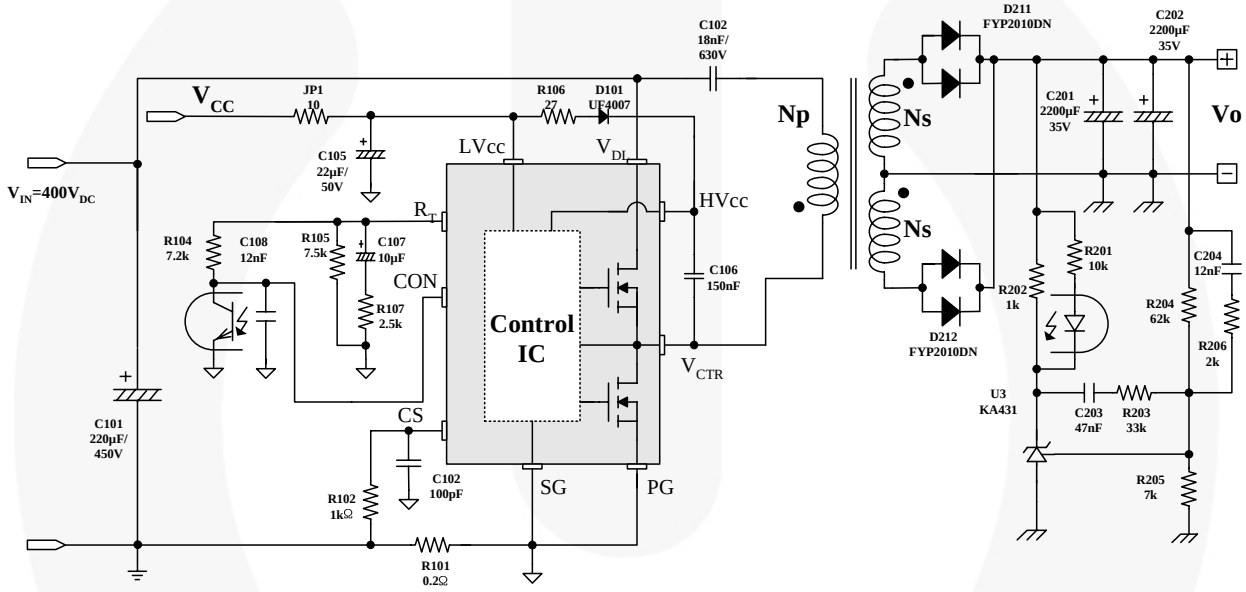
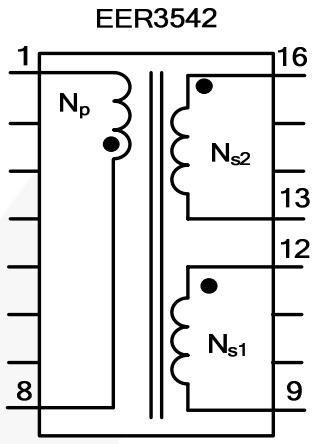


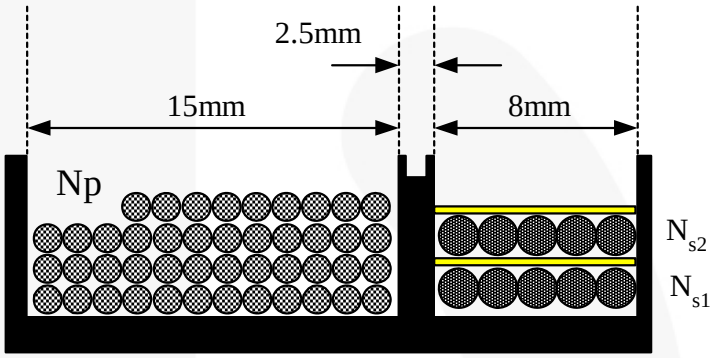
Figure 28. Typical Application Circuit

Typical Application Circuit (Continued)

Usually, LLC resonant converter requires large leakage inductance value. To obtain a large leakage inductance, sectional winding method is used.

- Core: EER3542 (Ae=107 mm^2)
- Bobbin: EER3542 (Horizontal)





	Pin(S → F)	Wire	Turns	Winding Method
N_p	8 → 1	0.12φ×30 (Litz wire)	45	Section winding
N_{s1}	12 → 9	0.1φ×100 (Litz wire)	5	Section winding
N_{s2}	16 → 13	0.1φ×100 (Litz wire)	5	Section winding

	Pin	Specification	Remark
Primary-side Inductance (L_P)	1–8	630μH ± 5%	100kHz, 1V
Primary-side Effective Leakage (L_R)	1–8	145μH ± 5%.	Short one of the secondary windings

Physical Dimensions

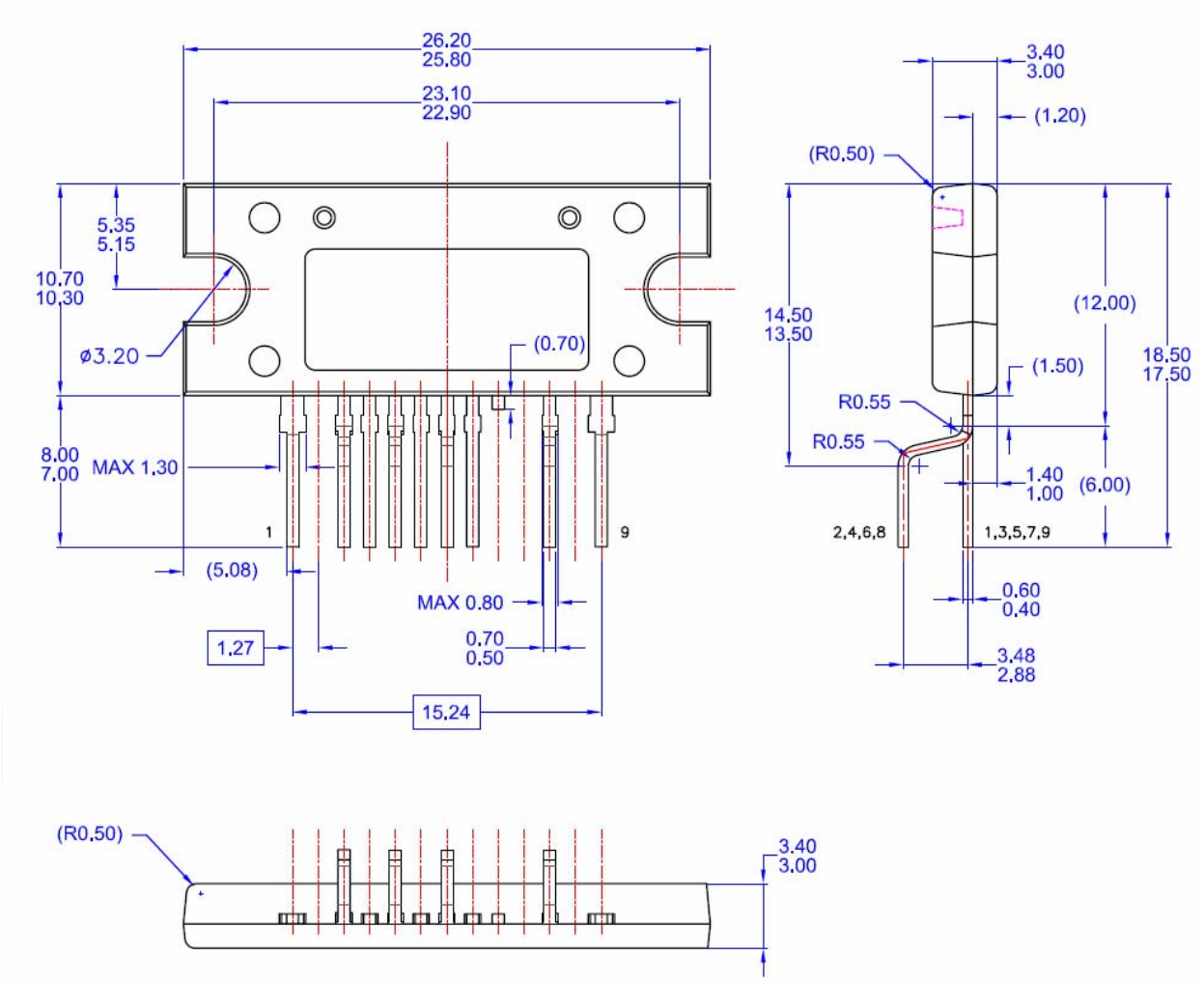


Figure 29. 9-SIP Package

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