TRAILING EDGE PRODUCT - MINIMUM ORDER APPLIES

PRODUCT MAY BE MADE OBSOLETE WITHOUT NOTICE

hmp

128K x 8 SRAM

MSM8128 - 70/85/10/12

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Description

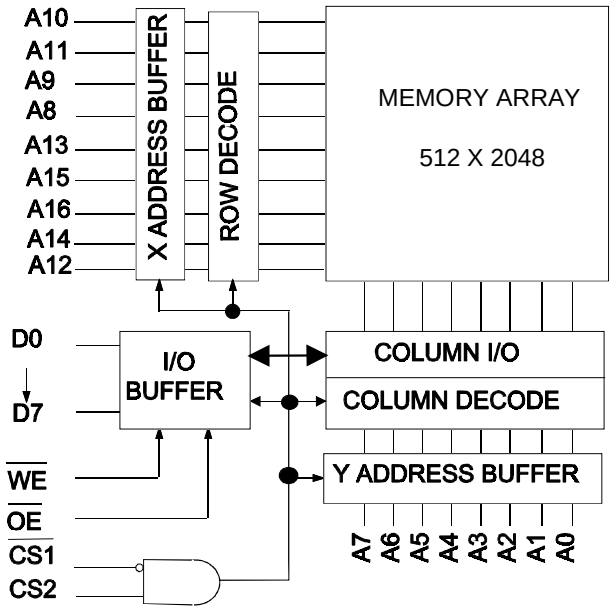
The MSM8128 is a 1Mbit monolithic SRAM organised as 128K x 8. It is currently available in a VIL Package, with access times of 70, 85, 100, 120ns. It has a low power standby version and has 3.0V battery backup capability. It is directly TTL compatible and has common data inputs and outputs.
Two pinout variants (single and dual $\overline{CS}$) are available.
All versions may be screened in accordance with MIL-STD-883.

131,072 x 8 CMOS Static RAM

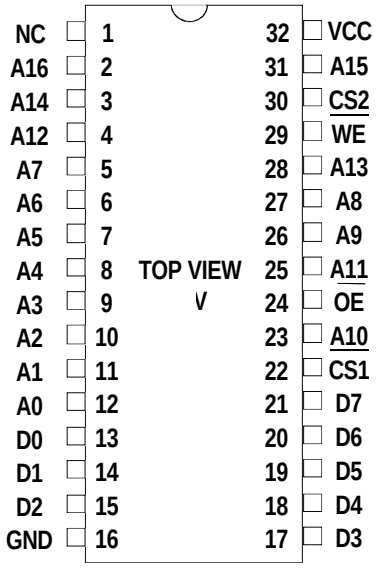
Features

Access Times of 70/85/100/120 ns
JEDEC standard Dual $\overline{CS}$ footprints.
Operating Power 550 mW (max)
Low Power Standby (-L) 2.2 mW (max)
Low Voltage Data Retention.
Completely Static Operation
Directly TTL compatible.
May be processed in accordance with MIL-STD-883

Block Diagram



Pin Definition



See Page 9 for VX

Pin Functions

A0-A16	Address Inputs
D0-7	Data Input/Output
$\overline{CS1}$	Chip Select 1
CS2	Chip Select 2
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
NC	No Connect
V_{cc}	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type
32	0.1" Vertical-in-LIne (VIL™)	V

Package details on pages 8 & 9.

DC OPERATING CONDITIONS

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5V	to	+7.0	V
Power Dissipation	P_T		1		W
Storage Temperature	T_{STG}	-55	to	+150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	5.8	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (**I** suffix)
	T_{AM}	-55	-	125	°C (**M**, **MB** suffix)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IH}=0V to V_{cc}	-2	-	2	µA
Output Leakage Current	$I_{I/O}$	$\overline{CS1}$=V_{IH}, CS2 =V_{IL}, $V_{I/O}$=0V to V_{cc} ,$\overline{OE}$=V_{IH}	-2	-	2	µA
Average Supply Current	I_{CC1}	Min. Cycle, V_{IN}=V_{IL} or V_{IH}	-	-	110	mA
Standby Supply Current	I_{SB1}	$\overline{CS1}$=V_{IH},CS2 = V_{IL} , I/P's static	-	-	4	mA
-L Part	I_{SB2}	$\overline{CS1}$≥V_{CC}-0.2V, 0.2V≥CS2≥V_{CC}-0.2V , V_{IN} ≥ 0.2V	-	-	450	uA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4	-	-	V

Capacitance (V_{CC}=5V±10%,T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
I/P Capacitance	C_{IN}	V_{IN}=0V	-	9	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	11	pF

Note: This parameter is not 100% tested.

Operating Modes

The table below shows the logic inputs required to control the MSM8128 SRAM.

Mode	*$\overline{CS1}$*	*CS2*	*$\overline{OE}$*	*$\overline{WE}$*	*V_{CC} Current*	*I/O Pin*	*Reference Cycle*
Not Selected	1	X	X	X	I_{SB1},I_{SB2}	High Z	Power Down
Not Selected	X	0	X	X	I_{SB},I_{SB1}	High Z	Power Down
Output Disable	0	1	1	1	I_{CC}	High Z	
Read	0	1	0	1	I_{CC}	D_{OUT}	Read Cycle
Write	0	1	X	0	I_{CC}	D_{IN}	Write Cycle

1 = V_{IH}, 0 = V_{IL}, X = Don't Care

Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

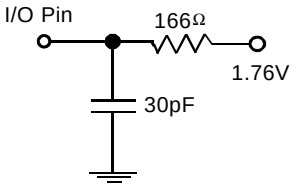
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1}$ ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V. V_{IN} ≥ 0V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V,V_{IN} ≥ 0V, $\overline{CS1}$ ≥V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or 0V ≤ CS2 ≤ 0.2V.	-	-	660	µA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes (1) CS2 controls address buffer, WE buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer. If CS2 controls data retention mode, Vin levels ($\overline{WE}$,$\overline{OE}$,$\overline{CS1}$,I/O) can be in the high impedance state. If $\overline{CS1}$ controls Data Retention mode, CS2 must be ≥ V_{CC} - 0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, $\overline{WE}$,$\overline{OE}$,I/O) can be in the high impedance state.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Load Diagram
* V_{cc}=5V±10%

Output Load



AC OPERATING CONDITIONS

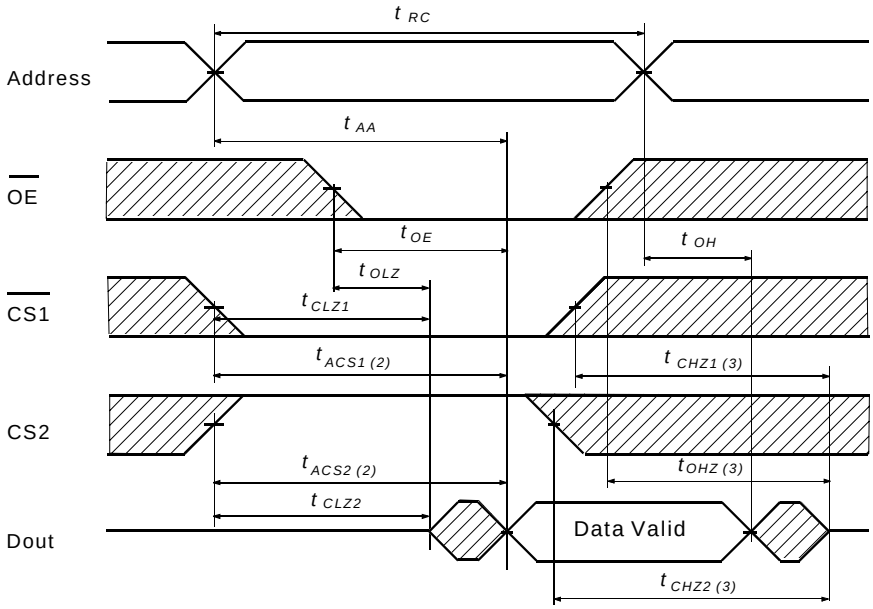
Read Cycle

Parameter	Symbol	70 min	70 max	85 min	85 max	10 min	10 max	12 min	12 max	Unit
Read Cycle Time	t_{RC}	70	-	85	-	100	-	120	-	ns
Address Access Time	t_{AA}	-	70	-	85	-	100	-	120	ns
Chip Select ($\overline{CS1}$) Access Time(2)	t_{ACS1}	-	70	-	85	-	100	-	120	ns
Chip Select (CS2) Access Time(2)	t_{ACS2}	-	70	-	85	-	100	-	120	ns
Output Enable to Output Valid	t_{OE}	-	35	-	45	-	50	-	60	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	10	-	10	-	ns
Chip Selection ($\overline{CS1}$) to Output in Low Z	t_{CLZ1}	10	-	10	-	10	-	10	-	ns
Chip Selection (CS2) to Output in Low Z	t_{CLZ2}	10	-	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	5	-	ns
Chip Disable ($\overline{CS1}$) to Output in High Z(3)	t_{CHZ1}	0	35	0	35	0	35	0	45	ns
Chip Disable (CS2) to Output in High Z(3)	t_{CHZ2}	0	35	0	35	0	35	0	45	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	30	0	30	0	35	0	45	ns

Write Cycle

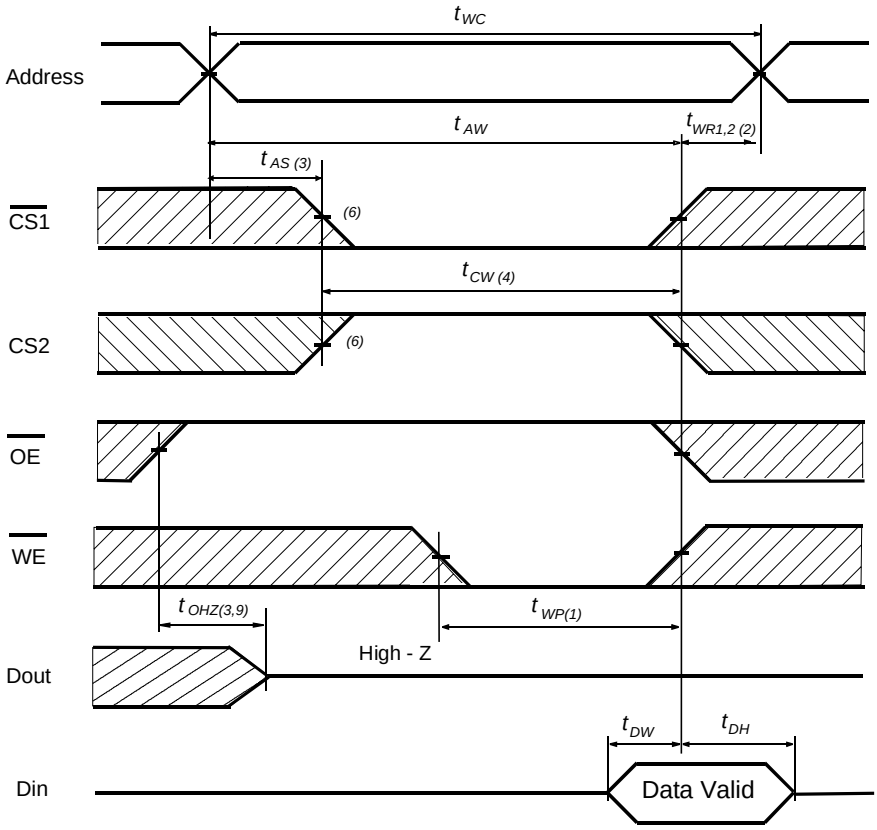
Parameter	Symbol	70 min	70 max	85 min	85 max	10 min	10 max	12 min	12 max	Unit
Write Cycle Time	t_{WC}	70	-	85	-	100	-	120	-	ns
Chip Selection to End of Write	t_{CW}	60	-	75	-	85	-	100	-	ns
Address Valid to End of Write	t_{AW}	60	-	75	-	85	-	100	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	50	-	60	-	70	-	70	-	ns
Write Recovery Time ($\overline{WE}$, $\overline{CS1}$)	t_{WR1}	5	-	5	-	5	-	5	-	ns
(CS2)	t_{WR2}	5	-	5	-	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}	0	30	0	30	0	35	0	40	ns
Data to Write Time Overlap	t_{DW}	30	-	35	-	40	-	45	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	5	-	ns

Read Cycle Timing Waveform (1,2)

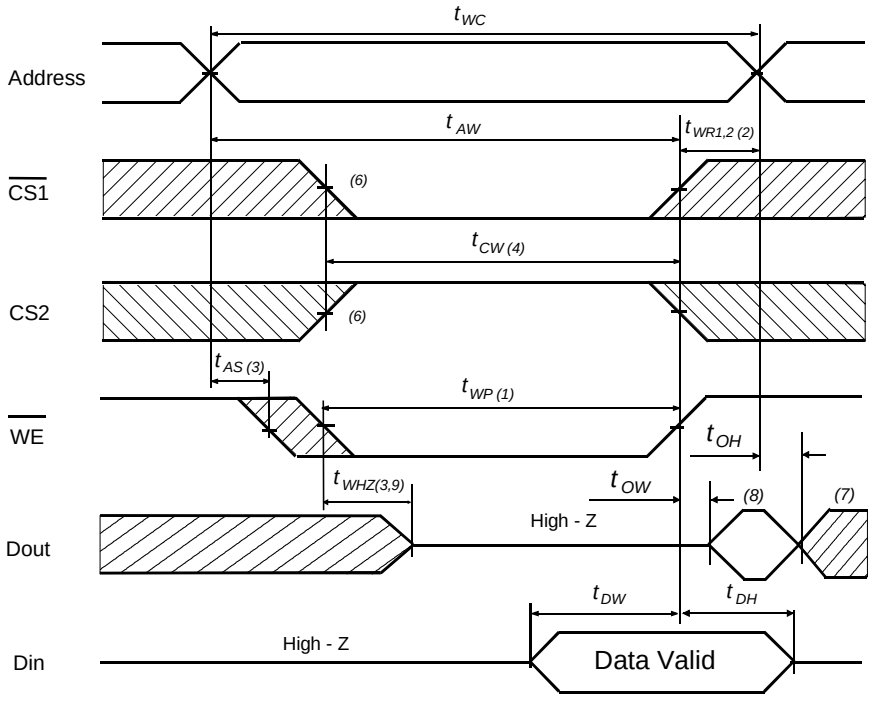


Notes:
(1) $\overline{WE}$ is High for Read Cycle.
(2) Address valid prior to or coincident with $\overline{CS1}$ transition low or CS2 high.
(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min both for a given device and from device to device. This parameter is sampled and not 100% tested.

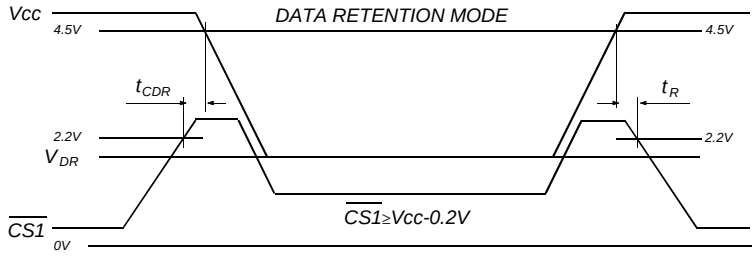
Write Cycle No.1 Timing Waveform



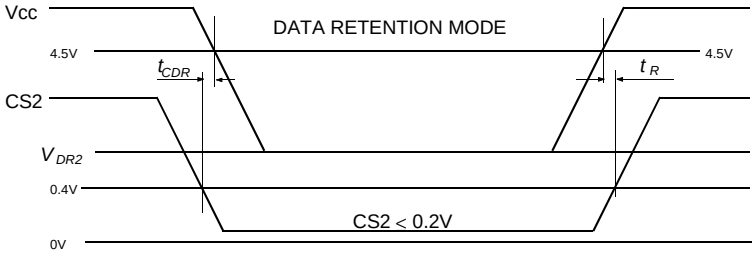
Write Cycle No.2 Timing Waveform (5)



Low V_{cc} Data Retention Timing Waveform 1 ($\overline{CS1}$ controlled)



Low V_{cc} Data Retention Timing Waveform 2 (CS2 controlled)



AC Characteristics Notes

(1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

(2) t_{WR} is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, outputs remain in high impedance state.

(5) OE is continuously low. ($\overline{OE}$=V_{IL})

(6) Dout is in the same phase as written data of this write cycle.

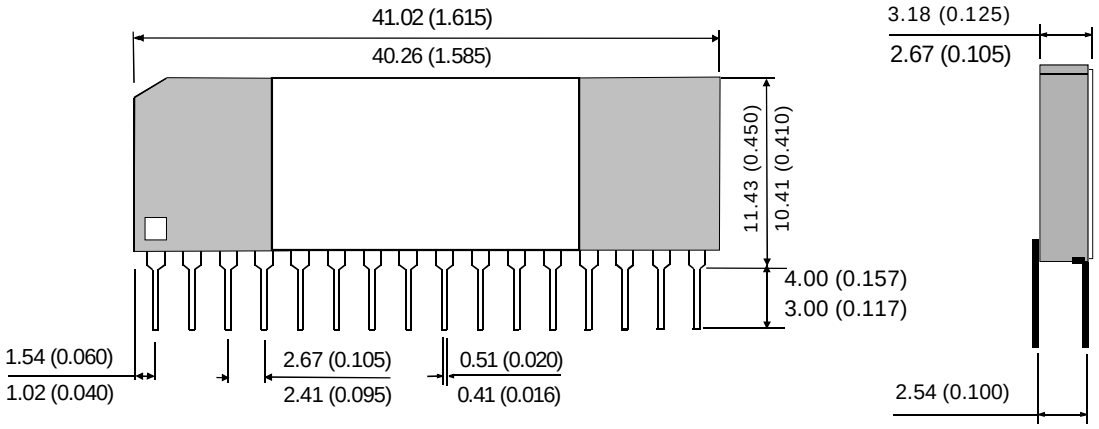
(7) Dout is the read data of next address.

(8) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.

(9) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. These parameters are sampled and not 100% tested.

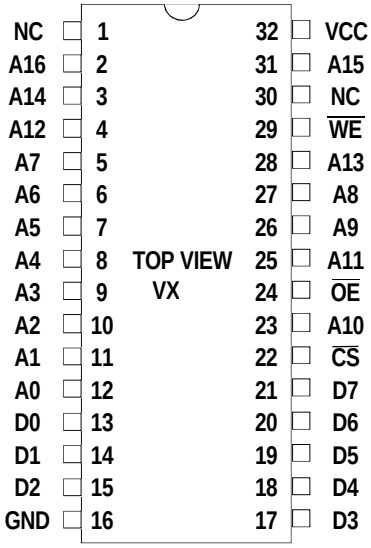
Package Details

32 pin 0.1" Vertical-in-Line (VIL™) - 'V' Package



All dimensions in mm (inches).

Alternate Pin Definition



Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883 method 5004

MB COMPONENT SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM8128VLMB - 70

Speed	70	= 70 ns
	85	= 85 ns
	10	= 100 ns
	12	= 120 ns
Temp. range/screening	Blank	= Commercial
	I	= Industrial
	M	= Military
	MB	= Screened in accordance with MIL-STD-883.
Power Consumption	Blank	= Standard Power
	L	= Low Power
Package		
	V	= 32 pin 0.1" VIL
	VX	= 32 pin 0.6" VIL (Single CS
Organisation	8128	= 128K x 8 SRAM

THE ABOVE PARTS ARE NOT RECOMMENDED FOR NEW DESIGNS AND MAY BE MADE OBSOLETE WITHOUT NOTICE.