



# YTD436

## ISTC

### ISDN BRI controller with S/T ref. pt. analog D/R

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YTD436 is a high-performance communication LSI for the ISDN BRI user-network interface function (digital four-wire time-division full-duplex operation), supporting D channel layer 1 and layer 2 functions in one 100-pin SQFP chip.

YTD436 supports layer 1 (physical layer) control function conforming to ITU-T Recommendation I.430 and fully supports layer 2 (LAPD protocol) function conforming to ITU-T Recommendations Q.920 and Q.921. ETSI (European Telecommunication Standards Institute) and North American standard operating modes are also supported.

In addition, YTD436 includes layer 3 processor interface function which operate in DMA transfer mode or I/O transfer mode. This gives a great advantage for mounting and functional designing of both “active” (CPU on board) terminal equipment and “passive” (no CPU on board) PC cards.

The layer 1 function has a built-in S/T reference point analog driver/receiver to support the S/T reference point interface. In order to support the U interface, YTD436 also has a I.430 TTL interface (no built-in analog driver/receiver) suitable for connecting to an NT1 chip or a DSU module.

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YTD436 CATALOG
CATALOG No.:4TD436A41
2005.1

## Features

### 1. Layer 1 function

- Conforms to ITU-T Recommendation I.430 (1992 edition) and TTC Standard JT-I430 (1997 edition) (default)
  - 192 kbps transmission rate
  - Interface structure : 2B + D (B = 64 kbps, D = 16 kbps)
  - Frame assembling and disassembling function
  - Collision control (built-in random number (Ri) reset), priority control (built-in retransmission control), and state transition control
  - Programmable T3 and T4 timers
- Supports ETSI ETS 300 012 (April 1992) and ANSI T1.605 operating modes
- Leased line capability (JT-I430-a)
- Built-in driver and receiver
  - I.430 TTL interface (when the driver / receiver is disconnected)
  - No external relay or common-mode choke needed
  - Supports 1-to-2 pulse transformer
- Abundant Test functions (for testing and maintenance)
  - Demo mode in which no switch simulator is needed.
  - Three kinds of loop-back modes (Loop-back 1 to 3)
  - INFO signals output for testing
  - Test pulse output for pulse shape check
- Multiframe capability
- INFO1 transmission and INFO4 reception monitor pins
- Power down monitor pin
- I.430 transmission frame phase adjustment function

### 2. Layer 2 function

- Conforms to ITU-T Recommendation Q.920 (1992 edition) and Q.921 (1997 edition) and TTC Standard JT-Q920 (1993 edition) and JT-Q921 (1998 edition)
  - HDLC frame control (Flag control, FCS generation/checking, Automatic zero insertion/deletion, Abort pattern transmission/detection, etc.)
  - LAPD status control (Sequence control, Flow control, SAPI control)
  - Built-in timer for time-out check
- Supports ETSI ETS 300 125 (September 1991), National ISDN-1/2, AT&T 5ESS 5E9 and Nortel DMS-100 S208-6 operating modes
- Multilink capability  
(circuit switching × 2 links, packet switching/teleaction communications × 2 links)
- Automatic assigned TEI/non-automatic assigned TEI (VC/PVC)
- Leased line mode (disable layer 2 function)

### 3. Layer 3 interface function

- Connects to 8-bit or 16-bit microprocessor  
(8086 family, 80186 family, 6800 family, 68000 family)
- Operates in one of two data transfer modes :
  - DMA transfer mode (with the built-in 16-bit address DMA controller)
  - I/O transfer mode (with the built-in FIFO)
- Primitive logical interface

### 4. B channel interface

- Data rate setting : 64 k, 56 k and 32 kbps
- Serial mode
  - B channel I/O clock selection function
    - Internal clock mode  
Inputs/outputs the B channel data with 64 k, 56 k or 32 kHz internal clock
    - External clock mode (PCM Highway mode)  
Inputs/outputs the B channel data with a 128 k to 2048 kHz external clock
  - B channel selection function
    - Internal clock mode  
Selects/switches B channel I/O pins
    - External clock mode (PCM Highway mode)  
Selects/switches B channel time slots
- Parallel mode
  - LSB/MSB switching function
  - Bit shift function
  - Data transfer mode
    - DMA transfer mode with the DMA request function
    - I/O transfer mode with the built-in FIFO

### 5. Low-power operation

(Host processor clock control function, Powerdown mode)

### 6. High-performance CMOS technology

### 7. 100-pin SQFP

### 8. Digital Supply Voltage (+5V or +3.3V ), Analog +5V supply

## **Applications**

- **ISDN telephone**
- **Video telephone**
- **Telemeter**
- **PBX**
- **Terminal adapter (TA)**
- **Other ISDN terminals**

## Functional Comparison of YAMAHA ISDN S/T Interface LSIs

FUNCTION		YTD410	YM7405B	YTD418	YTD423	YTD436
Layer 1	ITU-T Recommendation I.430	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition
	TTC Standard JT-I430	1993 edition	1993 edition	1993 edition	1993 edition	1997 edition
Layer 2 (LAPD)	ITU-T Recommendation Q.920 Q.921	1992 edition	1992 edition	1992 edition	1992 edition	1992 edition 1997 edition
	TTC Standard JT-Q920 JT-Q921	1993 edition	1993 edition	1993 edition	1993 edition	1993 edition 1998 edition
ETSI ETS 300 012, ETS 300 125			√	√	√	√
North American Switches National ISDN-1/2, AT&T 5ESS, Nortel DMS-100					√	√
S/T Reference Point Analog Driver/Receiver		Internal	Internal	External [YTD421B]	External [YTD421B]	Internal
Maximum D Channel Links	Circuit Switching	1	2	2	2	2
	Dch Packet Switching (Teleaction Communication)	1	2	2	2	2 (2)
D Channel Layer 3 Data Transfer Method		DMA Transfer	DMA Transfer	DMA Transfer	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer
HDLC Controller and DMA Controller for B Channel Data		External	External	External	Internal	Internal
B Channel Data Transfer Method		-	-	-	DMA Transfer or I/O Transfer	DMA Transfer or I/O Transfer <b>(Note 1)</b>
B Channel Internal Clock Mode (kHz)		56, 64	64	64	32, 56, 64	32, 56, 64
B Channel External Clock Mode			√	√	√	√
Clock Output Function for MPU		√			√	√
Signal Output Function for Testing		√			√	√
Supply Voltage (V)		+5	+5	+5	+5	+5 or +3.3 <b>(Note 2)</b>
Power Consumption during Operation [typ.] (mW)		65	125	75	85	75 (@+5V) 40 (@+3.3V)
Power Consumption during Sleep [typ.] (mW)		2	30	21	1	less than 0.5 <b>(Note 3)</b>
Package		80 pin QFP 100 pin TQFP	80 pin QFP 100 pin TQFP	80 Pin QFP	100 pin SQFP	100 pin SQFP

**Note 1:** DMA Transfer: Request function only  
I/O transfer: 4 byte FIFO

**Note 2:** With respect to Digital Supply Voltage

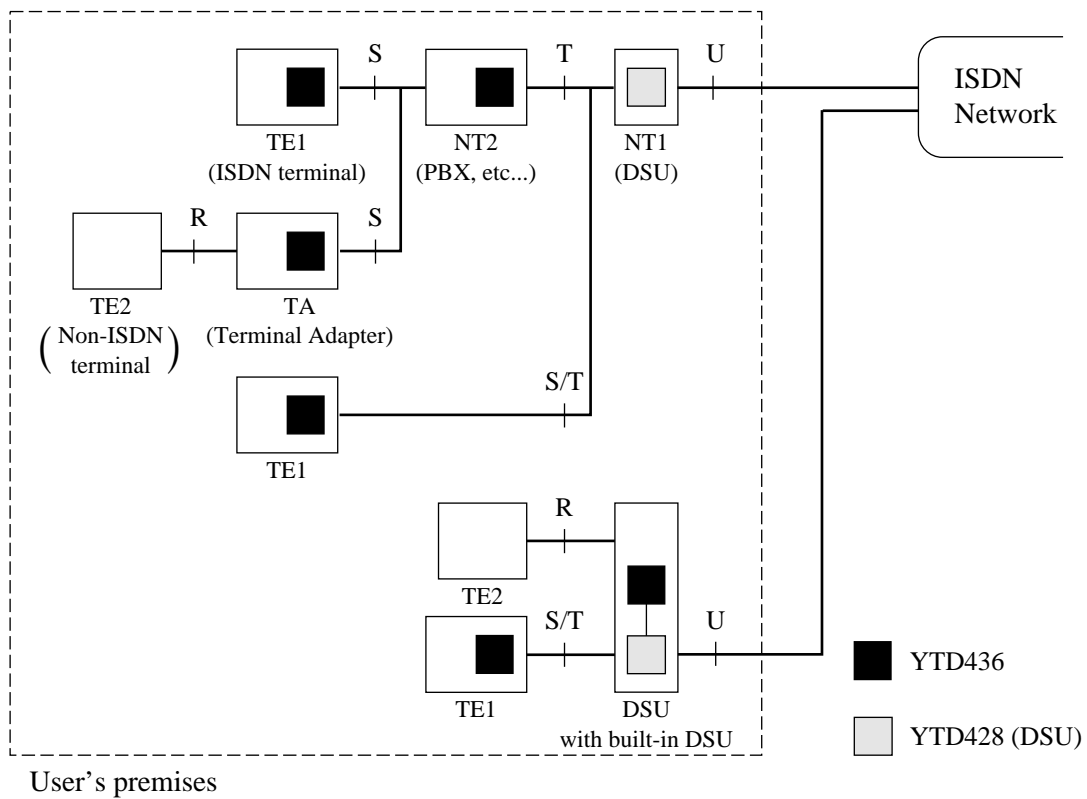
**Note 3:** State at Line interface disconnection + Power down (SLEEP state)

# BLOCK DIAGRAM

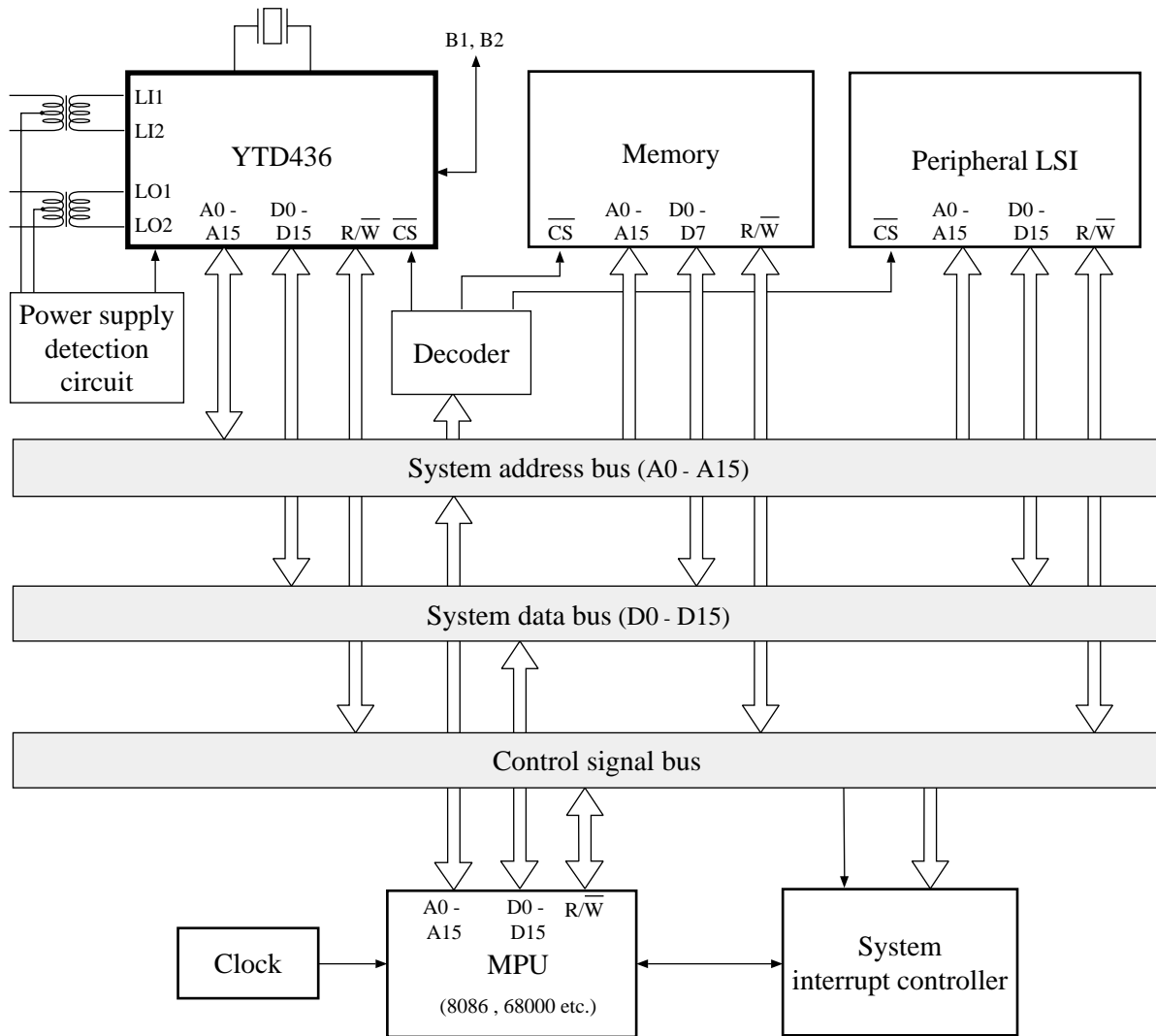
## User Network Interface Block Diagram

YTD436 is the most-suited LSI for terminal equipment such as ISDN telephones and video telephones and for PHS base stations.

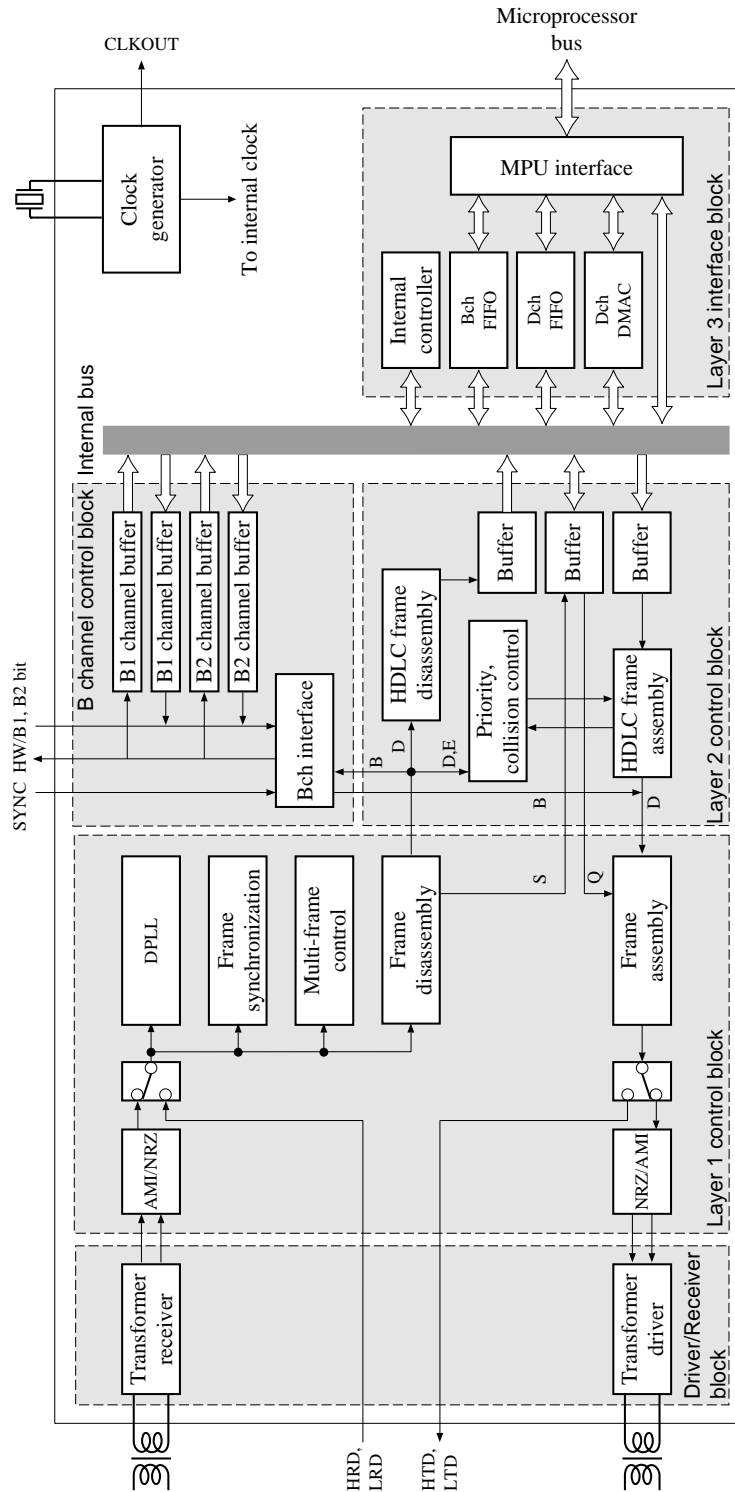
YTD436 contains layer 1 and layer 2 functions, analog driver/receiver for the S/T reference point, DMA request function for B channel data transfer, and DMA controller for D channel data transfer. Because of this, terminal equipment can be optimally configured by adding few circuits such as the layer 3 control processor.



YTD436 Peripheral LSI Interface Block Diagram

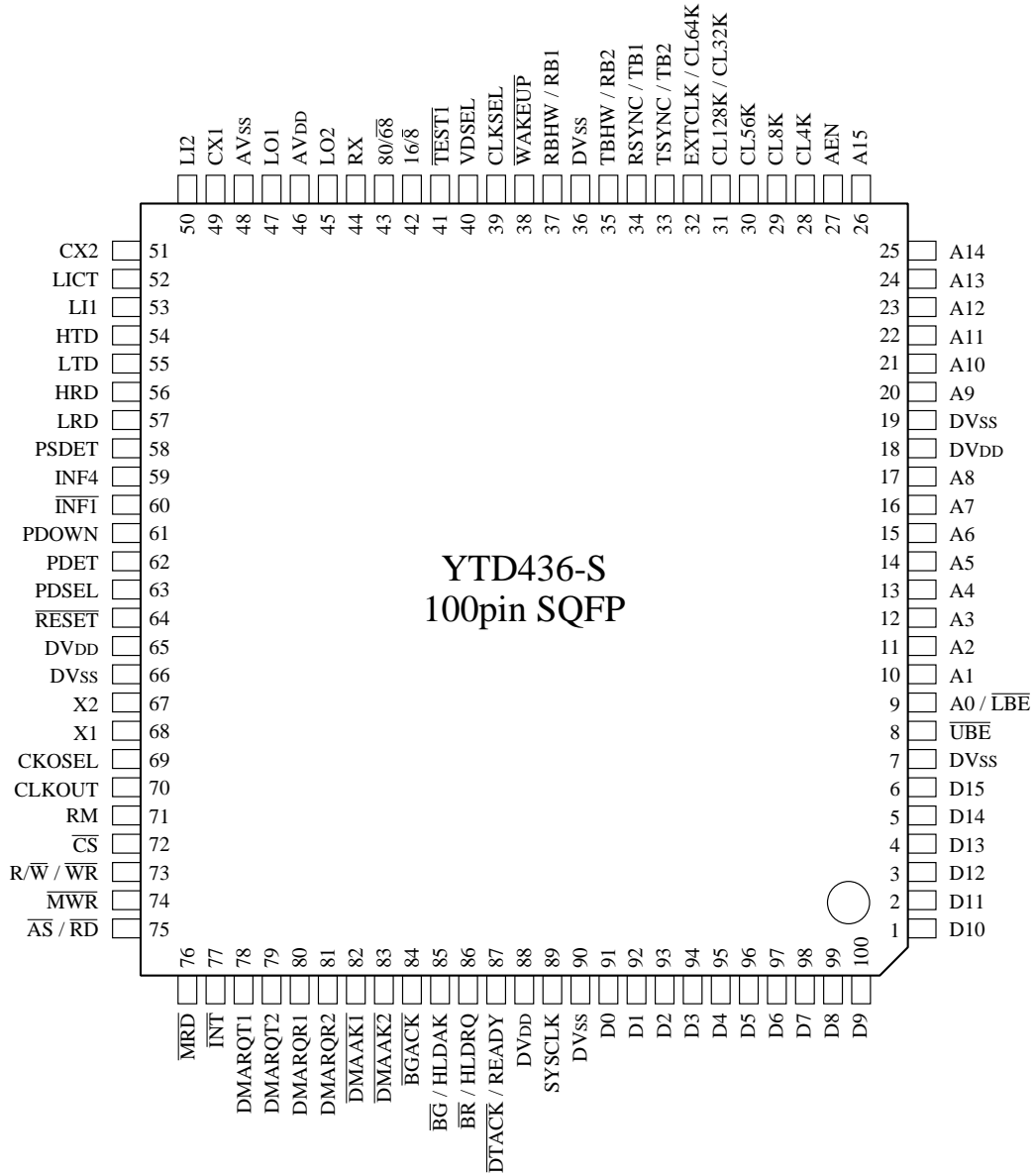


**YTD436 Internal Block Diagram**





# Pin Assignments



# ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V <sub>DD</sub>	- 0.3	+ 7.0	V
Input Voltage	DV <sub>I</sub>	- 0.3	DV <sub>DD</sub> + 0.3	V
	AV <sub>I</sub>	- 0.3	AV <sub>DD</sub> + 0.3	V
Storage Temperature	T <sub>stg</sub>	- 50	+ 125	°C

(Based on DV<sub>SS</sub> = AV<sub>SS</sub> = 0.0 V)

## Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Max.	Unit
Supply Voltage	DV <sub>DD</sub>	VDSEL="H"	4.75	5.25	V
		VDSEL="L"	3.0	3.6	V
	AV <sub>DD</sub>		4.75	5.25	V
Operating Temperature	T <sub>op</sub>		- 30	85	°C

(Based on DV<sub>SS</sub>= AV<sub>SS</sub> = 0.0 V)

## DC Characteristics

When DVDD = 5 V ± 5 %, AVDD = 5 V ± 5 % (VDSEL="H", Top = - 30 to + 85 °C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage (CMOS)	V <sub>DIH</sub>	(Note 1)	0.8DV <sub>DD</sub>			V
Low-Level Input Voltage (CMOS)	V <sub>DIL</sub>	(Note 1)			0.2DV <sub>DD</sub>	V
High-Level Input Voltage (TTL)	V <sub>DIH</sub>	(Note 2)	2.2			V
Low-Level Input Voltage (TTL)	V <sub>DIL</sub>	(Note 2)			0.8	V
High-Level Output Voltage (CMOS)	V <sub>DOH</sub>	I <sub>DOH</sub>   < 10 μA	DV <sub>DD</sub> - 0.4			V
Low-Level Output Voltage (CMOS)	V <sub>DOL</sub>	I <sub>DOL</sub>   < 10 μA			DV <sub>SS</sub> + 0.4	V
High-Level Output Voltage (TTL)	V <sub>DOH</sub>	(Note 3)	2.7			V
Low-Level Output Voltage (TTL)	V <sub>DOL</sub>	(Note 3)			0.4	V
Low-Level Output Voltage (Open-D)	V <sub>DOL</sub>	(Note 4)			0.4	V
Leakage Current	I <sub>L</sub>		-10		10	μA
Off-State Leakage Current	I <sub>LZ</sub>	(Note 5)	-10		10	μA
Power Supply Current (Digital block)	D <sub>IDD</sub>	(Note 6)		10.2		mA
		(Note 7, 9)		0.1		mA
Power Supply Current (Analog block)	A <sub>IDD</sub>	(Note 6, 10)		4.8		mA
		(Note 7, 10)		0.4		mA
		(Note 8, 10)		0.1		mA

**Note 1:** With respect to X1, PSDET, PDET, PDSEL, WAKEUP, RESET, CLKSEL, TEST1, VDSEL pins (except for the analog pins).

**Note 2:** With respect to other pins (except for the analog pins).

**Note 3:** CLKOUT pin            Test condition: I<sub>DOH</sub> = - 1.0 mA, I<sub>DOL</sub> = 2.0 mA  
 other output pins        Test condition: I<sub>DOH</sub> = - 0.4 mA, I<sub>DOL</sub> = 1.2 mA

**Note 4:** HTD, LTD, INT pin    Test condition : I<sub>DOL</sub> = 1.2 mA  
 INF1 pin                    Test condition : I<sub>DOL</sub> = 3 mA  
 RBHW pin                  Test condition : R<sub>L</sub> = 500 Ω

**Note 5:** With respect to cases in which D0 - D15, and A0 - A15 pins are in the input state and MWR and MRD pins are in Hi-Z state.

**Note 6:** RUN state (connecting with a B channel, transferring all "0", SYSCLK = 8 MHz, using internal driver/receiver, assuming as V<sub>DIH</sub> = DV<sub>DD</sub>, V<sub>DIL</sub> = DV<sub>SS</sub> )

**Note 7:** SLEEP state

**Note 8:** SLEEP state + Line interface disconnection

**Note 9:** When SYSCLK is stopped.

**Note 10:** When using internal driver/receiver

When  $DVDD = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $AVDD = 5\text{ V} \pm 5\%$  ( $VDSEL="L"$ ,  $Top = -30\text{ to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High-Level Input Voltage	$V_{DIH}$		$0.8DV_{DD}$			V
Low-Level Input Voltage	$V_{DIL}$				$0.2DV_{DD}$	V
High-Level Output Voltage	$V_{DOH}$	$ I_{DOH}  < 0.4\text{ mA}$	$DV_{DD} - 0.4$			V
Low-Level Output Voltage	$V_{DOL}$	$ I_{DOL}  < 1.2\text{ mA}$			$DV_{SS} + 0.4$	V
Low-Level Output Voltage (Open-D)	$V_{DOL}$	(Note 1)			0.4	V
Leakage Current	$I_L$		-10		10	$\mu\text{A}$
Off-State Leakage Current	$I_{LZ}$	(Note 2)	-10		10	$\mu\text{A}$
Power Supply Current (Digital block)	$D_{IDD}$	(Note 3)		4.9		mA
		(Note 4, 6)		0.1		mA
Power Supply Current (Analog block)	$A_{IDD}$	(Note 3, 7)		4.8		mA
		(Note 4, 7)		0.4		mA
		(Note 5, 7)		0.1		mA

**Note 1:**  $\overline{HTD}$ ,  $\overline{LTD}$ ,  $\overline{INT}$ ,  $\overline{INF1}$  pin Test condition :  $I_{DOL} = 1.2\text{ mA}$

$\overline{RBHW}$  pin Test condition :  $R_L = 500\ \Omega$

**Note 2:** With respect to cases in which  $D0 - D15$ , and  $A0 - A15$  pins are in the input state and  $\overline{MWR}$  and  $\overline{MRD}$  pins are in Hi-Z state.

**Note 3:** RUN state (connecting with a B channel, transferring all "0",  $SYSCLK = 8\text{ MHz}$ , using internal driver/receiver, assuming as  $V_{DIH} = DV_{DD}$ ,  $V_{DIL} = DV_{SS}$ )

**Note 4:** SLEEP state

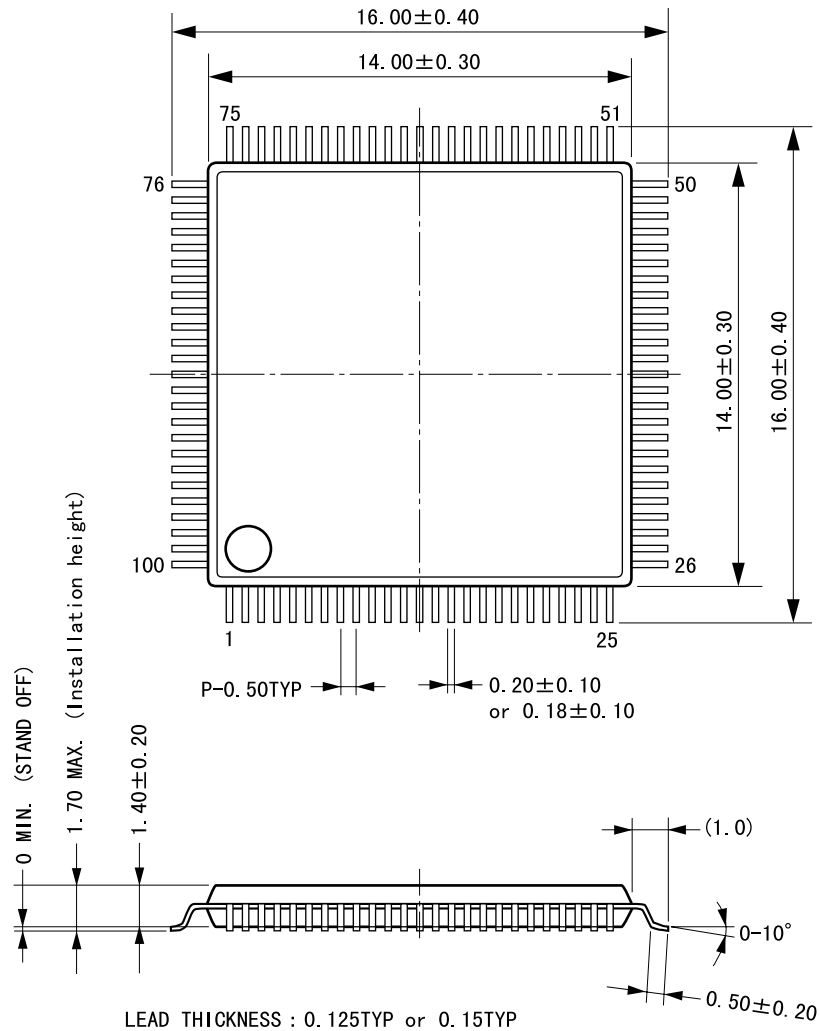
**Note 5:** SLEEP state + Line interface disconnection

**Note 6:** When  $SYSCLK$  is stopped.

**Note 7:** When using internal driver/receiver

# PACKAGE OUTLINE

C-PK100SP-1



(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.

Plastic body dimensions do not include burr of resin.

UNIT: mm

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