AU6336

USB2.0 SD/MMC Single LUN Card Reader Controller

Technical Reference Manual

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Revision History

Date	Revision	Description
Aug 2007	0.9W	Preliminary Release.
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1. Introduction

1.1 Description

AU6336 is an USB2.0 high-speed transmission controller, which is designed as a bridge between USB and SD compatible flash card interface, such as SD, HS-SD, MMC, HS-MMC, RS-MMC, MMCmicro…etc. AU6336 can read digital contents stored on memory card designed to cover a wide area of applications such as digital cameras, PDAs, MP3 players and smart phones…etc.
AU6336 inherits the high-performance and cost-efficiency character from Alcor's products, included power switch integration, dynamic icon utility support, and DMA engine integration.

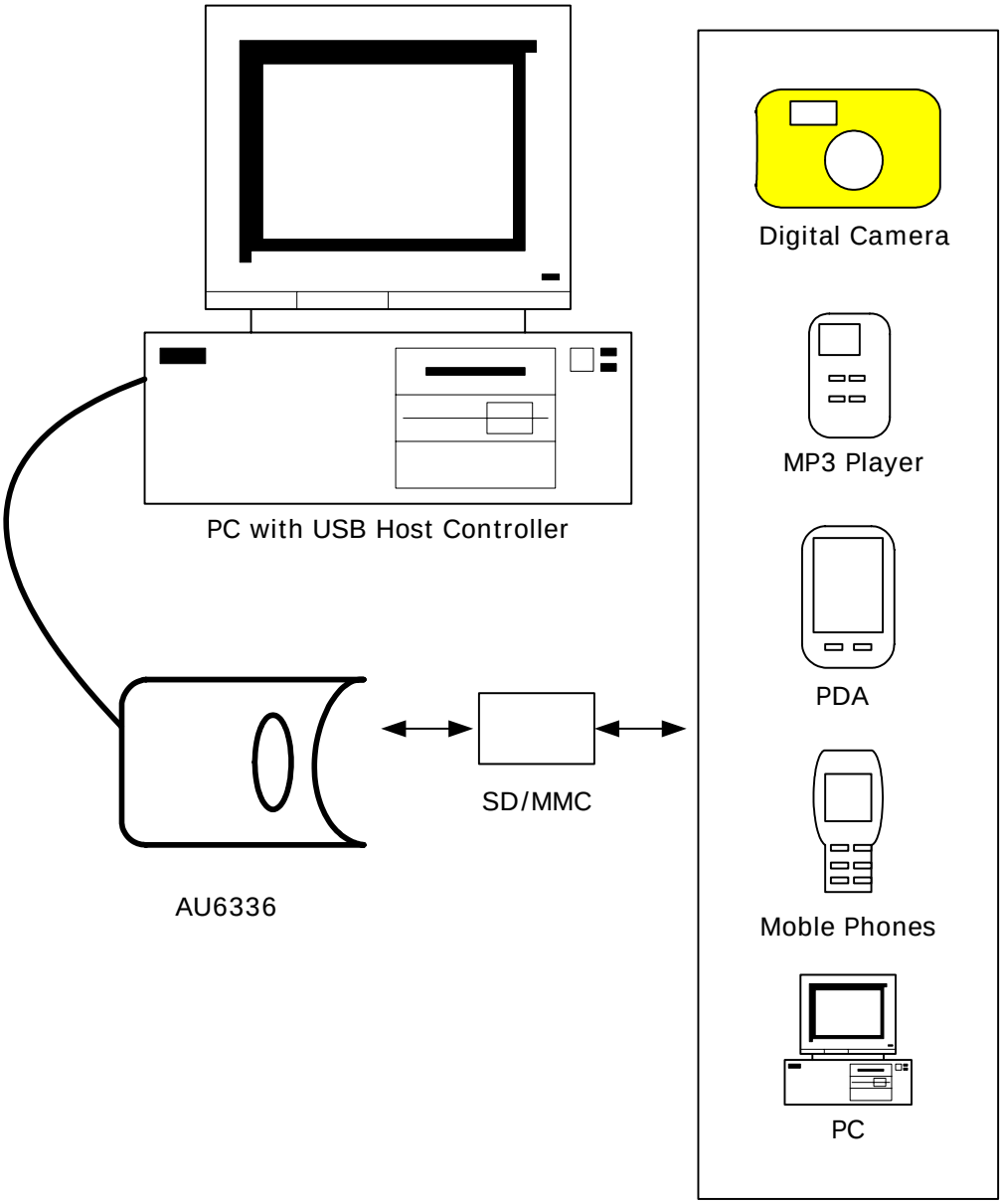
1.2 Features

- Support USB V2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0
- Support SD/MMC compatible flash card
- Support the latest flash card specification: SD2.0 (SDHC), MSPro parallel mode (4-bit)
- Alcor DMA engine integrated for performance enhancement
- Work with default driver from Windows ME/2000/XP/Vista and Mac OS X; Windows 98/2000(SP1/SP2) and Mac OS 9 are supported by vendor driver from Alcor.
- Compliant to xD 1.2 spec.
- Ping-pong FIFO implementation for concurrent bus operation.
- Support multiple sectors transfer optimize performance
- Support Dynamic Icon Utility
- Support LED for bus operating indication
- Power switch integrated to reduce production BOM cost
- 5→3.3 and 3.3→1.8V regulators built in
- 28-SSOP package for SD/MMC
- 24-QFN package for SD/MMC

2. Application Block Diagram

Following application diagram demonstrates a typical card reader using the AU6336 chip. By connecting the card reader to a desktop or notebook PC through USB bus, the AU6336 becomes a bus-powered, high speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

Figure 2.1 Block Diagram



3. Pin Assignment

There are two different form factor packages available to choose from. The following figure shows signal names for each pin and the table in the page after describes each pin in details.

Figure 3.1 AU6336-MAS Pin Assignment Diagram

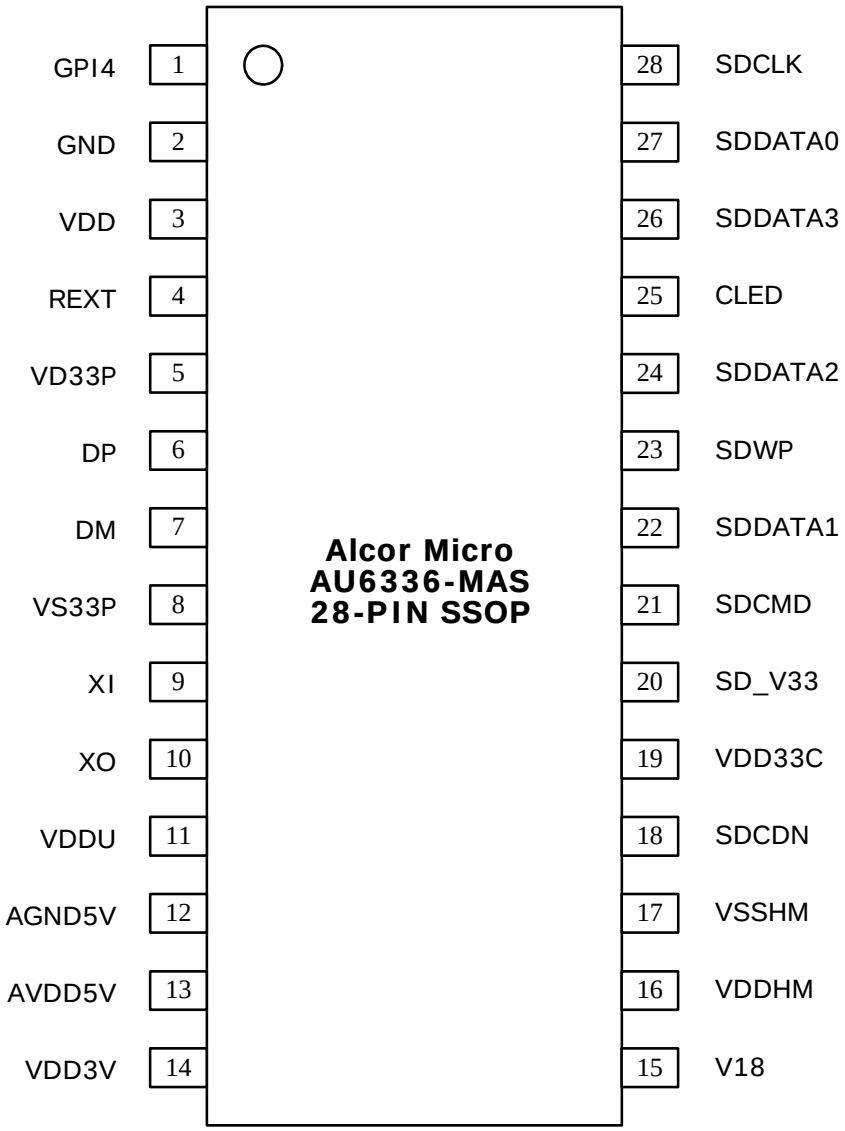


Table 3.1 AU6336-MAS Pin Descriptions

Pin #	Pin Name	I/O	Description
1	GPI4	I	Force to full speed '1' for normal [default] '0' for force to full speed.
2	GND	I	Core ground
3	VDD	I	Core 1.8V power input
4	REXT	I	UTMI reference resistor
5	VD33P	I	UTMI 3.3V power input
6	DP	I/O	USB DP
7	DM	I/O	USB DM
8	VS33P	I	UTMI 3.3V ground
9	XI	I	12MHz crystal input
10	XO	O	12MHz crystal output
11	VDDU	I	UTMI 1.8V input
12	AGND5V	I	5 to 3.3 regulator ground
13	AVDD5V	I	5 to 3.3 regulator 5V input
14	VDD3V	O	5 to 3.3 regulator 3.3V output
15	V18	I	3.3 to 1.8 regulator 1.8V output
16	VDDHM	I	IO 3.3V power / 3.3 to 1.8 regulator 3.3V input
17	VSSHM	I	IO 3.3V ground
18	SDCDN	I	SD card detect
19	VDD33C	I	Card power switch 3.3V input
20	SD_V33	O	Card power switch output
21	SDCMD	I/O	SD command
22	SDDATA1	I/O	SD data 1
23	SDWP	I	SD write protect
24	SDDATA2	I/O	SD data 2
25	CLED	O	Card Access LED
26	SDDATA3	I/O	SD data 3
27	SDDATA0	I/O	SD data 0
28	SDCLK	O	SD clock

The following figure shows signal names of each pin of the 24 QFN package and the table in the page after describes each pin in details.

Figure 3.2 AU6336-MDF Pin Assignment Diagram

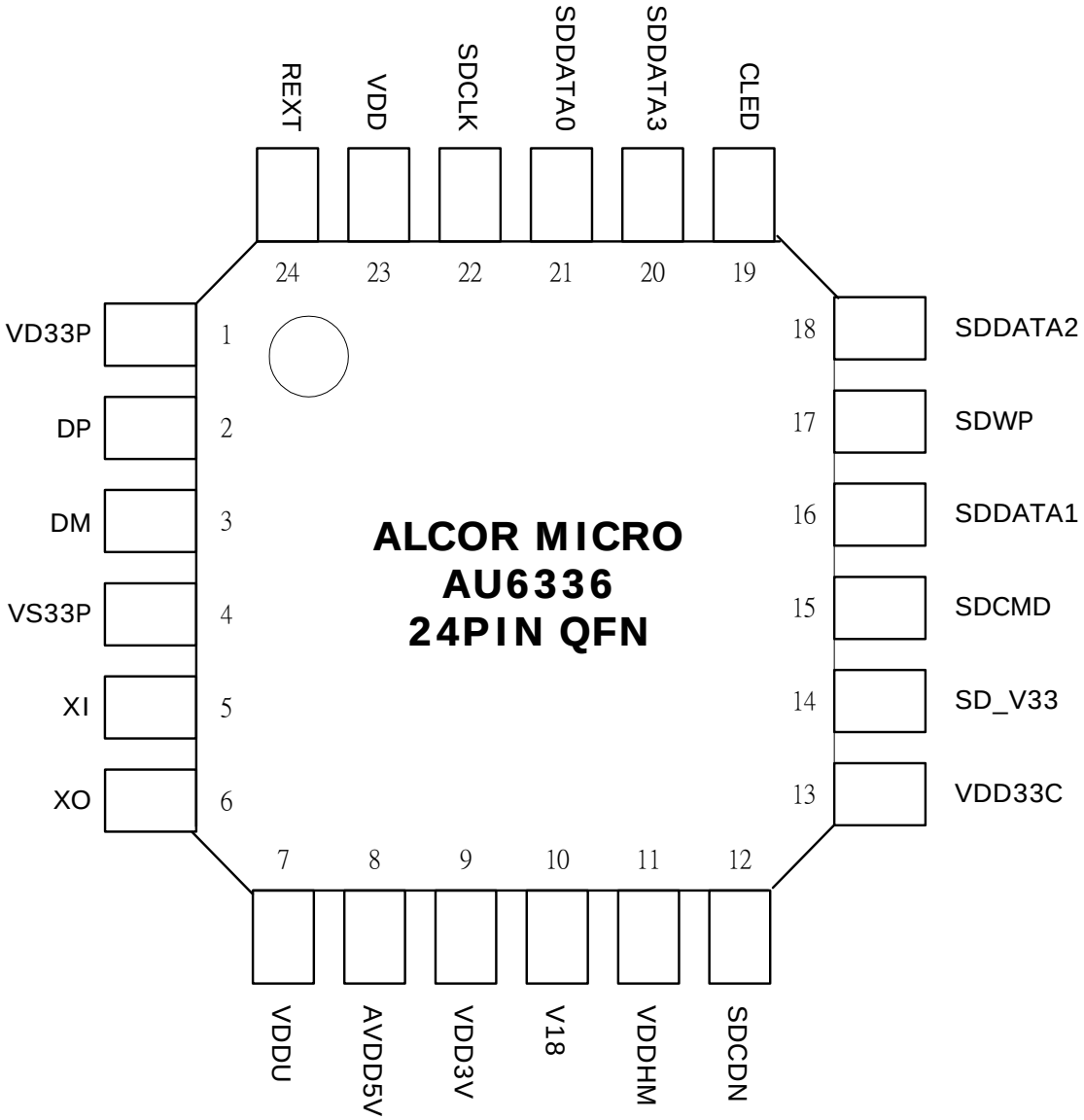


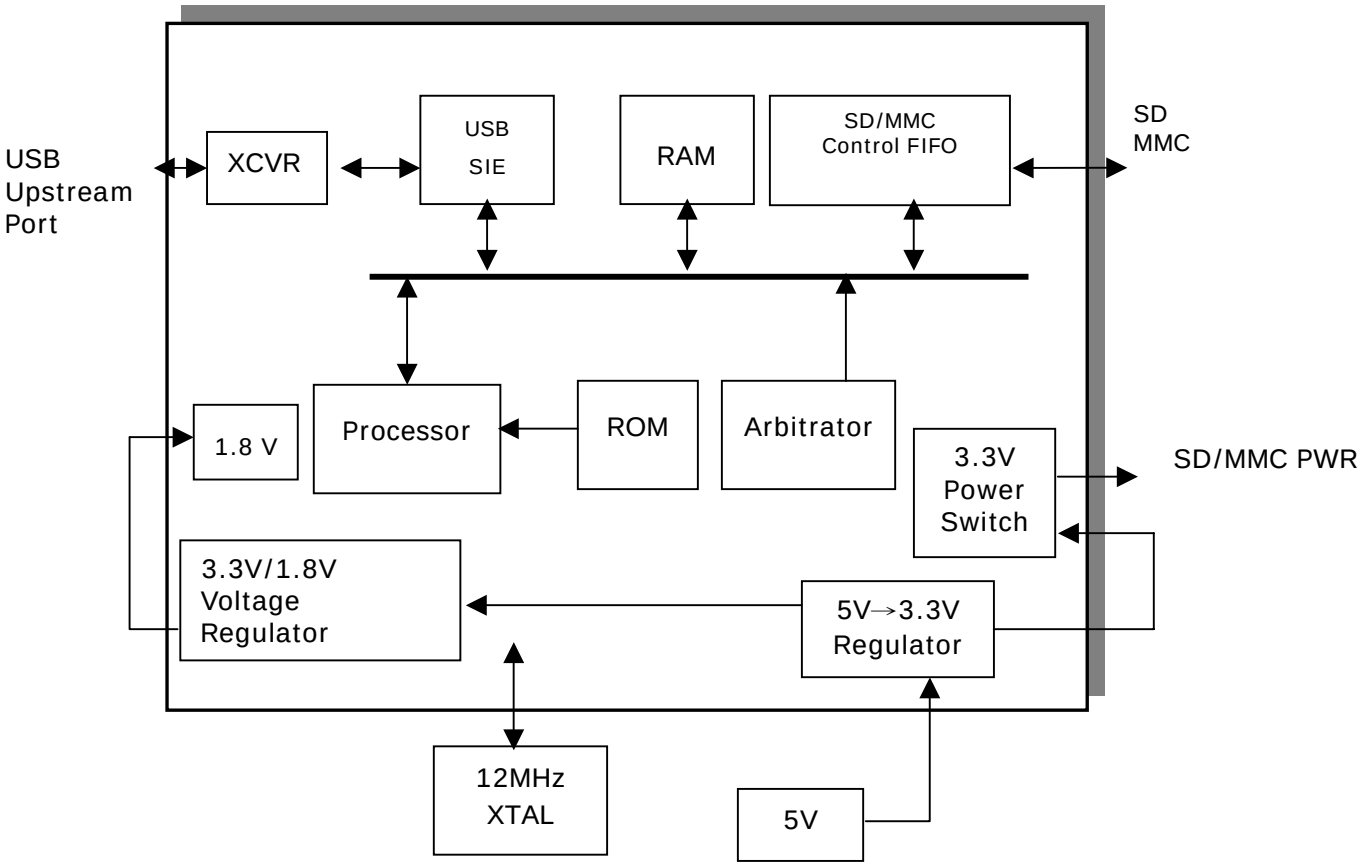
Table 3.2 AU6336-MDF Pin Descriptions

Pin #	Pin Name	I/O	Description
1	VD33P	I	UTMI 3.3V power input
2	DP	I/O	USB DP
3	DM	I/O	USB DM
4	VS33P	I	UTMI 3.3V ground
5	XI	I	12MHz crystal input
6	XO	O	12MHz crystal output
7	VDDU	I	UTMI 1.8V input
8	AVDD5V	I	5 to 3.3 regulator 5V input
9	VDD3V	O	5V to 3.3V regulator 3.3V output 3.3V to 1.8V regulator 3.3V input
10	V18	O	3.3V to 1.8V regulator 1.8V output
11	VDDHM	I	IO 3.3V power / 3.3 to 1.8 regulator 3.3V input
12	SDCDN	I	SD card detect
13	VDD33C	I	Card power switch 3.3V input
14	SD_V33	O	Card power switch output
15	SDCMD	I/O	SD command
16	SDDATA1	I/O	SD data 1
17	SDWP	I	SD write protect
18	SDDATA2	I/O	SD data 2
19	CLED	O	Card access LED. Low for card present High for card absent Blink for card access
20	SDDATA3	I/O	SD data 3
21	SDDATA0	I/O	SD data 0
22	SDCLK	O	SD clock
23	VDD	I	Core 1.8V power input
24	REXT	I	UTMI reference resistor

4. System Architecture and Reference Design

4.1 AU6336 Block Diagram

Figure 4.1 AU6336 Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{DDHM}	Power Supply	-0.3 to V_{DDH} +0.3	V
V_{IN}	Input Signal Voltage	-0.3 to 3.6	V
V_{OUT}	Output Signal Voltage	-0.3 to V_{DDHM} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{DDHM}	Power Supply	3.0	3.3	3.6	V
V_{18}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		85	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDHM}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{DDHM} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD33	Analog supply Voltage		3.0	3.3	3.6	V
V18	Digital supply Voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			55	mA

Table 5.6 Static characteristic：Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VDDH-0.2			V

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω

		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS/LS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
Low-Speed Mode						
t_{LR}	Rise time	CL=200pF-600pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$；	75		300	ns

t_{LF}	Fall time	CL=200pF-600pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$ ；	75		300	ns
t_{LRMA}	Differential rise/fall time matching（t_{LR} / t_{LF}）	Excluding the first transition from idle mode	80		125	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V
V_{OH}	High-level output voltage		2.8		3.6	V

5.6 Power Switch Feature

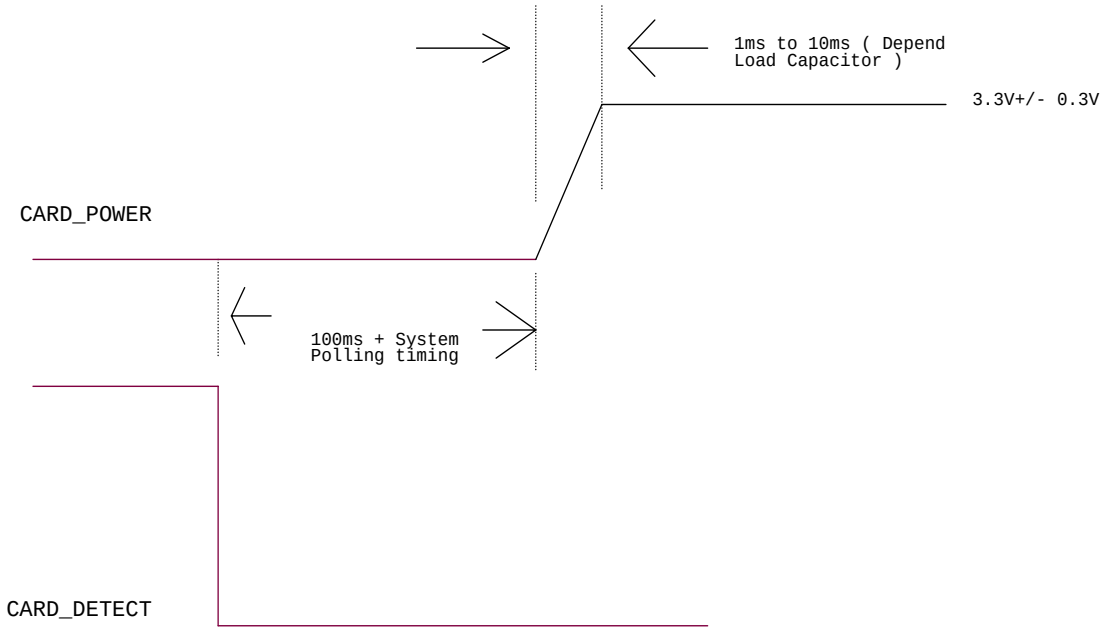


Figure 5.1 Card Detect Power-in Timing

6. Mechanical Information

Figure 6.1 28 SSOP Mechanical Information Diagram

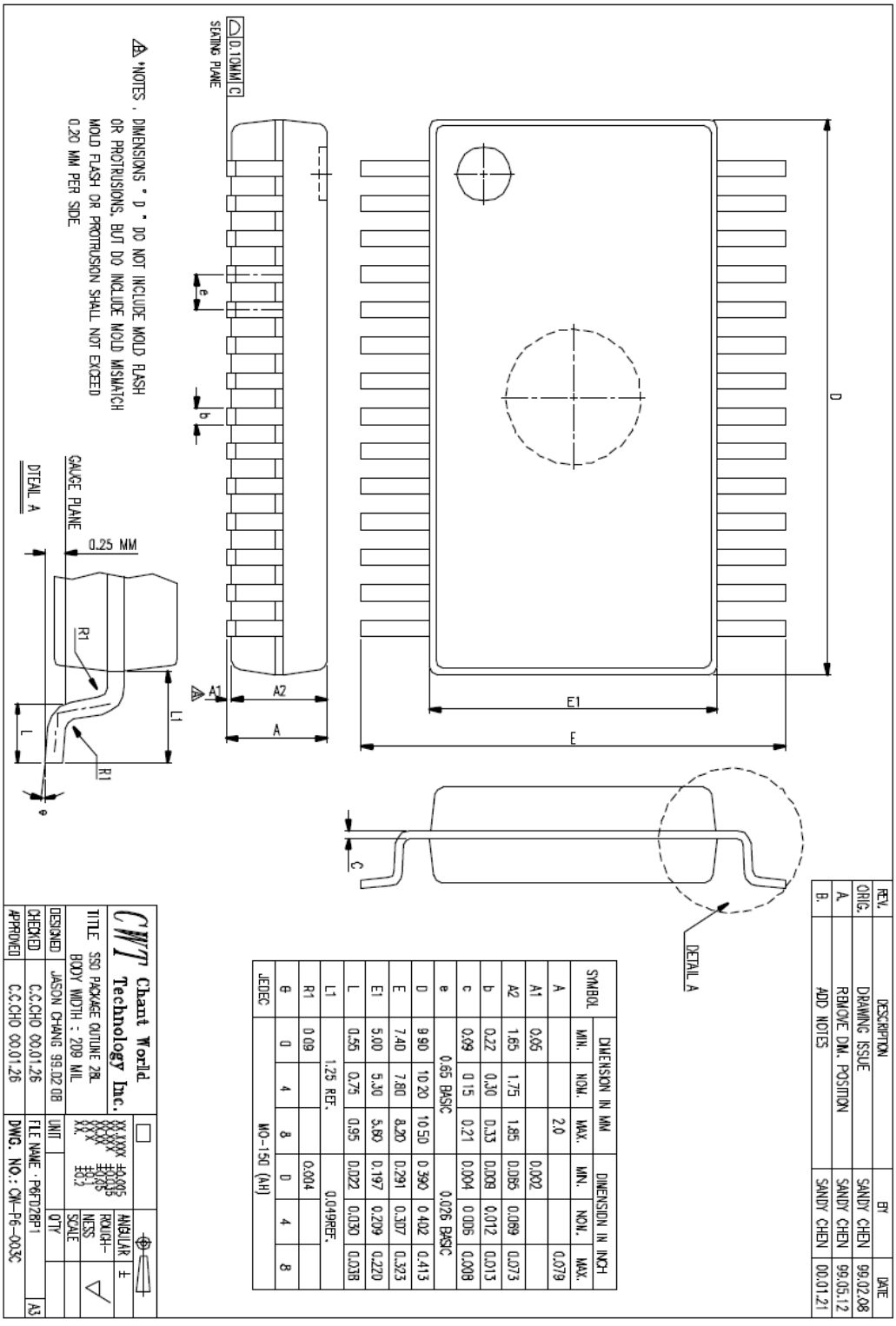
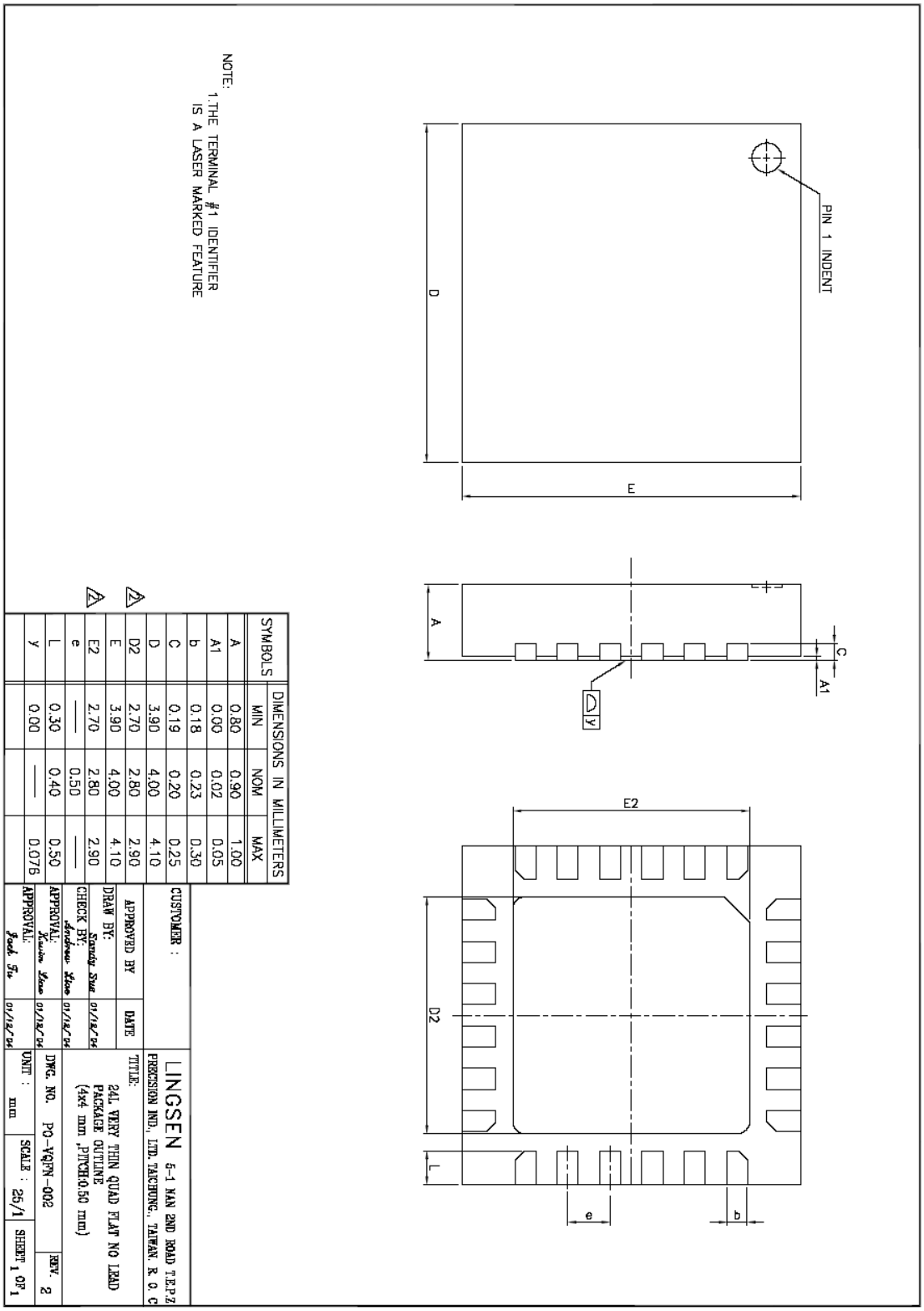


Figure 6.2 24 QFN Mechanical Information Diagram



7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
SD	Secure Digital
MMC	Multimedia Card
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.