

### POWER MANAGEMENT

#### Description

The SC1457 is a low dropout linear regulator that operates from a +2.25V to +6.5V input range and delivers up to 150mA. A PMOS pass transistor allows the low 75 $\mu$ A supply current to remain independent of load, making these devices ideal for battery operated portable equipment such as cellular phones, cordless phones and personal digital assistants.

The SC1457 has very low dropout voltage (typically 1.1mV at light loads and 150mV at 150mA) with better than 1.5% initial output voltage accuracy. It has a logic compatible enable control input and an internal output undervoltage monitor.

Designed especially for hand held, battery powered devices, the SC1457 can be switched by a CMOS or TTL compatible logic signal. When disabled, power consumption drops nearly to zero. Other features include short circuit protection, thermal shutdown protection and reverse battery protection.

The SC1457 is available in several fixed voltages in the tiny 5 lead SOT-23 package and the ultra low profile 5 lead TSOT-23.

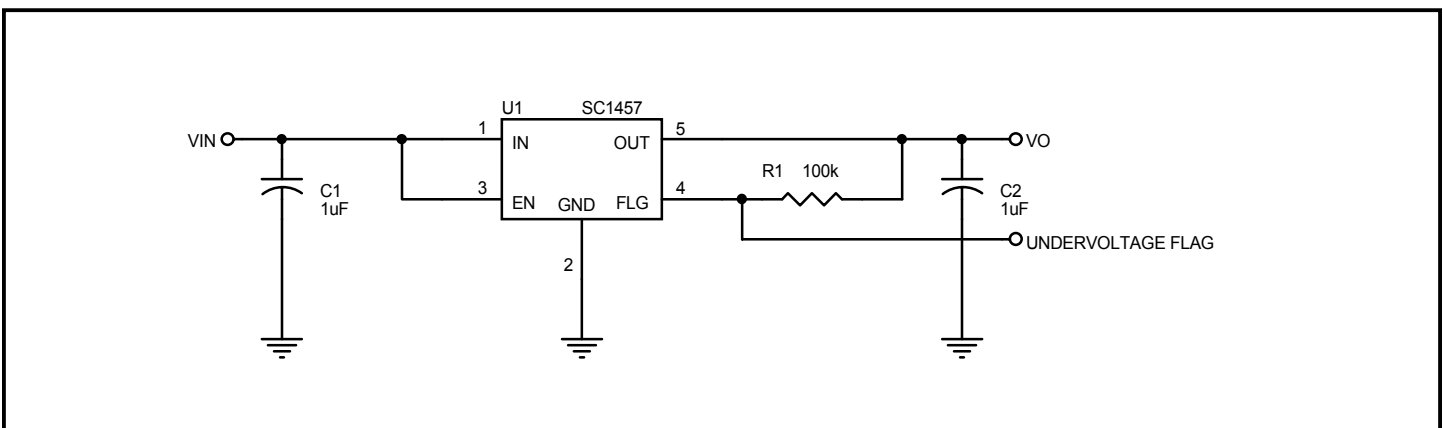
#### Features

- ◆ Guaranteed 150mA output current
- ◆ Error flag indicates output undervoltage fault
- ◆ 2% output accuracy guaranteed over line, load and temperature
- ◆ Very small external components - designed to work with ceramic capacitors
- ◆ Low 110 $\mu$ V<sub>RMS</sub> output noise
- ◆ Very low supply current
- ◆ Thermal overload protection
- ◆ Reverse battery protection
- ◆ Low power shutdown
- ◆ Full industrial temperature range
- ◆ Very low profile packaging available (1mm max. height)
- ◆ Surface mount packaging (SOT-23-5 and TSOT-23-5)

#### Applications

- ◆ Battery Powered Systems
- ◆ Cellular Telephones
- ◆ Cordless Telephones
- ◆ Personal Digital Assistants
- ◆ Portable Instrumentation
- ◆ Modems
- ◆ PCMCIA cards

#### Typical Application Circuit



**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	$V_{IN}$	-0.6 to +7	V
I/O Pin Voltages	$V_{EN}, V_{FLG}$	-0.6 to $V_{IN}$	V
Thermal Resistance Junction to Ambient	$\theta_{JA}$	256	°C/W
Thermal Resistance Junction to Case	$\theta_{JC}$	81	°C/W
Operating Ambient Temperature Range	$T_A$	-40 to +85	°C
Operating Junction Temperature Range	$T_J$	-40 to +125	°C
Storage Temperature Range	$T_{STG}$	-60 to +150	°C
Lead Temperature (Soldering) 10 seconds	$T_{LEAD}$	300	°C
ESD Rating (Human Body Model)	$V_{ESD}$	2	kV

**Electrical Characteristics**

Unless specified:  $V_{IN} = V_{OUT} + 1V$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 100\mu A$ ,  $T_A = 25^\circ C$ . Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>IN</b>						
Supply Voltage Range	$V_{IN}$		<b>2.25</b>		<b>6.50</b>	V
Supply Current	$I_Q$	$I_{OUT} = 0mA \text{ to } 150mA$		75	130	$\mu A$
					<b>160</b>	
		$V_{IN} = 6.5V, V_{EN} = 0V$		0.1	1.0	$\mu A$
					<b>1.5</b>	
<b>OUT</b>						
Output Voltage <sup>(1)</sup>	$V_{OUT}$	$I_{OUT} = 1mA$ $0mA \leq I_{OUT} \leq 150mA, V_{OUT} + 1V \leq V_{IN} \leq 5.5V$	-1.5%	$V_{OUT}$	+1.5%	V
			<b>-2.0%</b>		<b>+2.0%</b>	
Line Regulation <sup>(1)(2)</sup>	$REG_{(LINE)}$	$(V_{OUT(NOM)} + 0.1V) \leq V_{IN} \leq 5.5V, I_{OUT} = 1mA$		2.5	10	mV
					<b>12</b>	
Load Regulation <sup>(1)</sup>	$REG_{(LOAD)}$	$I_{OUT} = 0.1mA \text{ to } 150mA$		-3	-10	mV
					<b>-20</b>	

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

 Unless specified:  $V_{IN} = V_{OUT} + 1V$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 100\mu A$ ,  $T_A = 25^\circ C$ . Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Out (Cont.)</b>						
Current Limit	$I_{LIM}$		<b>400</b>			mA
Dropout Voltage <sup>(1)(3)</sup>	$V_D$	$I_{OUT} = 1mA$		1		mV
		$I_{OUT} = 50mA$		50	65	mV
					<b>75</b>	
		$I_{OUT} = 100mA$			100	125
				<b>155</b>		
		$I_{OUT} = 150mA$		150	190	mV
					<b>230</b>	
Output Voltage Noise	$e_n$	10Hz to 100kHz, $I_{OUT} = 50mA$ , $C_{OUT} = 1\mu F$		135		$\mu V_{RMS}$
		10Hz to 100kHz, $I_{OUT} = 50mA$ , $C_{OUT} = 100\mu F$		110		
Power Supply Rejection Ratio	PSRR	$f = 120Hz$		60		dB
<b>EN</b>						
Enable Input Threshold	$V_{IH}$	$2.25V \leq V_{IN} \leq 6.5V$	<b>1.6</b>			V
	$V_{IL}$	$2.25V \leq V_{IN} \leq 6.5V$			<b>0.4</b>	
Enable Input Bias Current <sup>(4)</sup>	$I_{EN}$	$0V \leq V_{EN} \leq V_{IN}$	<b>-0.5</b>	0	<b>+0.5</b>	$\mu A$
<b>FLG</b>						
Flag Threshold	$V_{TH(FLG)}$	Under voltage condition (below nominal)	-4	-6	-8	%
			<b>-4</b>		<b>-12</b>	
Output Logic Low Voltage	$V_{FLG}$	$I_{FLG} = 1mA$ , undervoltage condition			<b>0.4</b>	V
Flag Leakage Current	$I_{FLG}$	Flag OFF, $V_{FLG} = 0V$ to 6.5V	<b>-1</b>	0.1	<b>+1</b>	$\mu A$
<b>Over Temperature Protection</b>						
High Trip Level	$T_{HI}$			150		$^\circ C$
Hysteresis	$T_{HYST}$			20		$^\circ C$

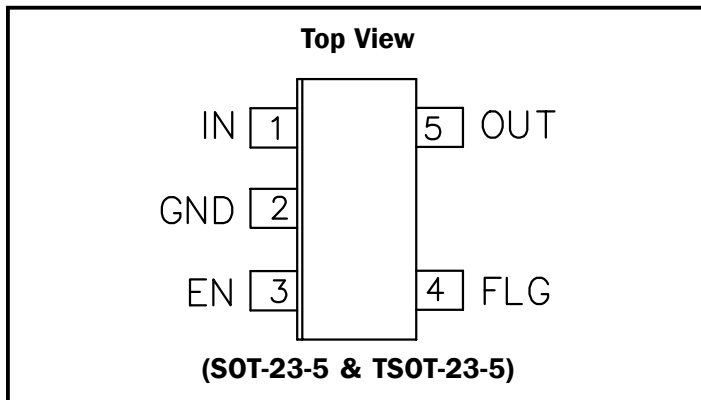
**NOTES:**

(1) Low duty cycle pulse testing with Kelvin connections required.

 (2)  $V_{IN(MIN)} = 2.25V$ .

 (3) Defined as the input to output differential at which the output voltage drops 100mV below the value measured at a differential of 1V. Not measurable on 1.5V and 1.8V parts due to minimum  $V_{IN}$  constraints.

(4) Guaranteed by design.

**POWER MANAGEMENT**
**Pin Configuration**

**Ordering Information**

Part Number	Package
SC1457ISK-X.XTR <sup>(1)</sup>	SOT-23-5 <sup>(2)</sup>
SC1457ISKX.XTRT <sup>(1)(4)</sup>	
SC1457ITSK-XXTR <sup>(1)</sup>	TSOT-23-5 <sup>(2)</sup>
SC1457ITSKXXTRT <sup>(1)(4)</sup>	
SC1457EVB <sup>(3)</sup>	N/A

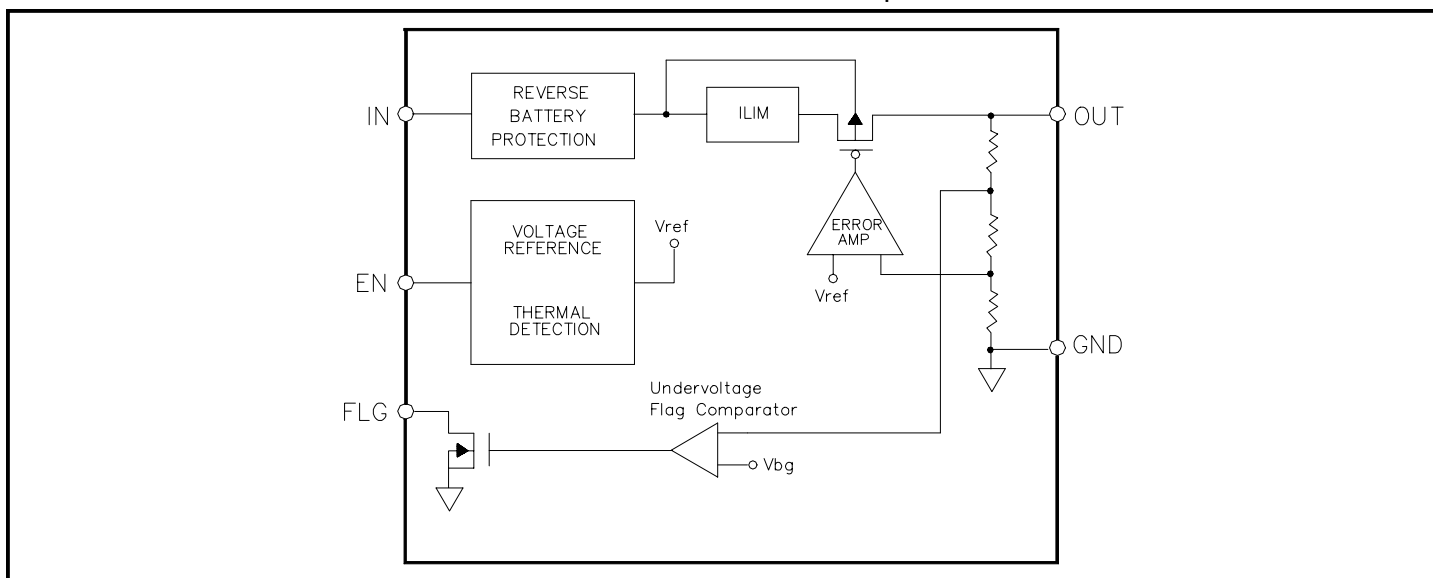
**Notes:**

(1) Where X.X or XX denotes voltage options. Available voltages are: 1.5V (1.5 or 15), 1.8V (1.8 or 18), 2.5V (2.5 or 25), 2.7V (2.7 or 27), 2.8V (2.8 or 28), 2.9V (2.9 or 29), 3.0V (3.0 or 30), 3.1V (3.1 or 31), 3.2V (3.2 or 32) and 3.3V (3.3 or 33).

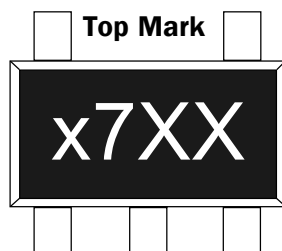
(2) Only available in tape and reel packaging. A reel contains 3000 devices.

(3) Evaluation board for SC1457. Specify output voltage option when ordering.

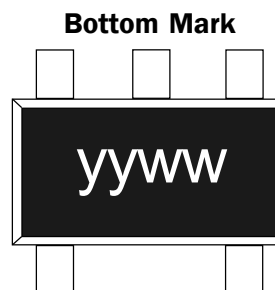
(4) Lead free product. This product is fully WEEE and RoHS compliant.

**Block Diagram**

**Pin Descriptions**

Pin	Pin Name	Pin Function
1	IN	Input pin
2	GND	Ground pin. Can be used for heatsinking if needed.
3	EN	Active high enable pin. Connect $V_{IN}$ if not being used.
4	FLG	Error Flag. Open drain output. Active low indicates an output undervoltage condition.
5	OUT	Regulator output sourcing up to 150mA.

**POWER MANAGEMENT**
**Marking Information**


x = package (5 for SOT-23-5, T for TSOT-23-5)  
 7 = SC1457  
 XX = voltage option  
 (examples: 5731 for 3.1V option in SOT-23-5,  
 T728 for 2.8V option in TSOT-23-5)



yyww = Date code  
 (example: 0008 for week 8 of 2000)

**Applications Information**
**Theory Of Operation**

The SC1457 is intended for applications where very low dropout voltage, low supply current and output voltage monitoring are critical. It provides a very simple, low cost solution that uses very little pcb real estate. Only two external capacitors and one resistor are required for operation.

The SC1457 contains a bandgap reference trimmed for optimal temperature coefficient which is fed into the inverting input of an error amplifier. The output voltage of the regulator is divided down internally using a resistor divider and compared to the bandgap voltage. The error amplifier drives the gate of a low  $R_{DS(ON)}$  P-channel MOSFET pass device.

An active high enable pin (EN) allows the regulator to be shut down. Pulling this pin low causes the device to enter a very low power shutdown mode, where it will draw typically 0.1 $\mu$ A from the input supply.

An open drain flag pin (FLG) is provided to signal whenever the output voltage is 6% (typically) below nominal. A tap is taken from the internal resistor divider and compared to the bandgap voltage to determine if the output voltage is above or below this level. The flag pin pulls low whenever the output is out of specification. An external pullup resistor is required for a high signal when the flag pin is not pulling low. Since this circuitry is powered from the input supply, the FLG pin will pull low for output voltages all the way down to zero, unlike external devices powered from the LDO output.

The regulator has its own current limit circuitry to ensure that the output current will not damage the device during output short, overload or start-up. The current limit is guaranteed to be greater than 400mA to allow fast charging of the output capacitor and high initial currents for DSP initialization.

The SC1457 includes thermal shutdown circuitry to turn off the device if  $T_J$  exceeds 150°C (typical), with the device remaining off until  $T_J$  drops by 20°C (typical). Reverse battery protection circuitry ensures that the device cannot be damaged if the input supply is accidentally reversed, limiting the reverse current to less than 1.5mA.

**Component Selection - General**

**Output capacitor** - Semtech recommends a minimum capacitance of 1 $\mu$ F at the output with an equivalent series resistance (ESR) of < 1 $\Omega$  over temperature. While the SC1457 has been designed to be used with ceramic capacitors, it does not have to be used with ceramic capacitors, allowing the designer a choice. Increasing the bulk capacitance will further reduce output noise and improve the overall transient response.

**Input capacitor** - Semtech recommends the use of a 1 $\mu$ F ceramic capacitor at the input. This allows for the device being some distance from any bulk capacitance on the rail. Additionally, input droop due to load transients is reduced, improving overall load transient response.

**Flag pullup resistor** - Semtech recommends a maximum value of 100k $\Omega$  for this resistor to ensure that this pin is high even under worst-case flag pin leakage conditions of 1 $\mu$ A when off.

**POWER MANAGEMENT**
**Applications Information (Cont.)**
**Thermal Considerations**

The worst-case power dissipation for this part is given by:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \cdot I_{OUT(MAX)} + V_{IN(MAX)} \cdot I_{Q(MAX)} \quad (1)$$

For all practical purposes, equation (1) can be reduced to the following expression:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \cdot I_{OUT(MAX)} \quad (2)$$

Looking at a typical application, 3.3V to 2.8V at 150mA:

$$\begin{aligned} V_{IN(MAX)} &= 3.3 + 5\% = 3.465V \\ V_{OUT(MIN)} &= 2.8V - 2\% = 2.744V \\ I_{OUT} &= 150mA \\ T_A &= 85^\circ C \end{aligned}$$

Inserting these values into equation (2) gives us:

$$P_{D(MAX)} = (3.465 - 2.744) \cdot 0.150 = 108mW$$

Using this figure, we can calculate the maximum thermal impedance allowable to maintain  $T_J \leq 125^\circ C$ :

$$\theta_{JA(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{P_{D(MAX)}} = \frac{(125 - 85)}{0.108} = 370^\circ C/W$$

With the standard SOT-23-5/TSOT-23-5 Land Pattern shown at the end of this datasheet, and minimum trace widths, the thermal impedance junction to ambient for SC1457ISK is  $256^\circ C/W$ . Thus no additional heatsinking is required for this example.

The junction temperature can be reduced further (or higher power dissipation can be allowed) by the use of larger trace widths and connecting PCB copper to the GND pin (pin 2), which connects directly to the device substrate. Adding approximately one square inch of PCB copper to pin 2 will reduce  $\theta_{JA}$  to approximately  $130^\circ C/W$  and  $T_{J(MAX)}$  for the example above to approximately  $100^\circ C$  for the SOT-23-5 package. The use of multi layer boards with internal ground/power planes will lower the junction temperature and improve overall output voltage accuracy.

**Layout Considerations**

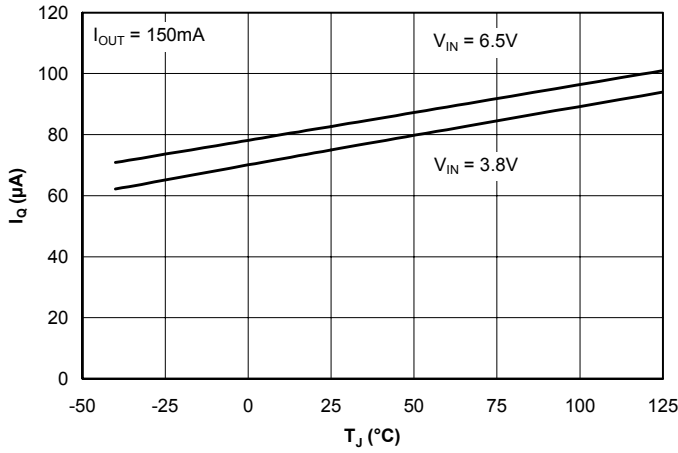
While layout for linear devices is generally not as critical as for a switching application, careful attention to detail will ensure reliable operation.

- 1) Attaching the part to a larger copper footprint will enable better heat transfer from the device, especially on PCBs where there are internal ground and power planes.
- 2) Place the input, output and bypass capacitors close to the device for optimal transient response and device behaviour.
- 3) Connect all ground connections directly to the ground plane. If there is no ground plane, connect to a common local ground point before connecting to board ground.

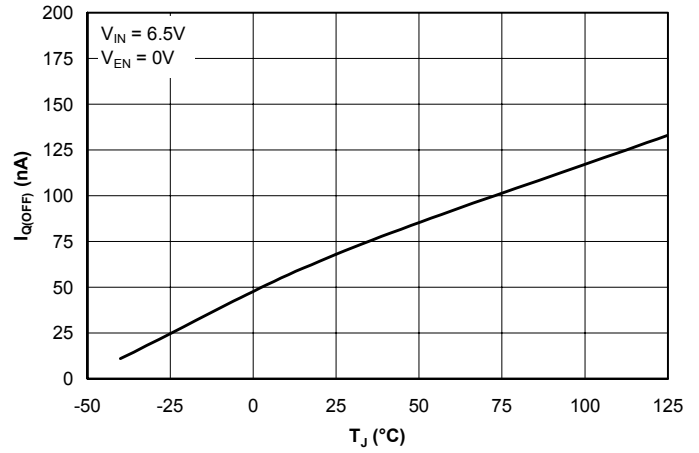
**POWER MANAGEMENT**

**Typical Characteristics**

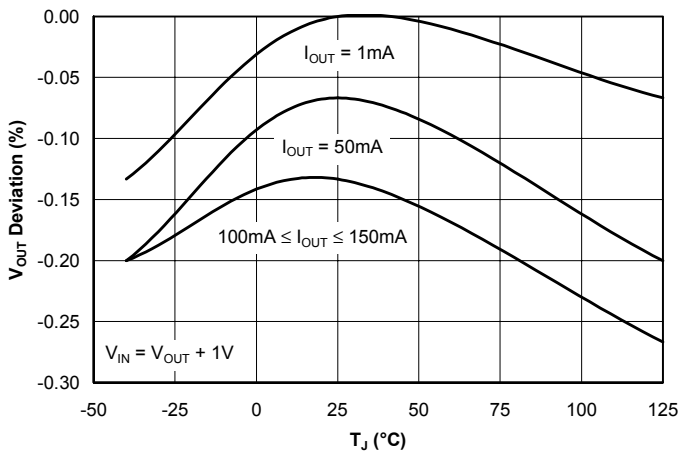
**Quiescent Current vs. Junction Temperature vs. Input Voltage**



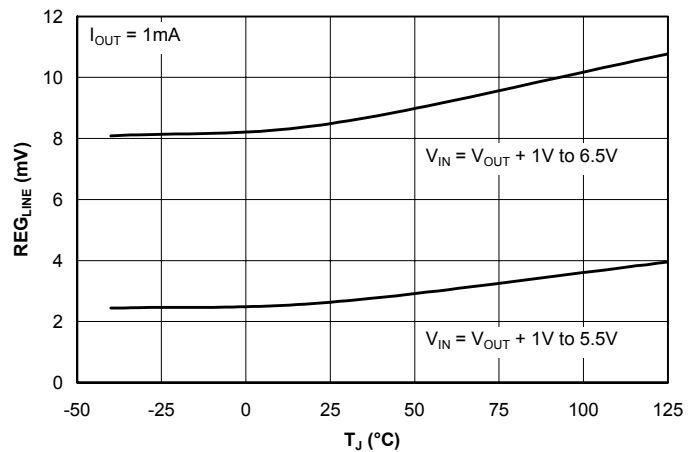
**Off-State Quiescent Current vs. Junction Temperature**



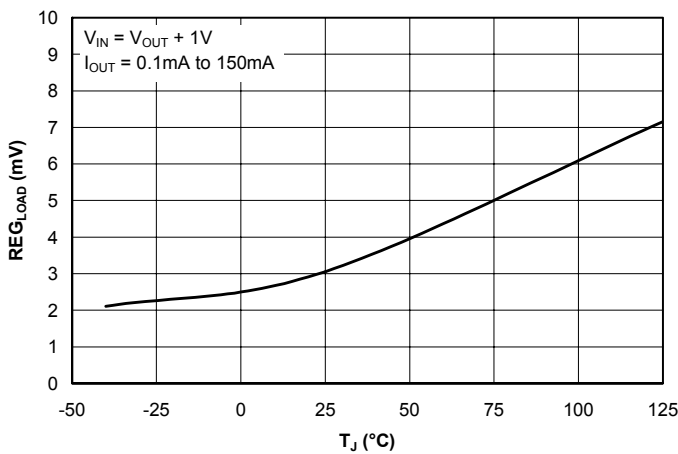
**Output Voltage vs. Junction Temperature vs. Output Current**



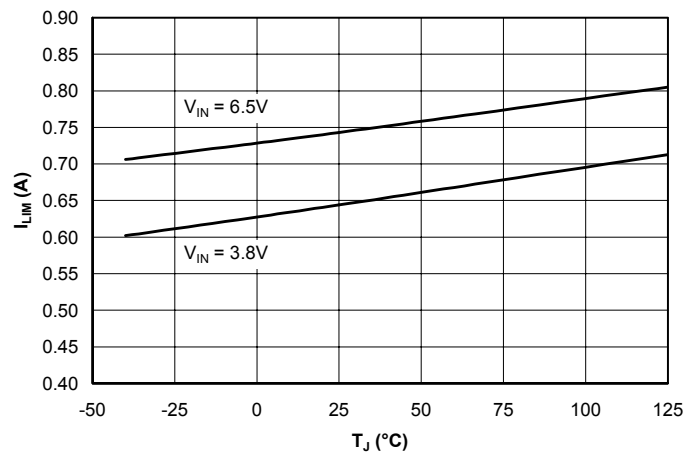
**Line Regulation vs. Junction Temperature vs. Input Voltage Change**



**Load Regulation vs. Junction Temperature**



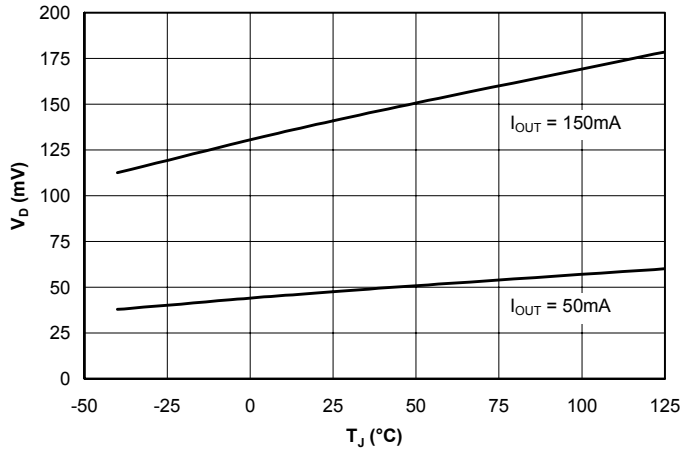
**Current Limit vs. Junction Temperature vs. Input Voltage**



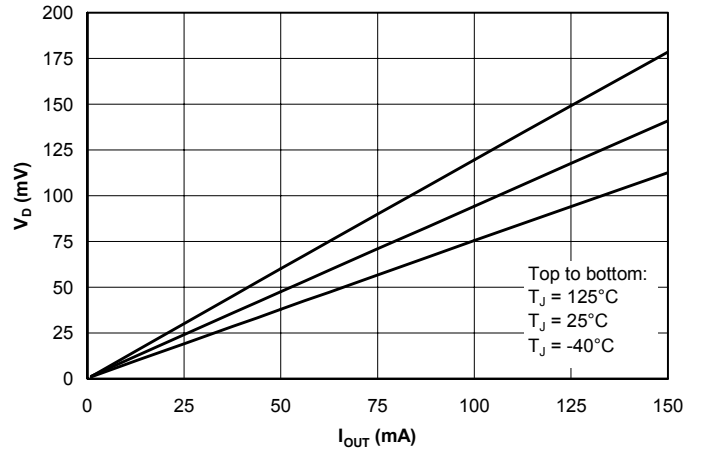
**POWER MANAGEMENT**

**Typical Characteristics (Cont.)**

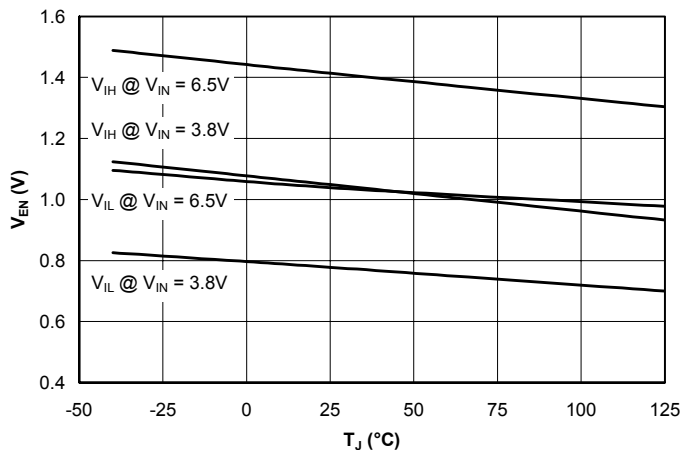
**Dropout Voltage vs. Junction Temperature vs. Output Current**



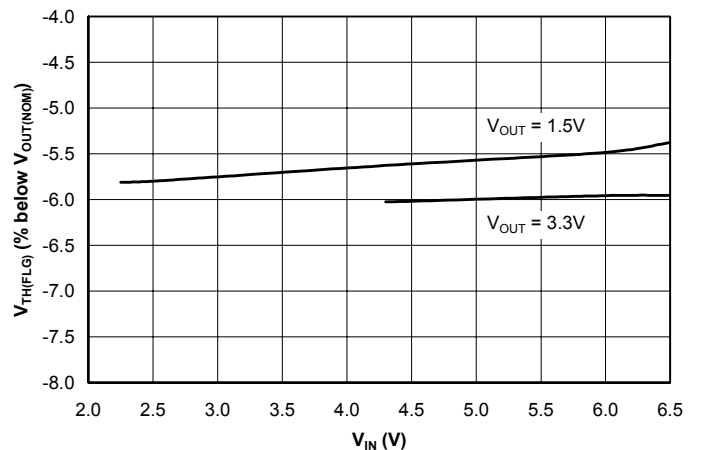
**Dropout Voltage vs. Output Current vs. Junction Temperature**



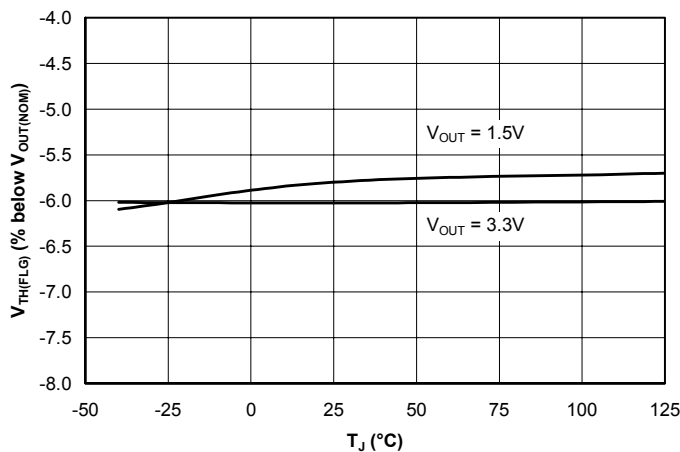
**Enable Input Threshold Voltage vs. Junction Temperature vs. Input Voltage**



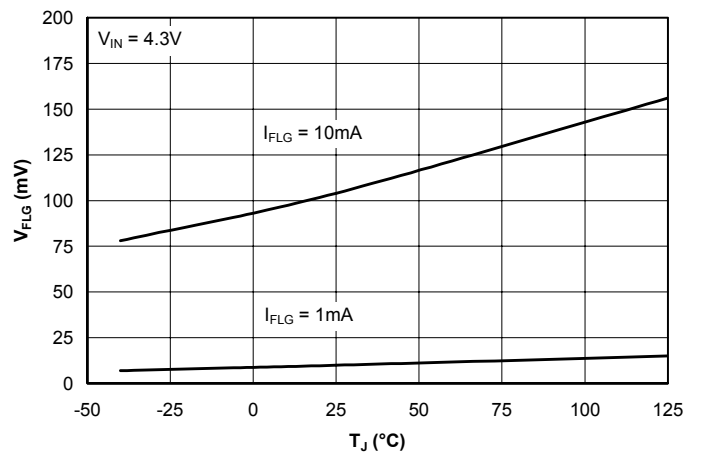
**Flag Threshold Voltage vs. Input Voltage vs. Output Voltage**



**Flag Threshold Voltage vs. Junction Temperature vs. Output Voltage**



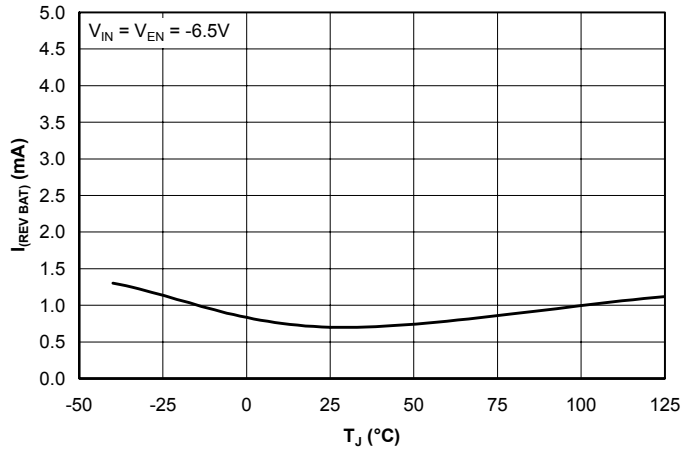
**Flag Voltage vs. Junction Temperature vs. Flag Current**





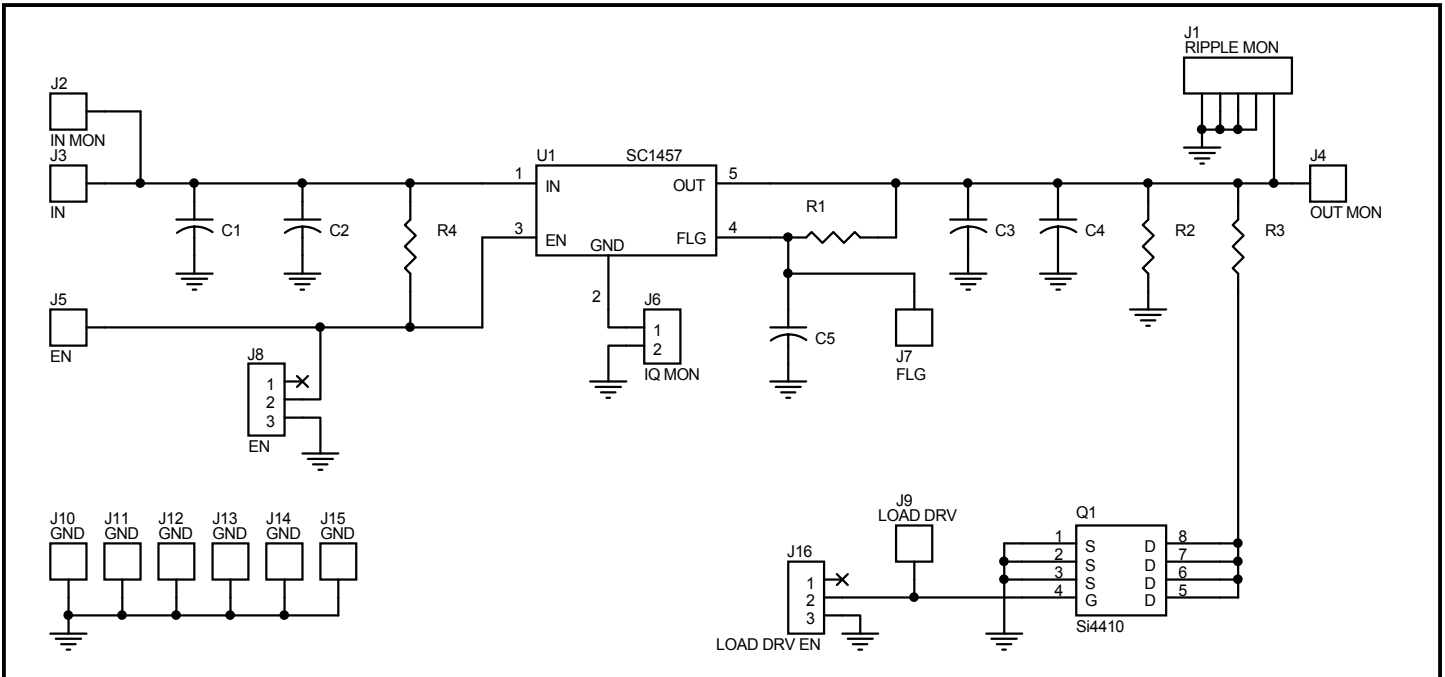
## POWER MANAGEMENT

## Typical Characteristics (Cont.)

**Reverse Battery Protection vs.  
Junction Temperature**

**POWER MANAGEMENT**

**Evaluation Board Schematic**

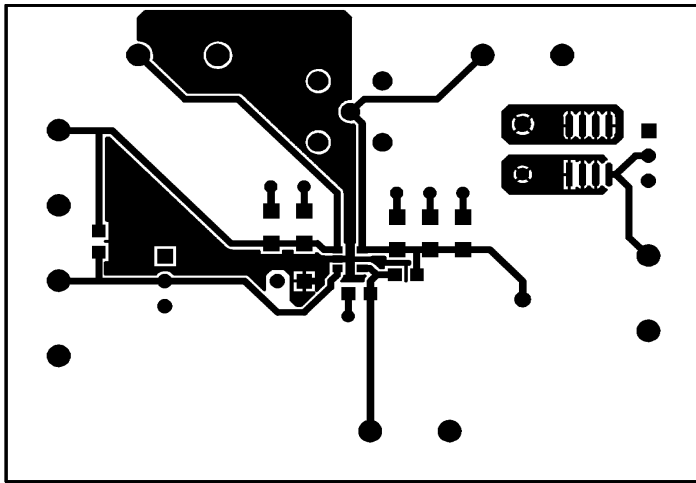


**Evaluation Board Bill of Materials**

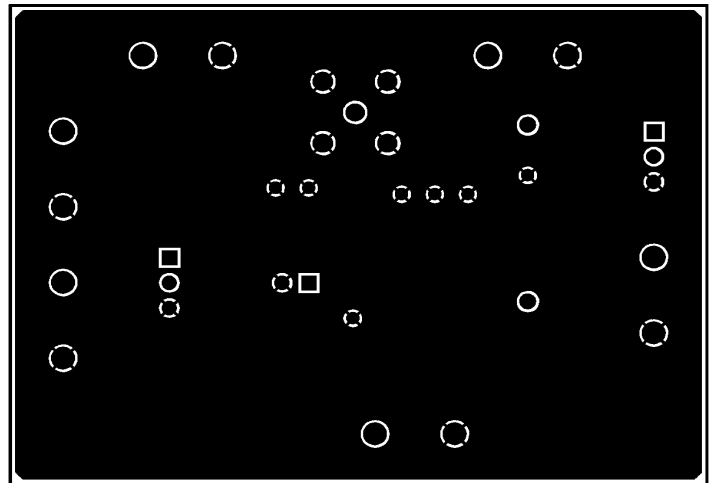
Quantity	Reference	Part/Description	Vendor	Notes
3	C1, C4, C5	Not placed		
2	C2, C3	1µF ceramic	Murata	GRM42-6X7R105K10
1	J1	BNC socket	Various	V <sub>OUT</sub> ripple monitor
3	J2 - J4	Test pin	Various	Red
1	J5	Test pin	Various	White
1	J6	Header, 2 pin	Various	
1	J7	Test pin	Various	Yellow
2	J8, J16	Header, 3 pin	Various	
1	J9	Test pin	Various	Orange
6	J10 - J15	Test pin	Various	Black
1	Q1	Si4410	Vishay	
1	R1	100kΩ, 1/10W	Various	
1	R2	Not placed		
1	R3	See next page	Various	
1	R4	10kΩ, 1/10W	Various	
1	U1	<b>SC1457ISK-X.X or SC1457ITSK-XX</b>	Semtech	

**POWER MANAGEMENT**

**Evaluation Board Gerber Plots**

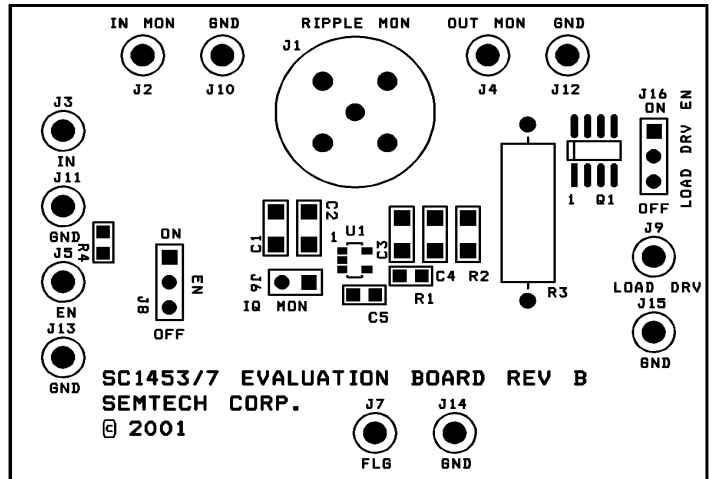


**Top Copper**



**Bottom Copper**

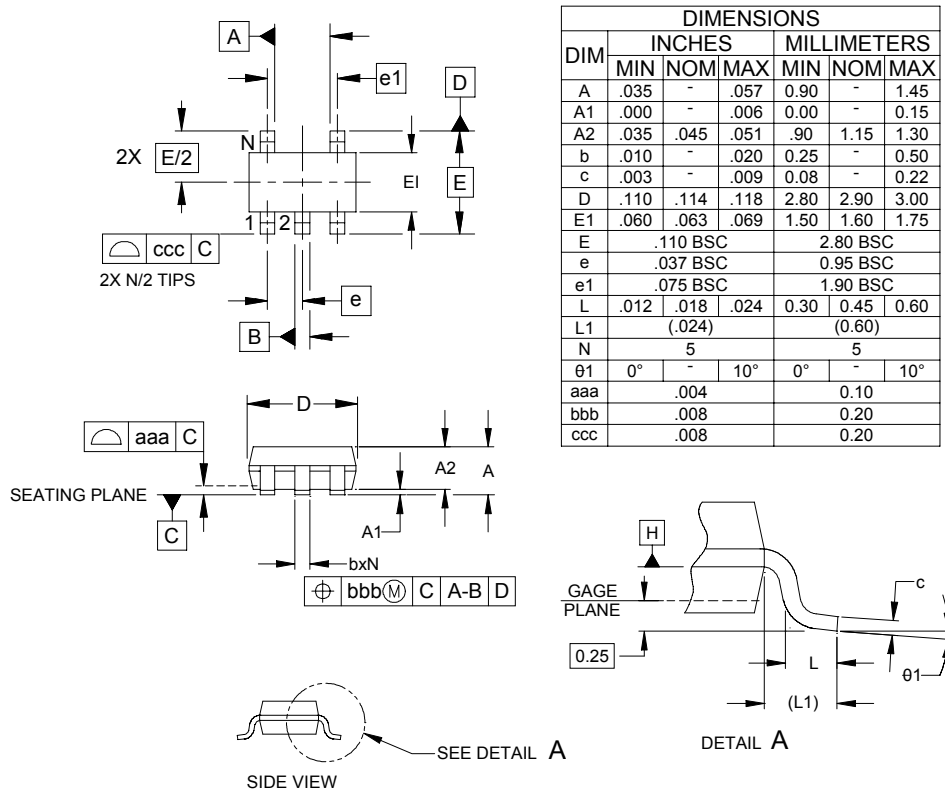
Output Voltage Option (V)	R3 Value/Size
1.5	10Ω/0.5W
1.8	12Ω/0.5W
2.5	16Ω/0.5W
2.7	18Ω/0.5W
2.8	18Ω/0.5W
2.9	18Ω/0.5W
3.0	20Ω/0.5W
3.1	20Ω/0.5W
3.2	22Ω/0.5W
3.3	22Ω/0.5W



**Top Silk Screen**

POWER MANAGEMENT

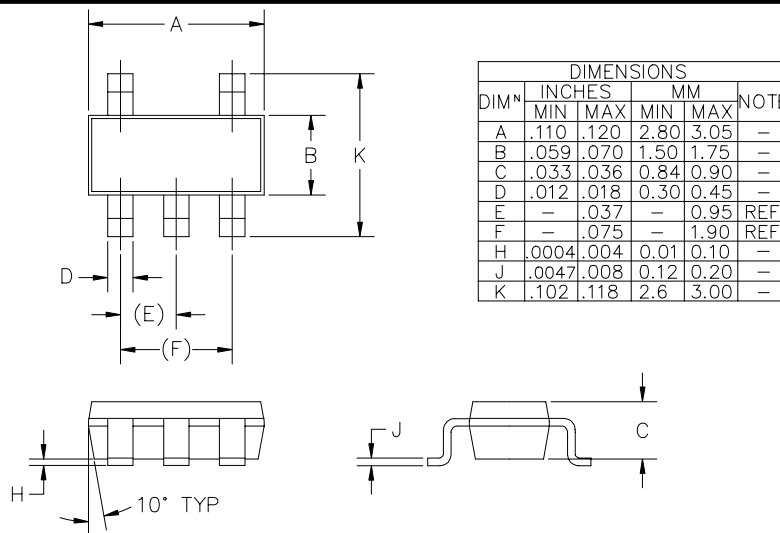
Outline Drawing - SOT-23-5



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

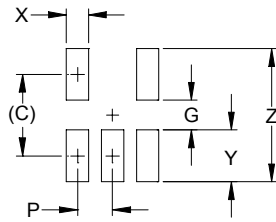
Outline Drawing - TSOT-23-5



- 2 PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
- 1 CONTROLLING DIMENSIONS: MILLIMETERS.

**POWER MANAGEMENT**

**Land Pattern - SOT-23-5 & TSOT-23-5**



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

**Contact Information**

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