AKD4121A
AK4121A Evaluation Board Rev.0

GENERAL DESCRIPTION

The AKD4121A is the evaluation board for the AK4121A, 96kHz asynchronous sample rate converter. This board has the optical connectors to interface with other digital audio equipments and serial interfaces for AKM AD/DA evaluation boards. The AKD4121A achieves quick evaluation of AK4121A

■ Ordering guide

AKD4121A --- Evaluation board for AK4121A

FUNCTION

- ☐ **Optical fiber connectors (for Digital Audio Interface. input x 1, output x 1.)**
- ☐ **10pin Header (for AKM AD/DA evaluation board. input x 1, output x 1.)**
- ☐ **On board X'tal Oscillator (input x 1, output x 1.)**

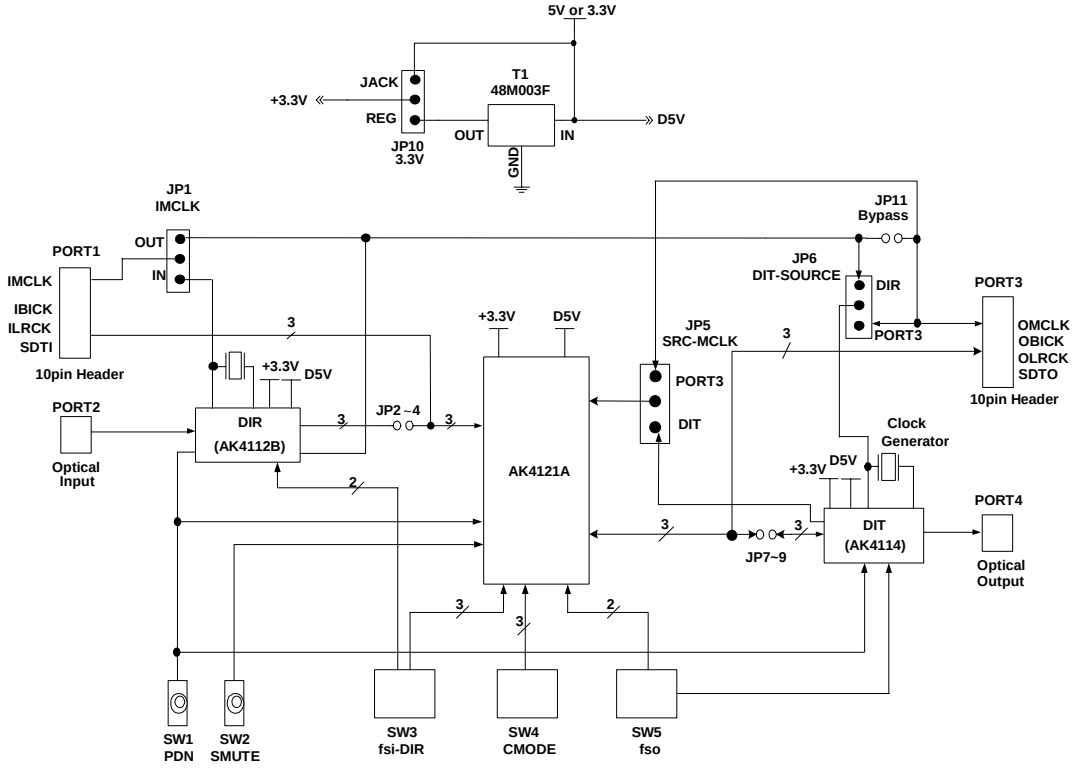

Figure 1. AKD4121A Block Diagram

*Circuit diagram and PCB layout are attached at the end of this manual.

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■ Operating Sequence

Please use the AKD4121A according to the following sequence.

1. Jumper Setting for Power Supply: JP10(3.3V)

The JP10 (3.3V) selects power supply of the AKD4121A.(3.3V or 5V.)

JACK : Providing power supply voltage with 3.3V. Opticlal input is not avaible.
REG : Providing power supply voltage with 5V. (3.3V is supplied via regulator on board.)

2. Power Supply Line Setting

Each supply line should be distributed directly from the power supply unit with low impedance connection.

5V or 3.3V : For power supply jack. 5V or 3.3V. (Power supply voltage is selectrd by JP10.)
GND : Groung of the board. 0V.

3. DIP Switch and Jumper Pins Setting (refer next page)

4. Power-on(After power is on, SW1 should be reset by setting "L"→"H" once.)

* The reset is done by SW1 during opertion.
The AK4121A is powered down during SW1 is “L”.The power down state is canceld by briging the SW1 to “H”, at the same time, the AK4121A is reset.

■ DIP switch and Jumper pin setting

1. Setting of fsi (input fs) block

1-1. Optical input(PORT2)

1-1-a. Jumper setting

Parts No.	Setting
JP1	(don't care)
JP2	SHORT
JP3	SHORT
JP4	SHORT
SW3-4	OFF
X1	(don't care)

Table 1. Jumper Setting (Refer following figures)

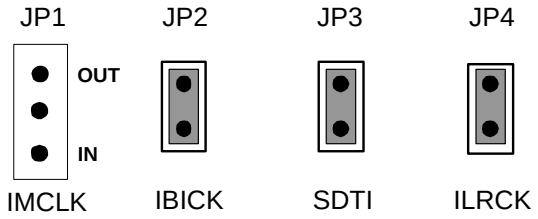


Figure 2. Jumper Setting

1-1-b. Audio Interface Format setting(IIS only)

Figure 3. DIP switch (SW3) setting

1-2. All clock are fed through the 10-pin port

1-2-a. Jumper setting

Parts No.	Setting
JP1	(don't care)
JP2	OPEN
JP3	OPEN
JP4	OPEN
SW3-4	(don't care)
X1	(don't care)

Table 2. Jumper Setting (Refer following figures)

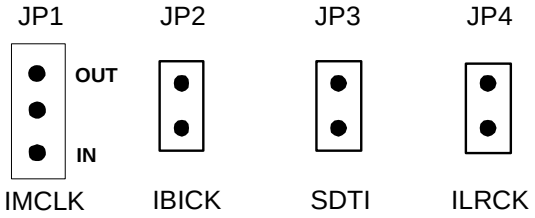
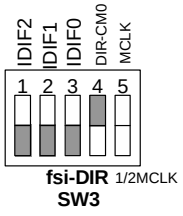


Figure 4. Jumper Setting

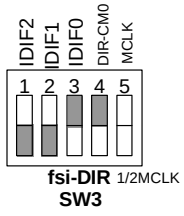
1-2-b. Audio Interface Format setting

Audio Interface Format	SRC:AK4121A		
	SW3-1	SW3-2	SW3-3
	DIF2	DIF1	DIF0
16bit, Right justified	0	0	0
20bit, Right justified	0	0	1
Left justified	0	1	0
I^2S	0	1	1
24bit, Right justified	1	0	0

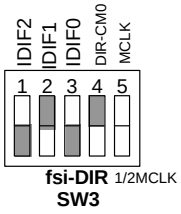
Table 3. DIP switch (SW3) setting(Refer following figures)



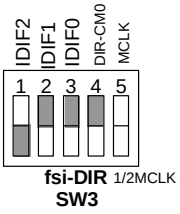
16bit, Right justified



20bit, Right justified



Left justified



I^2S

24bit, Right justified

Figure 5. DIP switch Setting

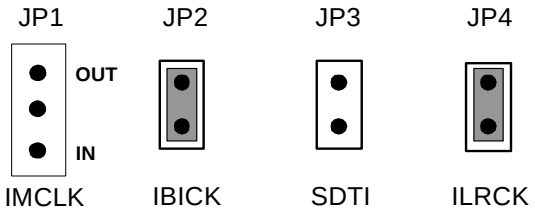
1-3. SDTI is fed through the 10-pin port and other clocks are fed from the AK4112B.

The X1(X'tal) or external clock (via PORT1) can be used as the system clock of the input block. Please remove X1 when unsed. The system clock can be selected as 256fsi or 512fsi. This clock is not used for the AK4121A directly.

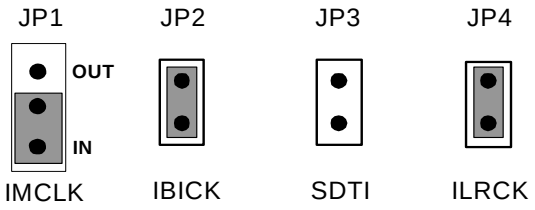
1-3-a. Jumper setting

Parts No.	Setting
JP1	OPEN: Using X'tal IN : System clock providing from 10port
JP2	SHORT
JP3	OPEN
JP4	SHORT

Table 4. DIP switch (SW3) setting(Refer following figures)



Using X'tal setting



Using external clock

Figure 6. Jumper Setting

No.	X'tal / External clock (Max: 24.576MHz)	DIP SW3 setting	
		DIR-CM0 SW3-4	OCKS0 SW3-5
1	256fs	ON	1/2 MCLK
2	512fs	ON	MCLK

Table 5. DIR(AK4112B)'s clock setting(Refer following figures)

Figure 7. DIP SW(SW3) setting(Refer following figures)

1-3-b Audio Interface Format setting

Refer "1-2-b Refer Audio Interface Format setting"

2. Setting of fso (output fs) block

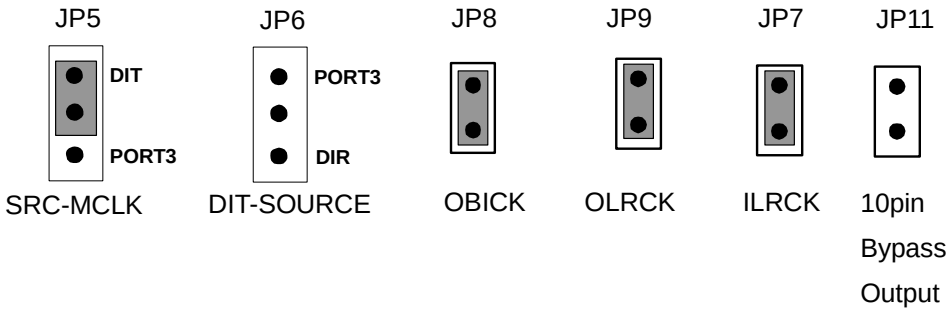
2-1. Optical Output(PORT4). Clocks are fed from AK4114 (DIT). (IIS Master Mode only.)

The X2(X'tal) or external clock via PORT3 can be used as the system clock of the output block. Please remove X2 when unused.

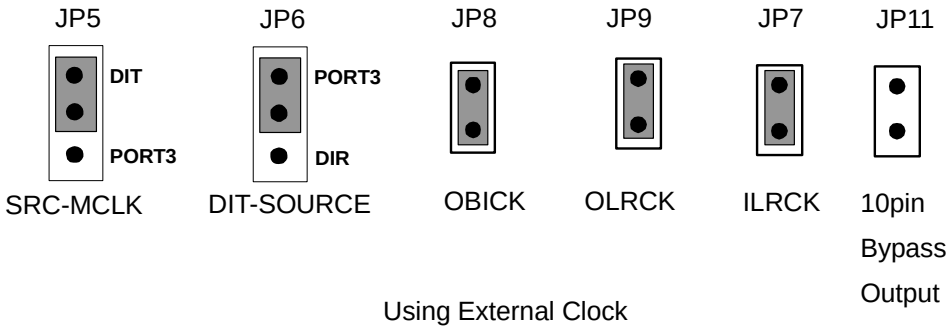
2-1-a. Jumper setting

Parts No.	Setting
JP5	DIT
JP6	OPEN: Using X'tal on board PORT3: Clock input form PORT3 (DIR: Using clock from DIR for Bypass Mode)
JP7	SHORT
JP8	SHORT
JP9	SHORT
JP11	OPEN

Table 6. Jumper setting(Refer following figures)



Using on-board X'tal



Using External Clock

Figure 8. Jumper setting

2-1-b. DIP SW setting

X2 or External Clock	SW4-1	SW4-2	SW4-3	SW5-3
	CMODE2	CMODE1	CMODE0	OCKS0
256fs	L	L	L	1/2 MCLK
512fs	L	H	L	MCLK

Table 7. Clock setting(Refer following figures)

Figure 9. DIP switch setting

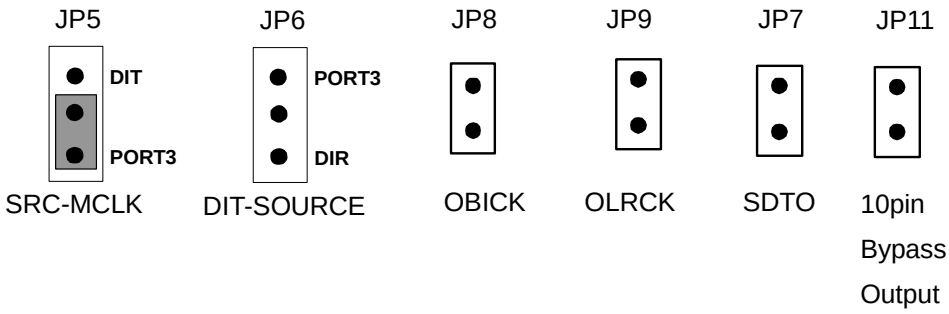
2-2. Clocks are fed through the 10-pin port(PORT3)

2-2-1. AK4121A in Master Mode

2-2-1-a. Jumper setting

Parts No.	Setting
JP5	PORT3
JP6	OPEN
JP8	OPEN
JP9	OPEN
JP7	OPEN
JP11	OPEN

Table 8. Jumper setting(Refer following figures)



Using X'tal on-board

Figure 10. Jumper setting

2-2-1-b. Audio Interface Format

Mode	SW4-1 CMODE2	SW4-2 CMODE1	SW4-3 CMODE0	MCLK	Master/Slave (Output Port)
0	L	L	L	256fso (fso~96kHz)	Master
1	L	L	H	384fso (fso~96kHz)	Master
2	L	H	L	512fso (fso~48kHz)	Master
3	L	H	H	768fso (fso~48kHz)	Master

Table 9. AK4121A System Clock setting

Mode	SW5-1 ODIF1	SW5-2 ODIF0	SDTO Format	OBICK (Slave)	OBICK (Master)
0	L	L	16bit LSB Justified	64fs	64fs
1	L	H	20bit LSB Justified	64fs	64fs
2	H	L	20bit MSB Justified	≥40fs	64fs
3	H	H	20bit I^2S Compatible	≥40fs or 32fs	64fs

Table 10. AK4121A Audio Interface Format setting

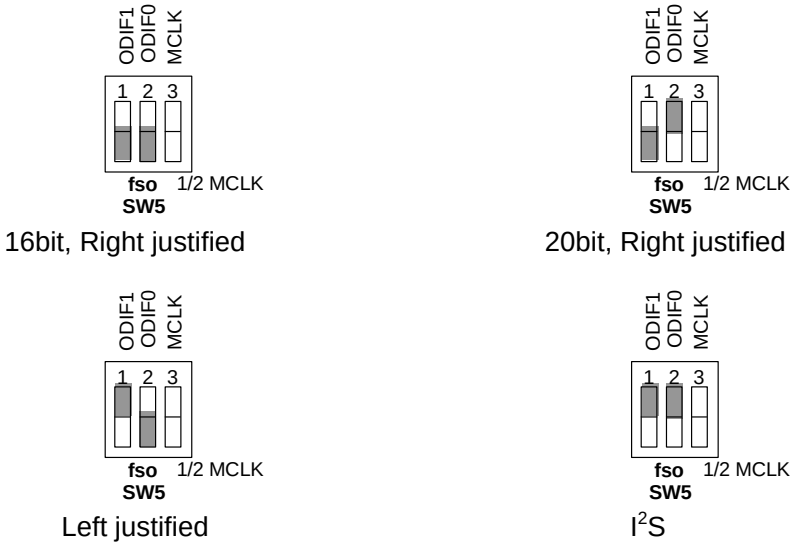


Figure 11. DIP switch setting

2-2-2. AK4121A in Slave Mode

2-2-2-a. Jumper setting

Parts No.	Setting
JP5	PORT3
JP6	OPEN
JP8	OPEN
JP9	OPEN
JP7	OPEN
JP11	OPEN

Table 11. Jumper setting(Refer following figures)

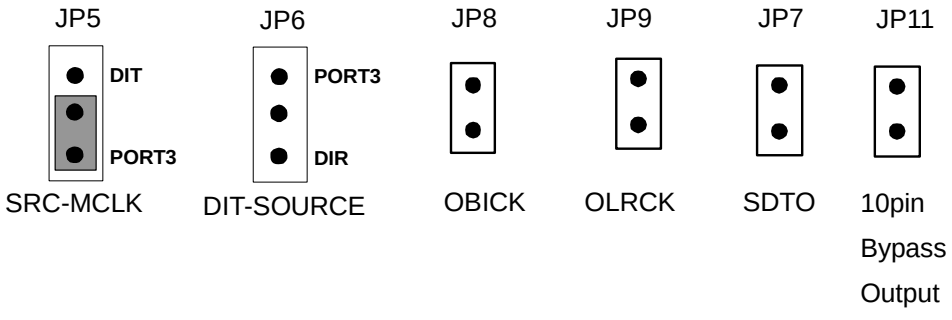


Figure 12. Jumper setting

2-2-2-b. Audio Interface Format

Mode	SW4-1 CMODE2	SW4-2 CMODE1	SW4-3 CMODE0	MCLK	Master/Slave (Output Port)
4	H	L	L	Not used. Set to DVSS	Slave

Table 12. AK4121A System Clock setting

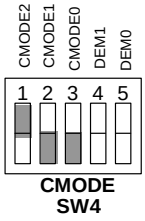


Figure 13. DIP switch setting

Mode	SW5-1 ODIF1	SW5-2 ODIF0	SDTO Format	OBICK (Slave)	OBICK (Master)
0	L	L	16bit LSB Justified	64fs	64fs
1	L	H	20bit LSB Justified	64fs	64fs
2	H	L	20bit MSB Justified	≥40fs	64fs
3	H	H	20bit I^2S Compatible	≥40fs or 32fs	64fs

Table 13. AK4121A Audio Interface Format setting

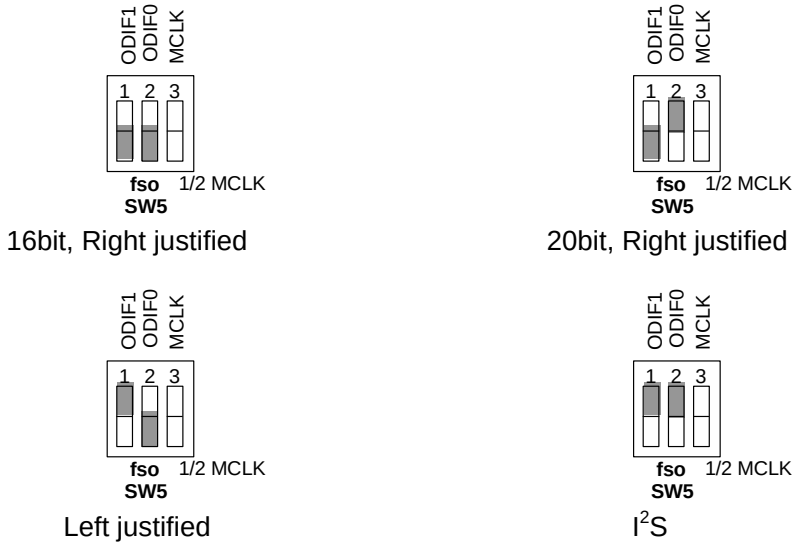


Figure 14. DIP switch setting

3. Bypass Mode

In case of Bypass Mode, please set DIP switch (SW3) as follows.

Mode	SW4-1 CMODE2	SW4-2 CMODE1	SW4-3 CMODE0	MCLK	Master/Slave (Output Port)
7	H	H	H	Not used. Set to DVSS	Master(Bypass)

Table 14. AK4121A System Clock setting

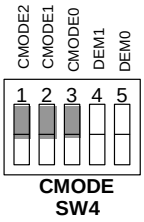


Figure 13. DIP switch setting

3-1. Setting of input block

3-1-1. Optical Input(PORT2)

3-1-1-a. Jumper setting

Parts No.	Setting
JP1	OUT
JP2	SHORT
JP3	SHORT
JP4	SHORT
X1	(don't care)

Table 15. Jumper setting(Refer following figures)

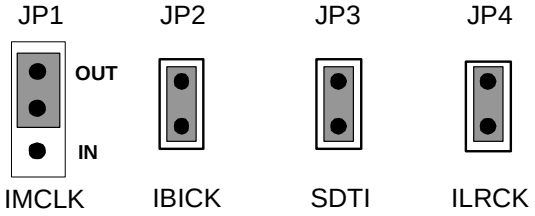


Figure 14. Jumper setting

3-1-1-b. Audio Interface Format setting (IIS only)

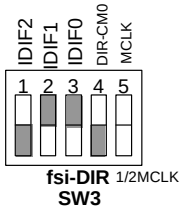


Figure 15. DIP switch (SW3) setting

3-1-2. All clock are fed through the 10-pin port

3-1-2-a. Jumper setting

Parts No.	Setting
JP1	OUT
JP2	OPEN
JP3	OPEN
JP4	OPEN
X1	(don't care)

Table 16. Jumper setting(Refer following figures)

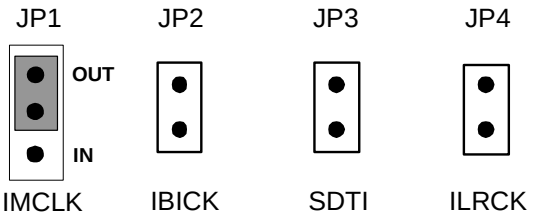
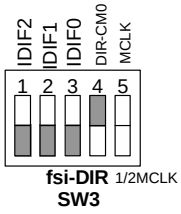


Figure 16. Jumper setting

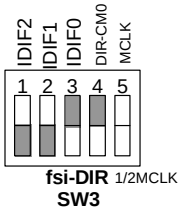
3-1-2-b. Audio Interface Format

Audio Interface Format	SRC:AK4121A		
	SW3-1	SW3-2	SW3-3
	DIF2	DIF1	DIF0
16bit, Right justified	0	0	0
20bit, Right justified	0	0	1
Left justified	0	1	0
I^2S	0	1	1
24bit, Right justified	1	0	0

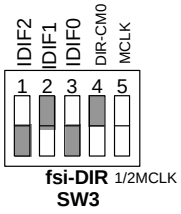
Table 17. DIP switch (SW3) setting



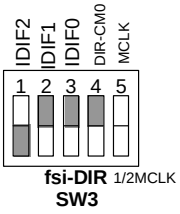
16bit, Right justified



20bit, Right justified



Left justified



I^2S

24bit, Right justified

Figure 17. DIP switch (SW3) setting

3-2. Setting of output block

3-2-1. Optical Output(PORT4). Clock are fed from AK4114 (DIT). (IIS Master Mode only.)

3-2-1-a. Jumper setting

Parts No.	Setting
JP8	SHORT
JP9	SHORT
JP7	SHORT
JP5	(don't care)
JP6	DIR
JP11	OPEN
X2	Remove

Table 18. Jumper setting

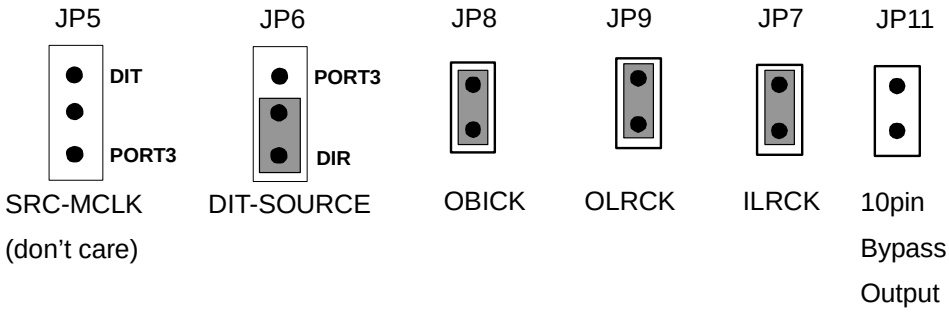


Figure 18. Jumper setting

No.	X1or External Clock (PORT1) (Max: 24.576MHz)	DIP SW3 setting	DIP SW5 setting
		OCKS0 SW3-5	OCKS0 SW5-3
1	256fs	1/2 MCLK	1/2 MCLK
2	512fs	MCLK	MCLK

Table 19. DIR/DIT Clock setting

Figure 19. DIP switch setting

3-2-2. Clock are fed through the 10-pin port(PORT3)

3-2-2-a. Jumper setting

parts No.	setting
JP8	OPEN
JP9	OPEN
JP7	OPEN
JP5	(don't care)
JP6	OPEN
JP11	OPEN
X2	(don't care)

Table20. Jumper setting

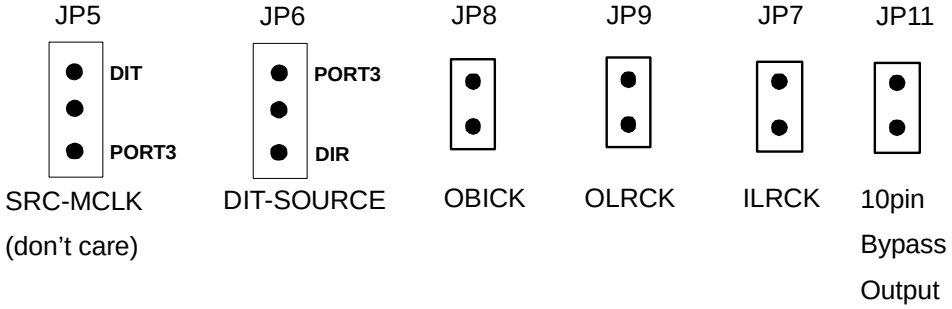


Figure 20. Jumper setting

3-2-2-b. Audio Interface Format

Mode	SW5-1 ODIF1	SW5-2 ODIF0	SDTO Format	OBICK (Master)
0	L	L	16bit LSB Justified	64fs
1	L	H	20bit LSB Justified	64fs
2	H	L	20bit MSB Justified	64fs
3	H	H	20bit I^2S Compatible	64fs

Table 21. AK4121A Audio Interface Format setting

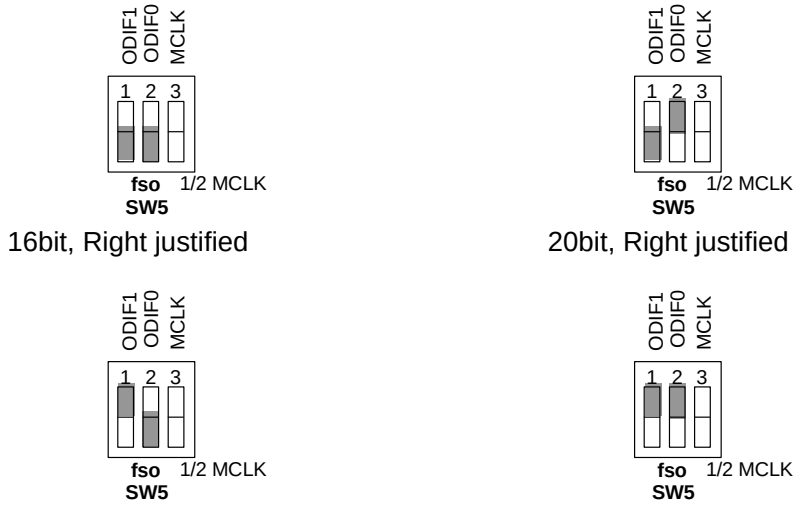


Figure 21. DIP switch setting

4. The other setting

4-1. De-emphasis filter

SW4-4 and SW4-5 control the de-emphasis filter.

Mode	SW4-4 DEM1	SW4-5 DEM0	De-emphasis filter
0	L	L	44.1kHz
1	L	H	OFF
2	H	L	48kHz
3	H	H	32kHz

Table22. De-emphasis filter setting

4-2. Soft Mute

Toggle switch SW2 controls the soft mute.

Mode	SW2 SMUTE	Soft Mute
0	OFF	OFF
1	ON	ON

Table23. Soft Mute setting

■ Jumper List

No.	Jumper Name	Default	Function
10	3.3V	REG	Power supply select for AKD4121A REG : Power supply for AKD4121A is 5V. The VDD(3.3V) of AK4121A is supplied from the regulator. JACK : Power supply for AKD4121A is 3.3V. Optical link is NOT available.
1	IMCLK	IN	MCLK select for fsi port. IN on-board X'tal(X1). OUT : external clock.
2, 3, 4	IBICK, ILRCK, SDTI	Short	Input select for fsi port. Open : PORT2 clock. Short : DIR clock.
5	SRC-MCLK	DIT	MCLK select for fso port. DIT : DIT (AK4114) clock. PORT3 : external clock.
6	DIT-SORUCE	Open	DIT-SORUCE select. Open on-board X'tal(X2). DIR : DIR(AK4112B) clock. PORT3: PORT3 clock.
11	10 pin Bypass Output	Open	Bypass mode select. Short : Setting for bypass mode. Open : for other modes.
7, 8, 9	OBICK, OLRCK, SDTO	Short	Output select for fso port. Open : Use only PORT3. Not use DIT (AK4114) clock. Short : Use DIT clock.

■ DIP switch list

SW3(fsi-DIR)

No.	Switch Name	Default	Function
1, 2, 3	IDIF2, 1, 0	OFF, ON, ON (IIS)	fsi data format. Refer Table 3.
4	DIR-CM0	OFF (Optical)	DIR clock mode. ON : X'tal mode OFF : Optical mode
5	MCLK 1/2MCLK	MCLK	DIR MCLK select. MCLK : 512fs 1/2MCLK : 256fs

SW4(CMODE)

No.	Switch Name	Default	Function
1, 2, 3	CMODE2, 1, 0	OFF, ON, OFF (Master, 512fso)	System clock selects. Refer Table 9, Table 12 and Table 14
4, 5	DEM1, 0	OFF, ON (off)	De-emphasis control. Refer Table 12.

SW5(fso)

No.	Switch Name	Default	Function
1,2	ODIF1, 0	ON, ON (IIS)	fso data format. Refer Table 10.
3	MCLK 1/2MCLK	MCLK	DIT MCLK select. MCLK : 512fs 1/2MCLK : 256fs

■ Toggle switch list (SW1 and SW2)

SW1 is reset switch for AK4121A, AK4112B(DIR) and AK4114(DIT). Set to "H" during Normal operation. Bring to "L" once after the power is supplied.

SW2 is SMUTE control switch. Refer Table 23.

■ LED

Bright when ERF pin of AK4112B goes to "H".
This indicates the UNLOCK state, etc. (Refer AK4112B datasheet).

MEASUREMENT RESULTS

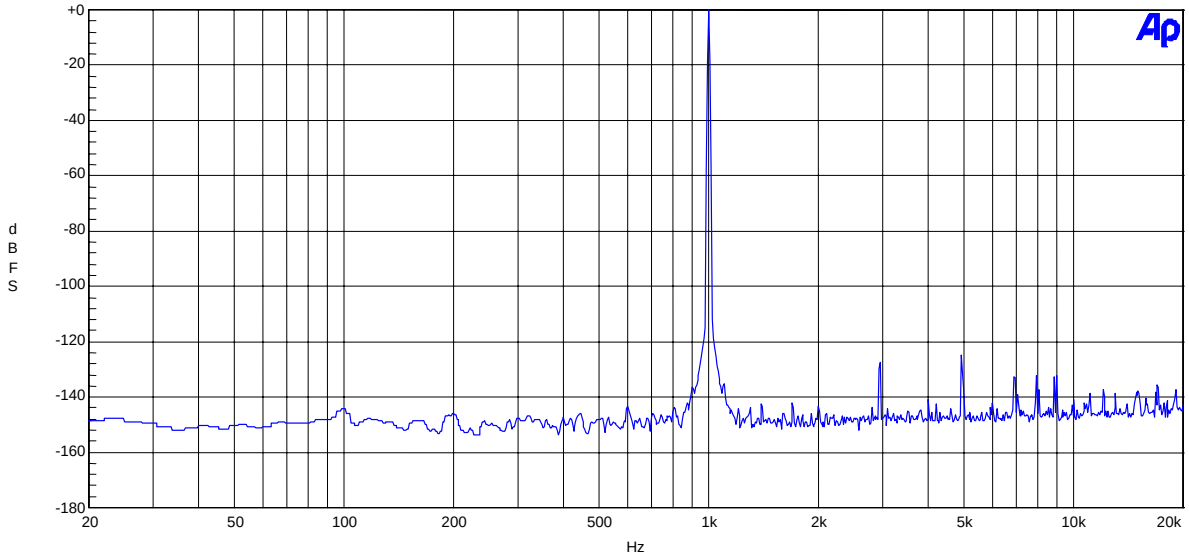
[Measurement Conditions]

Measurement unit : Audio Precision System Two Cascade
VDD : 3.3V
TVDD : 5V
Input Data : 44.1kHz, 20bit, I^2S
Output Data : 48kHz; 20bit, I^2S
Interface : Optical fiber

Parameter	Input signal	Measurement filter	Results
THD+N	1kHz, 0dB	fs/2	–113.5 dB
DR	1kHz, -60dB	fs/2	115.2 dB
DR	1kHz, -60dB	fs/2, A-weighted	117.6 dB

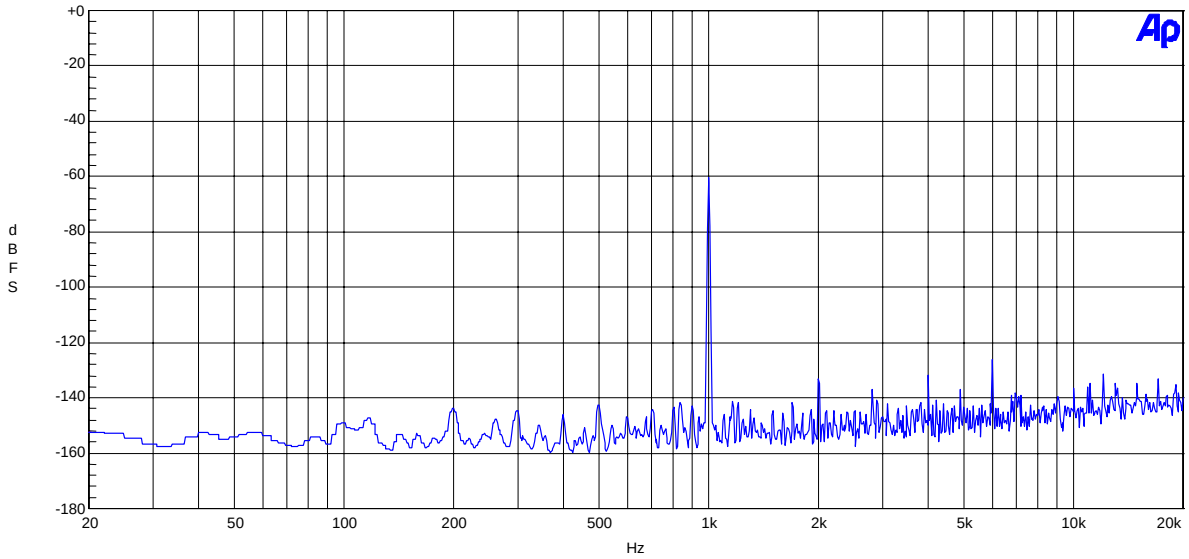
AKM

AK4121A SRC FFT (fsi=44.1kHz, fso=48kHz; fin=1kHz, 0dBFS input)
FFT points 16384, Avg.=8, Window=Equiripple

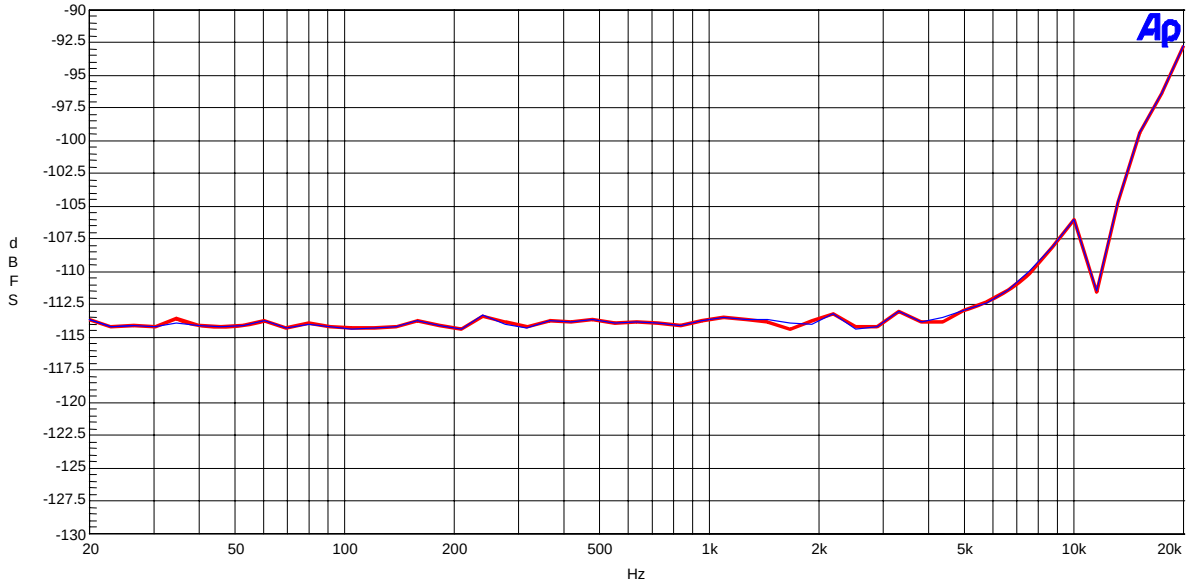


AKM

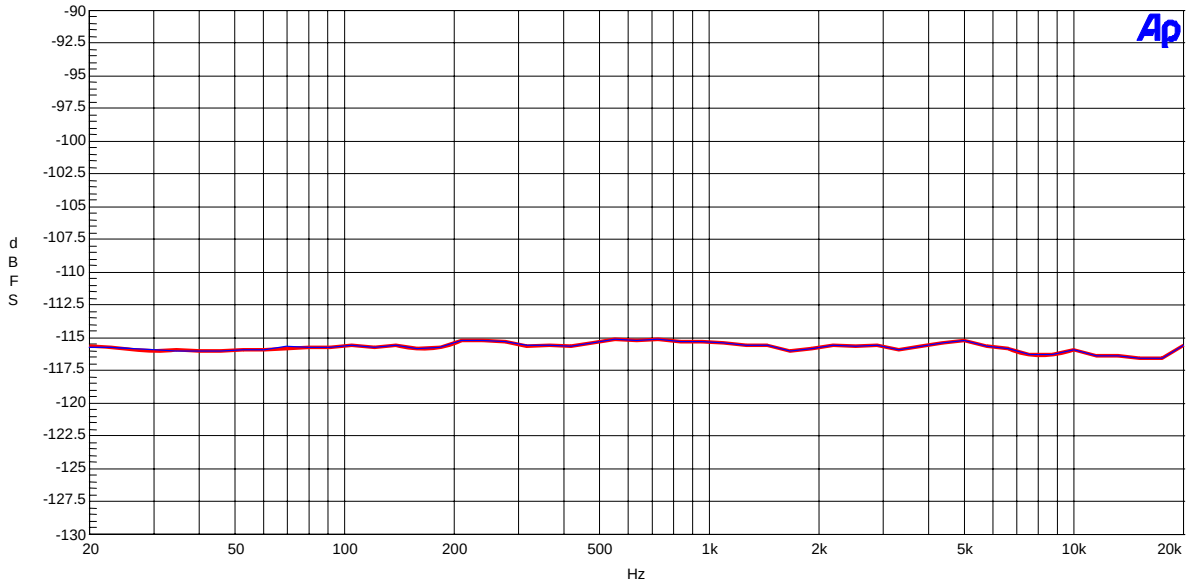
AK4121A SRC FFT (fsi=44.1kHz, fso=48kHz; fsi=1kHz, -60dBFS input)
FFT points 16384, Avg.=8, Window=Equiripple



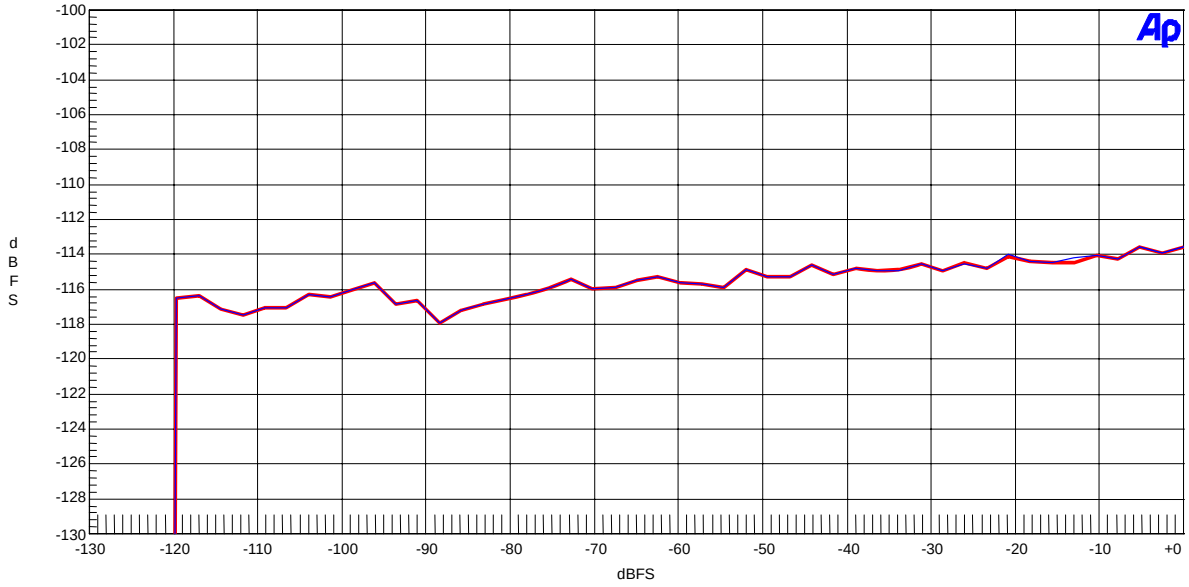
AKM AK4121A SRC THD+N vs. Input Frequency (fsi=44.1kHz, fso=48kHz; 0dBFS input)



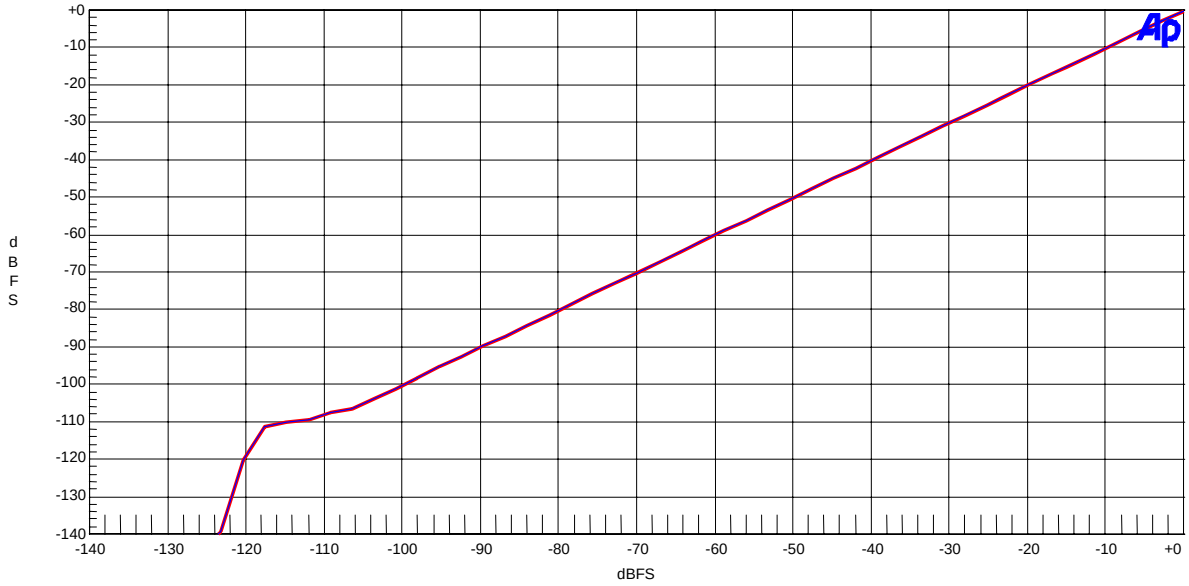
AKM AK4121A SRC THD+N vs. Input Frequency (fsi=44.1kHz, fso=48kHz; -60dBFS input)



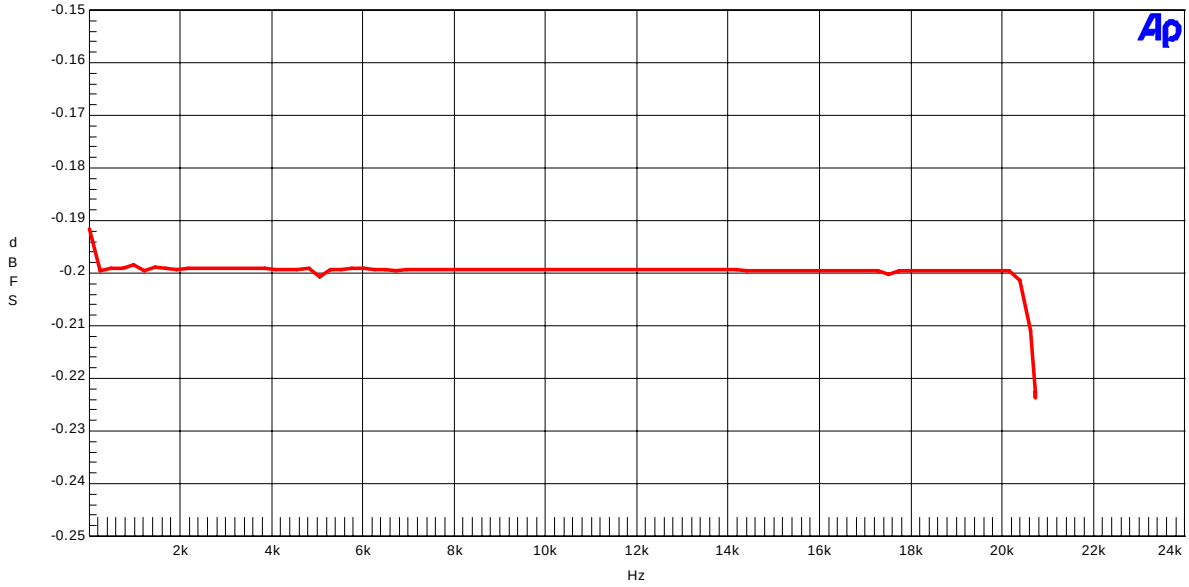
AKM AK4121A SRC THD+N vs. Input Level (fsi=44.1kHz, fso=48kHz; fin=1kHz)



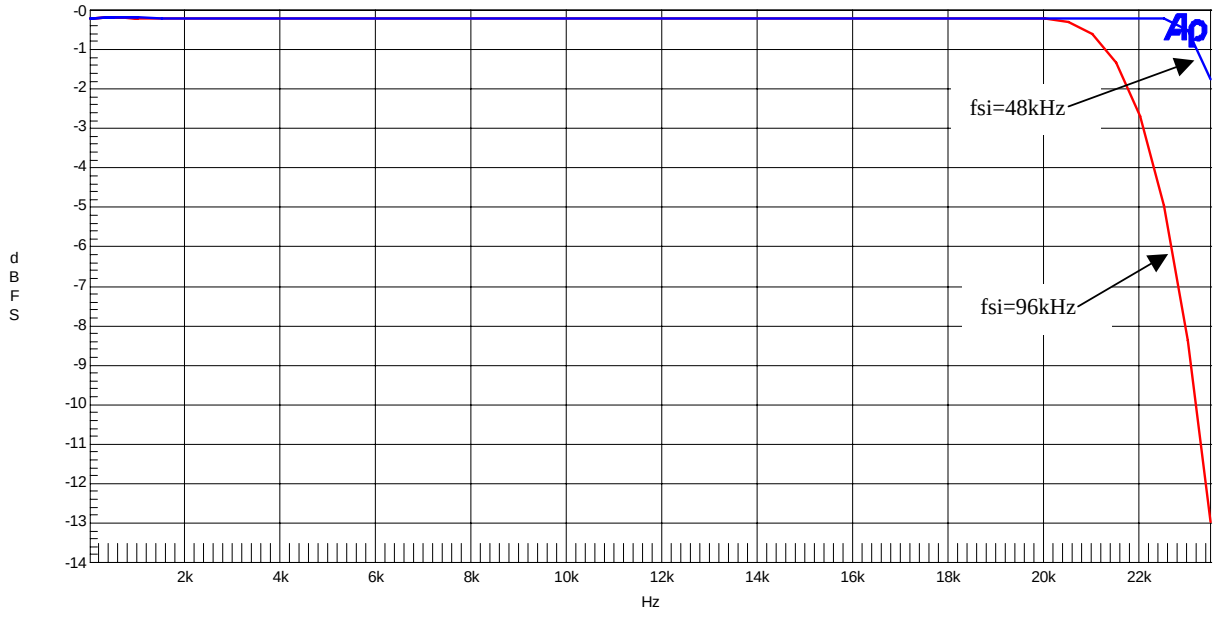
AKM AK4121A SRC Linearity (fsi=44.1kHz, fso=48kHz; fin=1kHz)



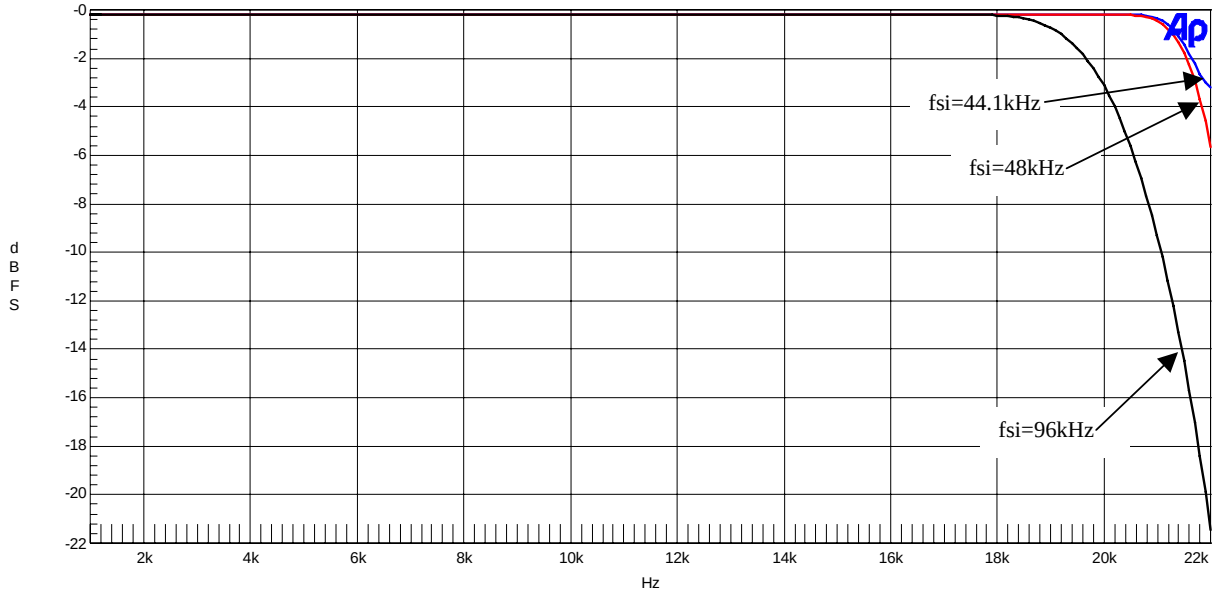
AKM AK4121A SRC Frequency Response (fsi=44.1kHz, fso=48kHz, 0dBFS input)



AK4121A Frequency Response (Blue:fsi=48kHz, Red:fsi=96kHz)
VDD=3.3V, TVDD=5.0V, fso=48kHz

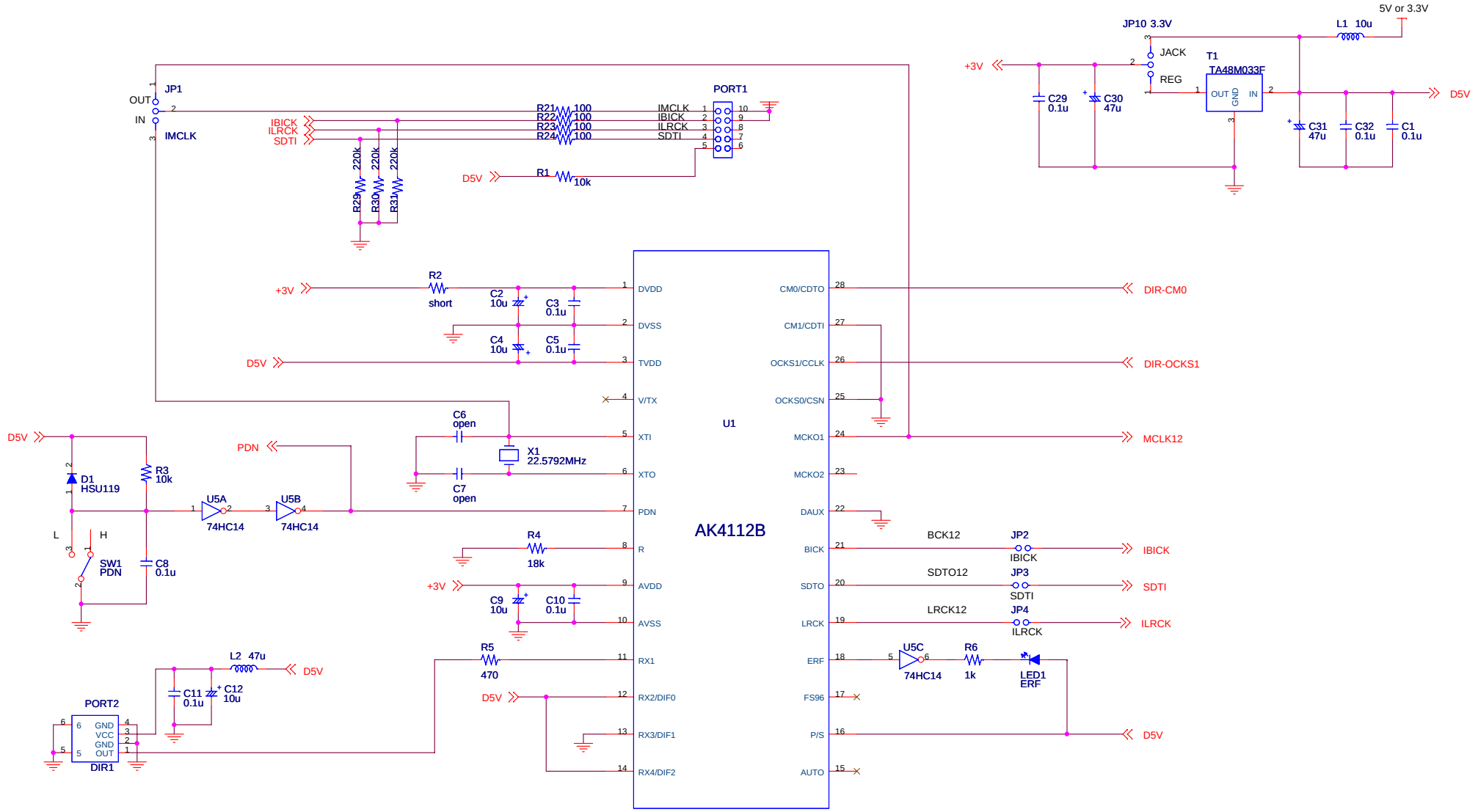


AKM AK4121A Frequency Response (Blue:fsi=44.1kHz, Red:fsi=48kHz, Gray:fsi=96kHz)
VDD=3.3V, TVDD=5.0V, fso=44.1kHz



Revision History

Date (YY/MM/DD)	Manual Revision	Board Revision	Reason	Contents
07/03/22	KM088800	0	First Edition	



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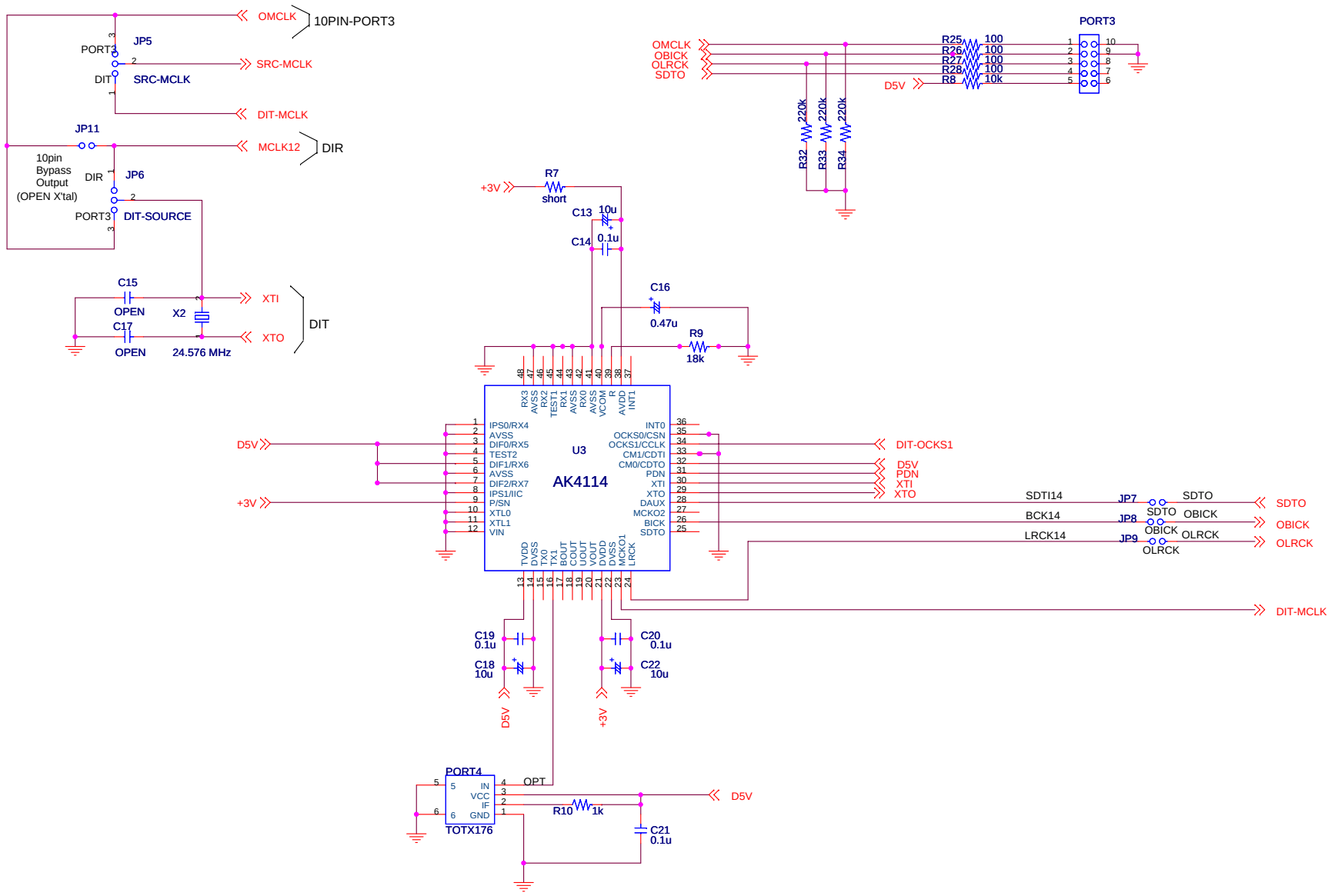
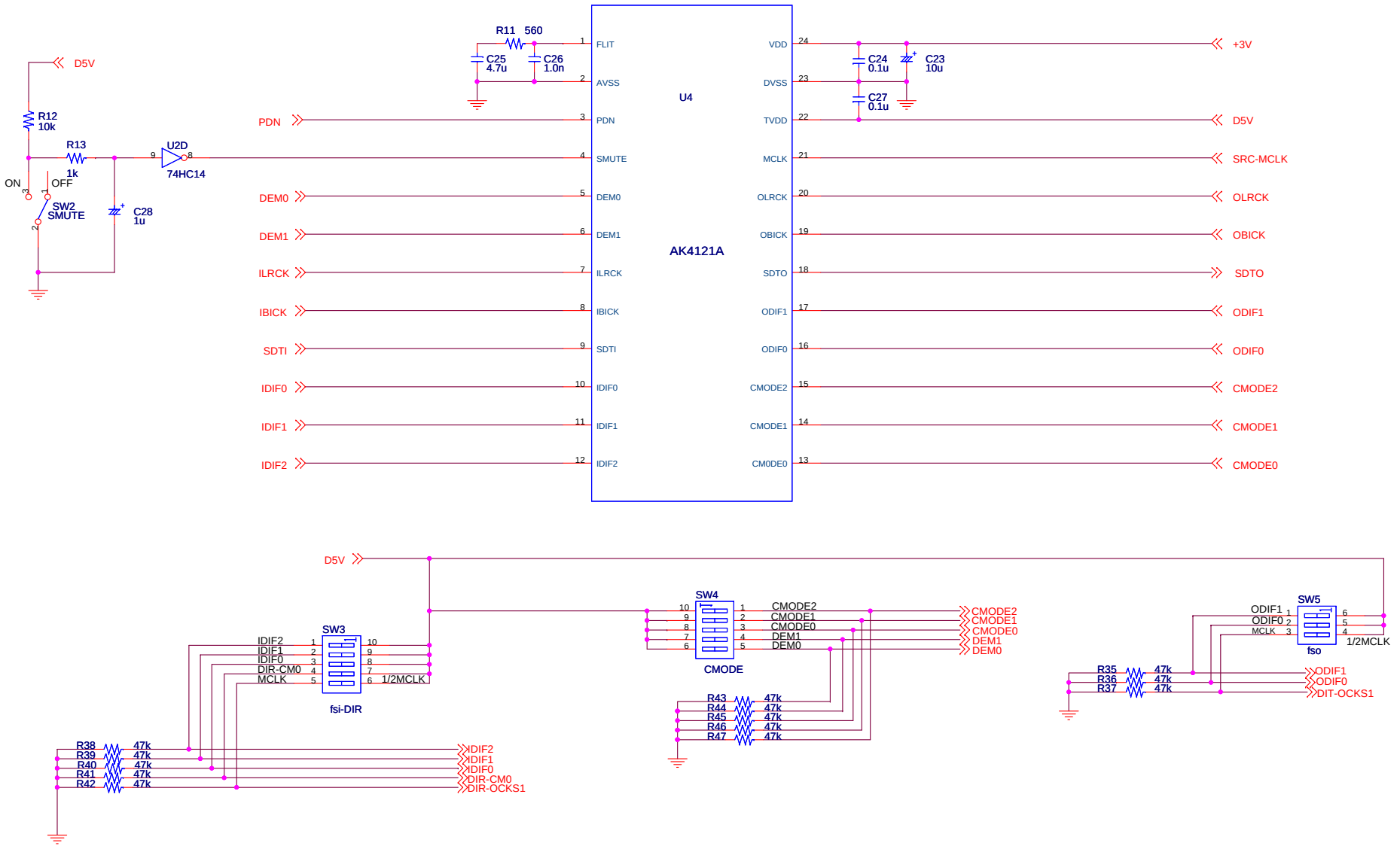
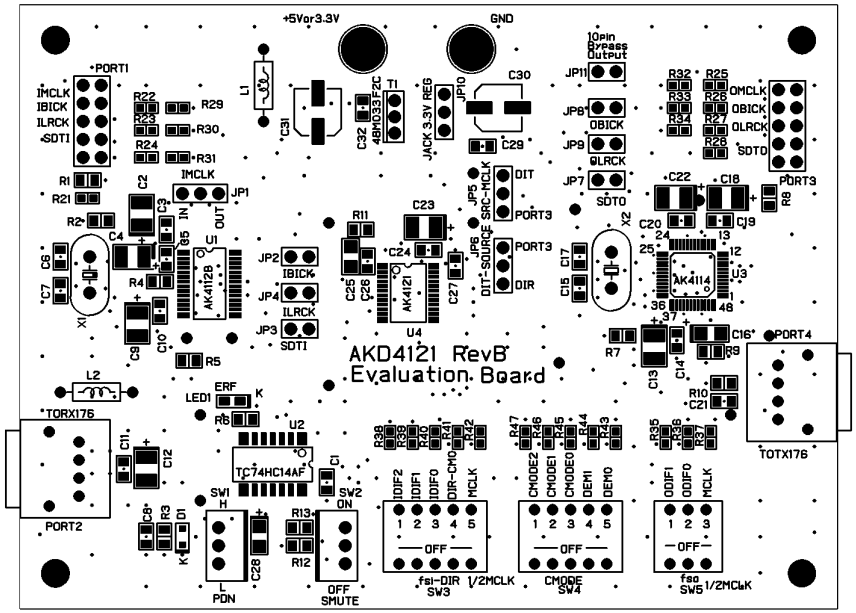
Size A3	Document Number AK4112B	Rev 0
Date: Tuesday, March 20, 2007	Sheet 1 of 3	

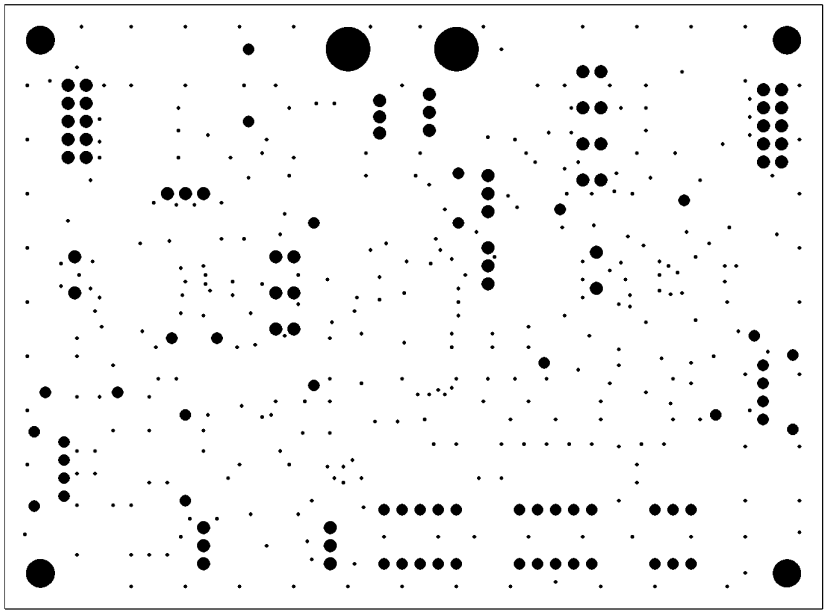


Title	AKD4121A	
Size A3	Document Number AK4114	Rev 0
Date: Tuesday, March 20, 2007	Sheet 2 of 3	

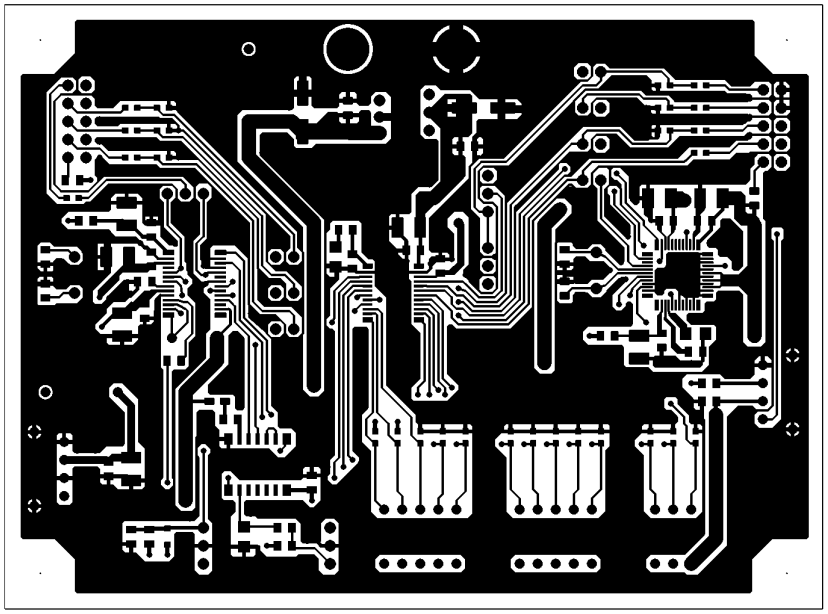


Title	AKD4121A	
Size A3	Document Number AK4121A	Rev 0
Date: Thursday, March 22, 2007	Sheet 3 of 3	

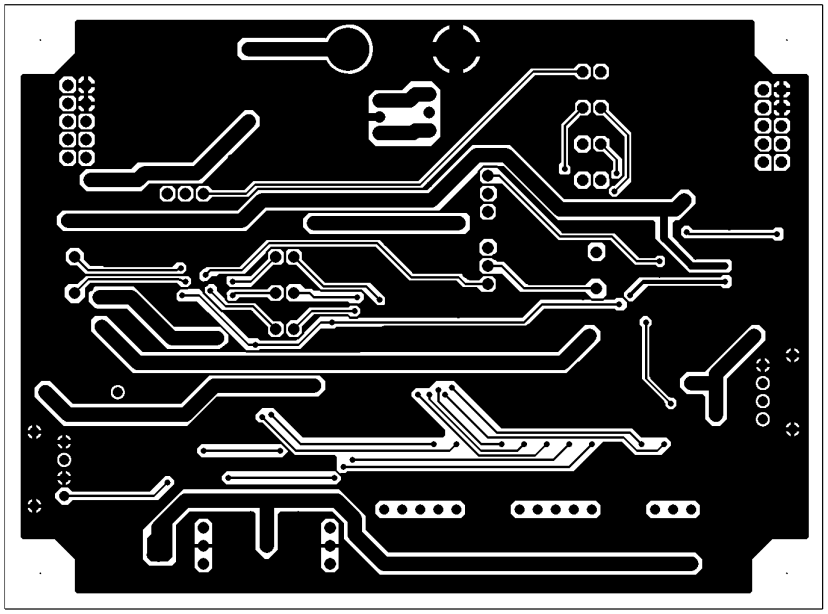

+5Vor3.3V
GND
AKD4121 RevB
Evaluation Board
AKD4121ver2 L1 SR SILK



AKD4121ver2 L2 SR



AKD4121ver2 L1 PATARN



AKD4121ver2 L2 PATARN