A. HE83117 Introduction

HE83117 is a member of 8-bit Micro-controller series developed by King Billion Electronics Ltd. Users can chose any one of combination among 【128 dots LCD Driver + 32 Bit I/O Port】…【64 dots LCD Driver + 48 Bit I/O Port】etc. The built-in OP comparator can be used with (light、voice、temperature、humility) sensor and used as battery low detection. And the 7-bit current-type D/A converter and PWM device provide the complete speech output mechanism. The built-in DTMF generator can generate the PSTN dialing tone directly. The 256K ROM Size can be used in the storage of speech (80 seconds at 3Kbytes per second), graphic, text etc. This IC also built-in A DRAM Interface(16M*4, 16M*1, 4M*4, 4M*1) for store recording data. It can be applicable to the medium systems such as Data Bank、Pocket Dialer、Educational Toy、Digital Voice Recording System and Voice Answer Machine etc..
The instruction set of HE83117 are quite easy to learn and simple to use. Only about thirty instructions with four-type addressing mode are provided. Most of instructions take only 3 oscillator clocks (machine cycles). The processing power is enough to most of battery operation system.

B.HE83117 Features

- Operation Voltage： 2.4V – 5.5V
- System Clock： DC ~ 8MHz @ 5.0V
  DC ~ 4MHz @ 2.4V
- Internal ROM： 256K Bytes(64K Program ROM+192K Data ROM)
- Internal RAM： 256 Bytes.
- Dual Clock System ： Normal (Fast) clock： 32.768K ~ 8MHz
  Slow clock： 32.768KHz
- Operation Mode： DUAL、FAST、SLOW、IDLE、SLEEP Mode.
- With WDT (WATCH DOG TIMER) to prevent deadlock condition..
- 32~48 bit Bi-directional I/O port. Mask Option can select PUSH-PULL or OPEN DRAIN output mode for each I/O pin.
- One built-in OP comparator.
- 128~64 dots LCD driver (A、B TYPE selectable).
- One 7-bit current-type DAC output.
- PWM device.
- Built-in DTMF Generator.
- Two external interrupts and three internal timer interrupts.
- Three 16-bit timer.
- Instruction set： 32 instructions, 4 addressing mode. 8-bit DATA POINTER for RAM and 18-bit TABLE POINTER for ROM.
- Built-in EDO DRAM interface.

C. Internal Block

Please always take in mind that ICE is different from IC. ICE is the whole set of HE80000 series IC, but each IC is a subset of ICE. Never use any hardware resource that real IC didn't have, especially RAM and register. KBIDS and compiler cannot prevent user to use some hardware resource that didn't exist. Please check the following table and refer the abbreviation in HE80000 user's manual.

I.F.C.	E.S.C.	I.P.R	PROM	DROM	TP	TP+1	RAM	PP	DP	I/O	DTMF	WDT	Timer
◎	◎	◎	64KB	192KB	18-bit	◎	256B	—	8-bit	32~48	◎	◎	T1,T2,TB

VO	DAO	OP	PWM	LCD	COM*SEG	Bias	Rgr	ChrgPmp	LV2	LR	LVG	REC	S.R.
◎	◎	◎	◎	128~64	4*32	1/3	—	1,3/2,3	◎	—	—	Ext.	I

D. Pin Description

Pin #	Pin name	I/O	Function	Description
64 63	**FXI,** **FXO**	B, O	External fast clock pin. Connecting to crystal or RC to generate 32.768 kHz ~ 8MHz frequency.	Mask option setting： MO_FCK/SCKN= 00：Slow Clock only 01：Illegal 10：Dual Clock 11：Fast Clock only MO_FOSCE = 0：Internal fast osc. = 1：External fast osc. MO_FXTAL = 0：RC osc. for fast clock = 1：X'tal osc. for fast clock MO_SXTAL = 0：RC for 32768 Hz clock = 1：X'tal for 32768 Hz clock Use OP1 and OP2 to switch among different operation mode (NORMAL, SLOW, IDEL and SLEEP). In Dual Clock mode, the main system clock is still the Fast Clock. The 32768 Hz clock is for LCD and Timer 1 only.
67 66	**SXI,** **SXO**	I, O	External slow clock pin. Connecting with 32768 Hz crystal or resistor as slow clock and providing clock source for LCD display, TIMER1, Time-Base and other internal blocks.	
62	**RSTP_N**	I	System Reset.	Level trigger, active low. Except for using this pin, using mask option (MO_PORE=1) could enable IC build-in Power-on reset circuit. Besides, MO_WDTE can set Watch Dog Timer： MO_WDTE=0：Disable Watch Dog Timer =1：Enable Watch Dog Timer
65	**TSTP_P**	I	Test Pin	Please bond this pin and add a test point on PCB for debugging. Leave this pin floating is OK.
81.. 88	**PRTC[7:0]**	B	8-pin bi-directional I/O port.	Mask options： MO_CPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
73.. 80	**PRTD[7:0]**	B	8-pin bi-directional I/O port. PRTD[7..2] as wake-up pin. PRTD[7..6] as external	Mask options： MO_DPP[7..0]=1 ~ Push-pull. =0 ~ Open-drain.

Pin #	Pin name	I/O	Function	Description
			interrupt pin.	Output must be "1" before reading whenever use them as input (No tri-state structure).
5.. 12	**PRT10[7:0]/ DRAM Pins**	B	8-pin bi-directional I/O port.	Mask Option : MO_DRAM=1 ~ as DRAM Pins. MO_DRAM=0 ~ as I/O Pins。 MO_10PP[7..0] =1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
89.. 92 1..4	**PRT11[7:0]/ DRAM Pins**	B	8-pin bi-directional I/O port.	Mask Option : MO_DRAM=1 ~ as DRAM Pins. MO_DRAM=0 ~ as I/O Pins。 MO_11PP[7..0] =1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
23.. 30	**PRT14[7:0]/ SEG[23:16]**	B/ O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO14[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_14PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
15.. 22	**PRT15[7:0]/ SEG[31:24]**	B/ O	8-pin bi-directional I/O port that is shared with LCD segment pin.	Mask options： MO_LIO15[7..0]=1 ~ LCD Pin. =0 ~ I/O Pin. MO_15PP[7..0]=1 ~ Push-pull. =0 ~ Open-drain. Output must be "1" before reading whenever use them as input (No tri-state structure).
47.. 50	**COM[3:0]**	O	LCD COMmon Output	LCD Data filled from F0H, please refer the LCD RAM map.
31.. 46	**SEG[15:0]**	O	LCD SEGment Output	
52	**LC2**	B	Charge Pump Switch 2	Add one 0.1 μF capacitor between LC1 and LC2. Please refer the application circuit.
51	**LC1**	B	Charge Pump Switch 1	
55	**L V3**	B	Charge Pump V3	LV3< 9 Volts. Please refer the application circuit.
54	**L V2**	B	Charge Pump V2	
53	**L V1**	B	Charge Pump V1	
13	**PWMP**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
14	**PWMN**	O	The PWM positive output can drive speaker or buzzer directly.	Set the bit2 of VOC register as one to turn on PWM.
57	**VO**	O	D/A output.	Bit 1 of VOC = '1' , Turn on DA
58	**DAO**	O	DAC Voice Output	Set the bit1(DA=1) of VOC register to turn on DAC with VO output.
59	**OPIN**	I	OPAMP negative input pin.	Built-in OP comparator. Set Bit 0 of VOC = '1' , Turn on OP
60	**OPIP**	I	OPAMP positive input pin.	
61	**OPO**	O	OPAMP output pin.	

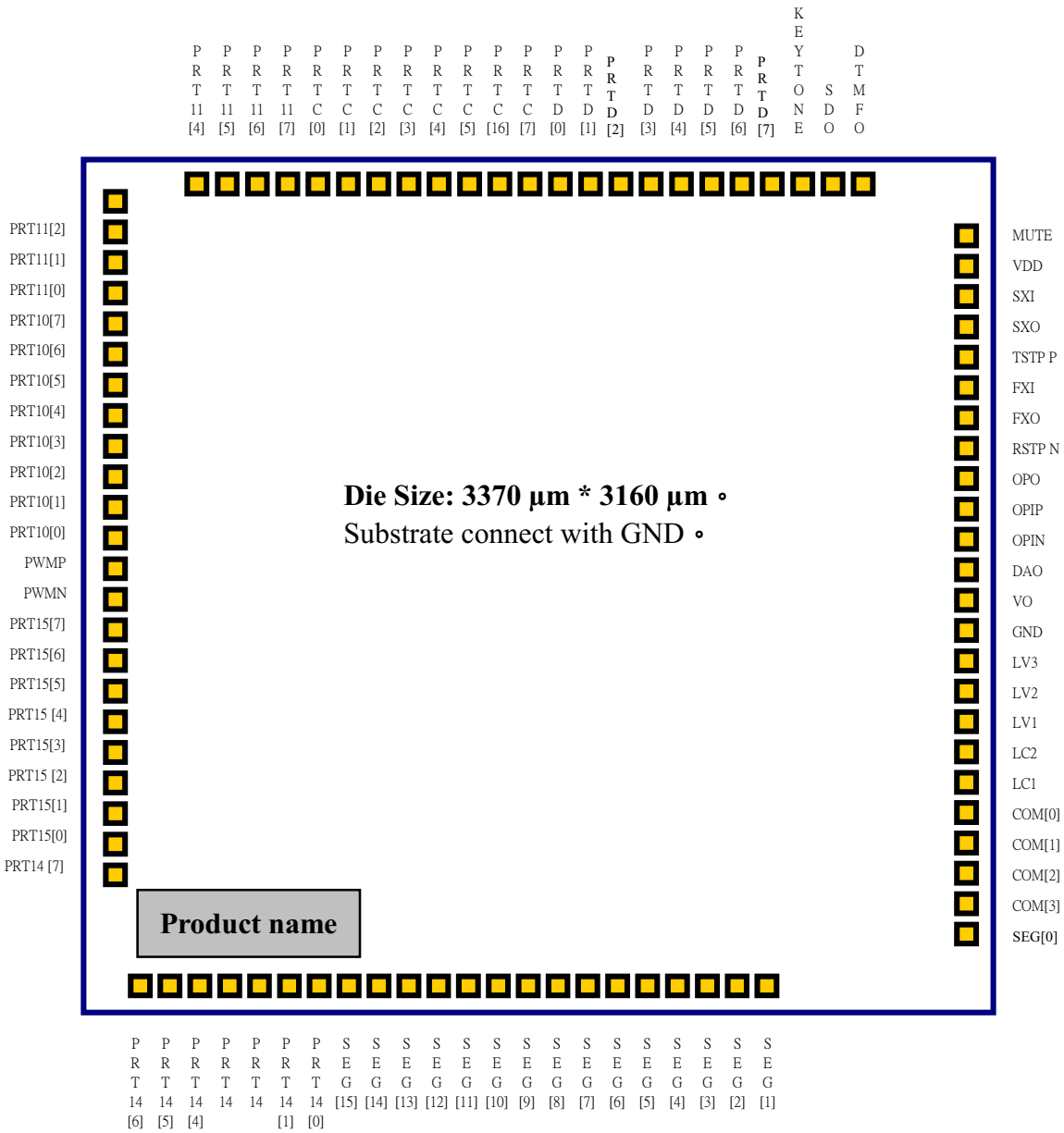
Pin #	Pin name	I/O	Function	Description
70	**DTMFO**	O	DTMF Output	Through PRT12 we can turn on/off DTMF and write data. Using Mask Option MO_DTMFSCK set the clock source of DTMF block. MO_DTMFSCK=0；Clock Source=3.579545 MHz =1；Clock Source=32768 Hz
69	**MUTE**	O	MUTE Output for Dialer	User can turn on/off MUTE pin by port12.
71	**SDO**	O	Serial Data Output	We can turn on/off SDO block or write data by port12.
72	**KEYTONE**	O	1024-Hz 50% duty square wave	User can turn on/off key tone by port12.
68	**VDD**	P	Positive Power Input	Adding 0.1 μF capacitor as by-pass capacitor on power pins is necessary. (within 1 cm distance)
56	**GND**	P	Power Ground Input	

E. LCD RAM Map

Page 0:

F0H	SEG1	SEG0	F8H	SEG17	SEG16
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F1H	SEG3	SEG2	F9H	SEG19	SEG18
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F2H	SEG5	SEG4	FAH	SEG21	SEG20
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F3H	SEG7	SEG6	FBH	SEG23	SEG22
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F4H	SEG9	SEG8	FCH	SEG25	SEG24
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F5H	SEG11	SEG10	FDH	SEG27	SEG26
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F6H	SEG13	SEG12	FEH	SEG29	SEG28
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]
F7H	SEG15	SEG14	FFH	SEG31	SEG30
	COM[3:0]	COM[3:0]		COM[3:0]	COM[3:0]

F. Pin Diagram



G. Bonding Pad Location

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
1	PRT11[3]	X= -1609.00	Y= 1440.50	47	COM[3]	X= 1608.70	Y= -1327.70
2	PRT11[2]	X= -1609.00	Y= 1325.00	48	COM[2]	X= 1608.70	Y= -1212.20
3	PRT11[1]	X= -1609.00	Y= 1209.50	49	COM[1]	X= 1608.70	Y= -1096.70
4	PRT11[0]	X= -1609.00	Y= 1094.00	50	COM[0]	X= 1608.70	Y= -981.10
5	PRT10[7]	X= -1609.00	Y= 978.50	51	LC1	X= 1608.70	Y= -865.60
6	PRT10[6]	X= -1609.00	Y= 863.00	52	LC2	X= 1608.70	Y= -750.10
7	PRT10[5]	X= -1609.00	Y= 747.50	53	LV1	X= 1608.70	Y= -634.60
8	PRT10[4]	X= -1609.00	Y= 632.00	54	LV2	X= 1608.70	Y= -519.10
9	PRT10[3]	X= -1609.00	Y= 516.50	55	LV3	X= 1608.70	Y= -403.60
10	PRT10[2]	X= -1609.00	Y= 400.90	56	GND	X= 1608.70	Y= -288.10
11	PRT10[1]	X= -1609.00	Y= 285.40	57	VO	X= 1608.70	Y= -154.50
12	PRT10[0]	X= -1609.00	Y= 169.90	58	DAO	X= 1608.70	Y= -2.70
13	PWMP	X= -1609.00	Y= 30.20	59	OPIN	X= 1608.70	Y= 130.90
14	PWMN	X= -1609.00	Y= -133.20	60	OPIP	X= 1608.70	Y= 246.40
15	PRT15[7]	X= -1609.00	Y= -272.20	61	OPO	X= 1608.70	Y= 361.90
16	PRT15[6]	X= -1609.00	Y= -387.80	62	RSTP_N	X= 1608.70	Y= 477.40
17	PRT15[5]	X= -1609.00	Y= -503.20	63	FXO	X= 1608.70	Y= 593.00
18	PRT15[4]	X= -1609.00	Y= -618.80	64	FXI	X= 1608.70	Y= 708.50
19	PRT15[3]	X= -1609.00	Y= -734.20	65	TSTP_P	X= 1608.70	Y= 824.00
20	PRT15[2]	X= -1609.00	Y= -849.80	66	SXO	X= 1608.70	Y= 939.50
21	PRT15[1]	X= -1609.00	Y= -965.20	67	SXI	X= 1608.70	Y= 1055.00
22	PRT15[0]	X= -1609.00	Y= -1080.80	68	VDD	X= 1608.70	Y= 1170.50
23	PRT14[7]	X= -1609.00	Y= -1196.20	69	MUTE	X= 1608.70	Y= 1286.00
24	PRT14[6]	X= -1542.20	Y= -1503.00	70	DTMFO	X= 1265.20	Y= 1501.60
25	PRT14[5]	X= -1426.80	Y= -1503.00	71	SDO	X= 1149.70	Y= 1501.60
26	PRT14[4]	X= -1311.20	Y= -1503.00	72	KEYTONE	X= 1021.20	Y= 1501.60
27	PRT14[3]	X= -1195.80	Y= -1503.00	73	PRTD[7]	X= 892.20	Y= 1501.60
28	PRT14[2]	X= -1080.20	Y= -1503.00	74	PRTD[6]	X= 776.80	Y= 1501.60
29	PRT14[1]	X= -964.80	Y= -1503.00	75	PRTD[5]	X= 661.20	Y= 1501.60
30	PRT14[0]	X= -849.20	Y= -1503.00	76	PRTD[4]	X= 545.80	Y= 1501.60
31	SEG[15]	X= -733.80	Y= -1503.00	77	PRTD[3]	X= 430.20	Y= 1501.60
32	SEG[14]	X= -618.20	Y= -1503.00	78	PRTD[2]	X= 314.80	Y= 1501.60
33	SEG[13]	X= -502.80	Y= -1503.00	79	PRTD[1]	X= 199.20	Y= 1501.60
34	SEG[12]	X= -387.20	Y= -1503.00	80	PRTD[0]	X= 83.80	Y= 1501.60
35	SEG[11]	X= -271.80	Y= -1503.00	81	PRTC[7]	X= -31.80	Y= 1501.60
36	SEG[10]	X= -156.20	Y= -1503.00	82	PRTC[6]	X= -147.20	Y= 1501.60

PIN Number	PIN Name	X Coordinate	Y Coordinate	PIN Number	PIN Name	X Coordinate	Y Coordinate
37	SEG[9]	X= -40.80	Y= -1503.00	83	PRTC[5]	X= -262.80	Y= 1501.60
38	SEG[8]	X= 74.80	Y= -1503.00	84	PRTC[4]	X= -378.20	Y= 1501.60
39	SEG[7]	X= 190.20	Y= -1503.00	85	PRTC[3]	X= -493.80	Y= 1501.60
40	SEG[6]	X= 305.80	Y= -1503.00	86	PRTC[2]	X= -609.20	Y= 1501.60
41	SEG[5]	X= 421.20	Y= -1503.00	87	PRTC[1]	X= -724.80	Y= 1501.60
42	SEG[4]	X= 536.80	Y= -1503.00	88	PRTC[0]	X= -840.20	Y= 1501.60
43	SEG[3]	X= 652.20	Y= -1503.00	89	PRT11[7]	X= -955.80	Y= 1501.60
44	SEG[2]	X= 767.80	Y= -1503.00	90	PRT11[6]	X= -1071.20	Y= 1501.60
45	SEG[1]	X= 883.20	Y= -1503.00	91	PRT11[5]	X= -1186.80	Y= 1501.60
46	SEG[0]	X= 1608.70	Y= -1443.20	92	PRT11[4]	X= -1302.20	Y= 1501.60

H. DC/AC Characteristics

Absolute Maximum Rating

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	-0.5V ~ 8V	
Input Voltage	V_{in}	-0.5V ~ V_{dd}+0.5V	
Output Voltage	V_o	-0.5V ~ V_{dd}+0.5V	
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

Recommended Operating Conditions

Item	Sym.	Rating	Condition
Supply Voltage	V_{dd}	2.4V ~ 5.5V	
Input Voltage	V_{ih}	0.9 V_{dd} ~ V_{dd}	
	V_{il}	0.0V ~ 0.1V_{dd}	
Operating Frequency	Fmax	8MHz	V_{dd} =5.0V
		4MHz	V_{dd} =2.4V
Operating Temperature	T_{op}	0^0C ~ 70^0C	
Storage Temperature	T_{st}	-50^0C ~ 100^0C	

測試條件:TEMP=25℃, VDD=3V+/-10%, GND=0V

	PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
I_{Fast}	NORMAL Mode Current	System	2M ext. R/C		0.75	1	mA
I_{Slow}	SLOW Mode Current	System	32.768K X'tal LCD Disable		6	9	μA
I_{Idle}	IDLE Mode Current	System	32.769K X'tal LCD Disable		4	7	μA
I_{LCD}	Extra Current if LCD ON	System	LCD Enable		2	3	μA
I_{Sleep}	Sleep Mode Current	System				1	μA
I_{oHPWM}	PWM Output Drive Current	PWMP, PWMN*2	V_{DD}=3V; V_{oh}=2V	12	15		mA
I_{oLPWM}	PWM Output Sink Current	PWMP, PWMN*2	V_{DD}=3V; V_{oL}=1V	33	40		mA
I_{oVO}	DAC Output Current	VO, DAO	V_{DD}=3V;VO=0~2V,Data=7F	2.5	3		mA
V_{iH}	Input High Voltage	I/O pins		0.8 V_{DD}			V
V_{iL}	Input Low Voltage	I/O pins				0.2 V_{DD}	V
V_{hys}	Input Hysteresis Width	I/O, RSTP_N	Threshold=2/3V_{DD}(input from low to high) Threshold=1/3V_{DD}(input from high to low)		1/3 V_{DD}		V
I_{oH}	Output Drive Current	I/O pull-high*1	V_{oL}=2.0V	50			μA
I_{oL_1}	Output Sink Current	I/O pull-low*1	V_{oL}=0.4V	1.0			mA
I_{iL_1}	Input Low Current	RSTP_N	V_{iL}=GND, pull high Internally		20		μA
I_{iL_2}	Input Low Current	I/O	V_{iL}=GND, if pull high Internally by user		100		μA

Note: *1: Drive Current Spec. for Push-Pull I/O port only
Sink Current Spec. for both Push-Pull and Open-Drain I/O port.
*2: This Spec. base on one driver only. There are five build-in driver, so user just multiply the number of driver he used to one driver current to get the total amount of current. (I_{oHPWM}、I_{oLPWM} * N; N=0,1,2,3,4,5)

I. DRAM Interface

HE83117 provide DRAM interface circuit for user to access the external DRAM with a programmable configuration of DRAM size from 16Mx4, 16Mx1, 4Mx4, 4Mx1 and so on. At the same time, it can interface with two dieces of DRAM. It is more flexibility for user to develop different kind of project such as Digital answer machine and Digital voice recorder.

The DRAM interface command register:

BIT7	BIT6	BIT5	BIT4	BIT [3..0]
0: Command mode 1: Initialize mode	Not use	0:No Overflow occurs 1:Column address Overflow	0: Disable address increase 1: Auto address increase	Command Selection / Type of DRAM selection

BIT 7 = 0: DRAM interface command mode
1: Initialize the DRAM configuration mode
BIT 6 = x: Not use
BIT5 = 1: Column address overflow. Otherwise, BIT5 = 0
BIT4 = 0: keeps address while R/W DRAM data
1: address+1 automatically while R/W DRAM data

BIT [3..0] =
DRAM interface command mode:

0xxx 0001 Increases DRAM address by 1,the whole DRAM address buffer (Row + Column) will be added by 1.

0xxx 0010 Update DRAM address buffer, after receive this command the next 3 "STA" to register R_DRMA will be treated as address update in the following way

Bit 3-0	Bit 3-0	
Row 11-8	Column11-8	1 st write
Row 7-0		2 nd write
Column 7-0		3 rd write

0xxx 0011 Read DRAM address buffer, after receive this command, the next 3 "LDA" from register R_DRMA can be read back address buffer in the order the same as command with Update DRAM address buffer (0xxx 0010).

0xxx 0100 Read DRAM data, DRAM interface circuit will activate corresponding signals to read DRAM data pointer by address buffer into internal DRAM data buffers (R_DRMD). "LDA" instruction is used to read the R_DRMD data to ACC.

0xxx 1000 Clear Column address overflow bit

Note: (1) If user continuously execute " STA R_DRMA " without changing address or data, refresh cycle could be blocked to long and DRAM is lost.
(2) Sleep /Slow/IDLE mode will stop or slow down the refresh cycle . Data in DRAM will be lost.
(3) Refresh cycle stops at reset cycle. A long RSTP_N low cycle(> 30ms @ FCK=4MHz) could cause DRAM data lost
(4) To make sure correct read, there must be at least 1 instruction cycle delay between " Read DRAM data" command and "LDA R_DRMD" instruction
(5) DRAM is continuously refreshed when MCU is not in
- DRAM read cycle
-DRAM write cycle
-Reset cycle = RSTP_N pin low level +16fast clock cycles

Initialize DRAM configuration mode :

1xxx RRCC Configure DRAM

RRCC :	Column address width definition
XX00	9 bits
XX01	10 bits
XX10	11 bits
XX11	12 bits

RRCC	Row address width definition
00XX	9 bits
01XX	10 bits
10XX	11 bits
11XX	12 bits

Note: (1) Unused address pin will send out '0' at corresponding DRAM R/W cycle
(2) 1 DRAM can be omit for 4bit I/O

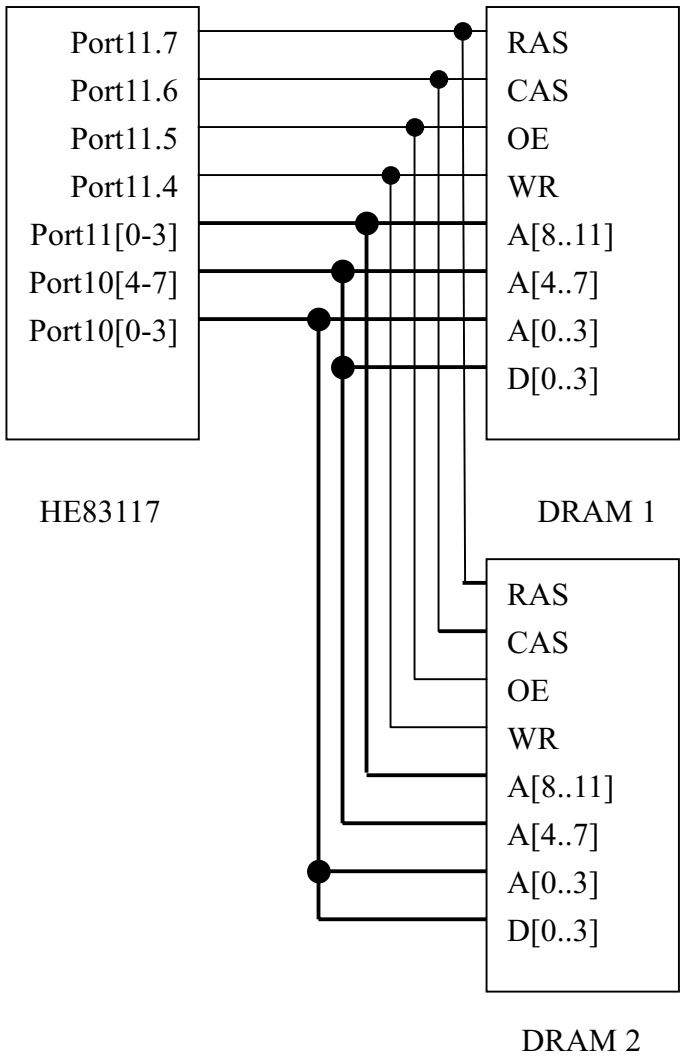
Example is shown as below:

```
_temp           equ     10h

_drma_inc       equ     01h
_drma_write     equ     02h
_drma_read      equ     03h
_drmd_rd        equ     04h
_drmc_clrv      equ     08h

                :
                :

lda     #10000101b      ; automatically Address++ disable while R/W DRAM data,
                        ; row =10 , columm=10
sta     r_drmc


sta     r_drmc          ; store the configuration of DRAM into DRAM control register
lda     #_drma_write    ; Update DRAM address buffer, after receive this command , the
sta     r_drmc          ; next 3 "STA" to register R_DRMA will be treated as address update

lda     #13h            ; Row=135h , Col=3ffh
```

```
sta     r_drma              ;
lda     #35h                ;
sta     r_drma
lda     #0ffh
sta     r_drma

lda     #10010101b          ; automatically Address++ enable while R/W DRAM data,
                            ; row =10 , columm=10
sta     r_drmc              ; store the configuration of DRAM into DRAM control register

lda     #00h                ; write data 00 to DRAM , also increase Column address (Col = 400h)
sta     r_drmd

lda     r_drmc              ; check Column address overflow
anda    #00111111b
sta     r_prtd

lda     #_drmc_clrv         ; clear Column overflow
sta     r_drmc


lda     #10000101b          ; Address++ disable, row =10 , column=10
sta     r_drmc              ; store the configuration of DRAM into DRAM control register

lda     #0ffh
sta     r_drmd              ; write data ffh to DRAM

lda     #_drma_inc          ; increasing one of DRMA
sta     r_drmc

lda     #10010101b          ;Address++ enable, row=10 ,column =10
sta     r_drmc

lda     #0aah
sta     r_drmd
sta     r_drmd              ; twice


lda     #_drma_read         ; Read DRAM address buffer. After receive this command, the
sta     r_drmc              ; next 3 " LDA" from register R_DRMA can read back address
                            ; buffers.
lda     r_drma
sta     r_prtd
lda     r_drma
sta     r_prtd
lda     r_drma
sta     r_prtd


lda     #_drmd_rd           ; read DRAM data
sta     r_drmc
nop
lda     r_drmd
sta     r_prtd

lda     #10000101b
sta     r_drmc

lda     #_drmd_rd           ; read DRAM data
sta     r_drmc
```

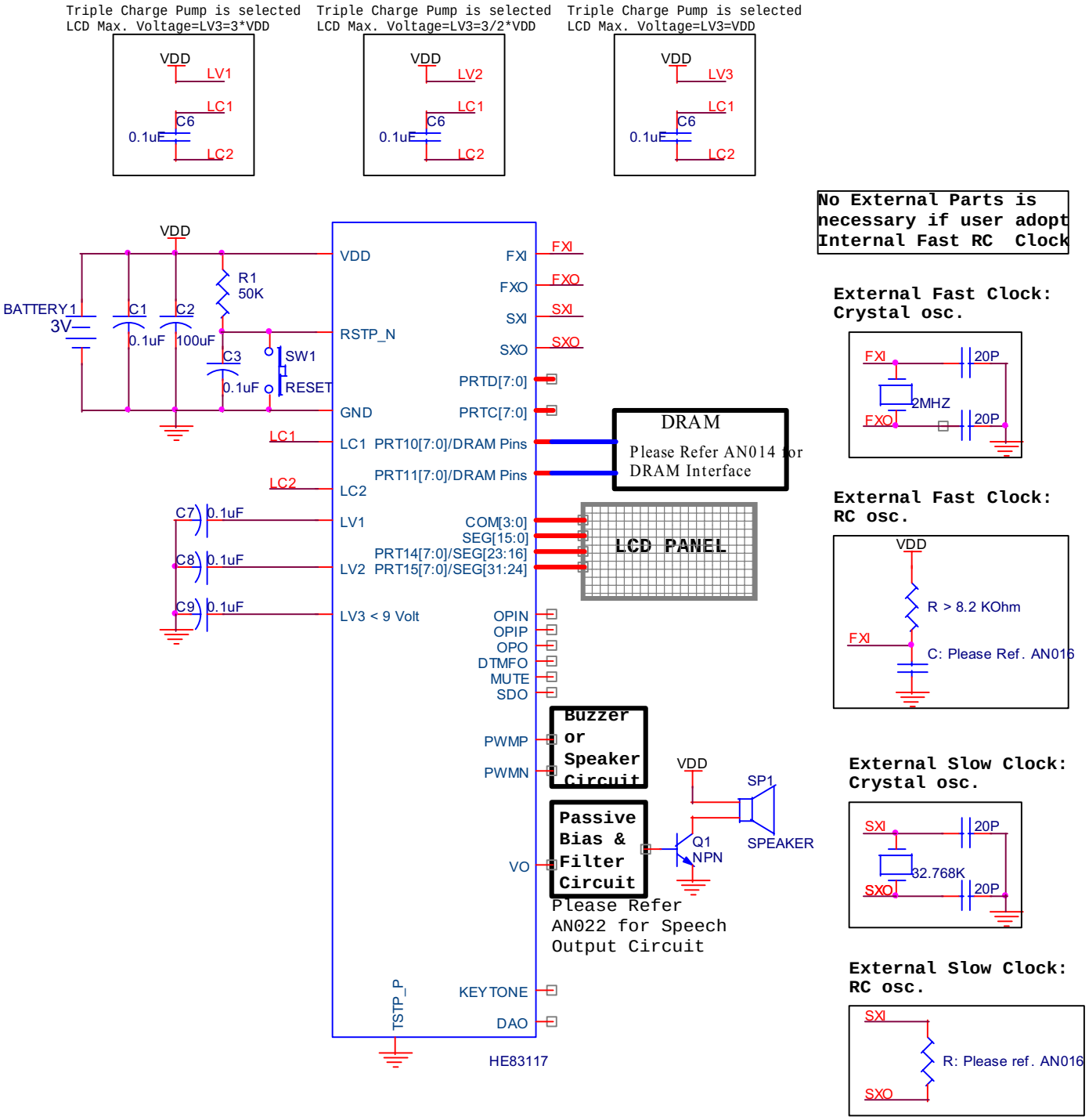
```
sta     r_drmc          ; twice
nop                     ; To make sure correct read, there must be at least 1 instruction cycle delay between
                        ;" Read DRAM data" command and "LDA R_DRMD" instruction
lda     r_drmd
sta     r_prtd
```

DRAM connection:



Important: Be notice that the DRAM Refresh Cycle is controlled by the fast clock of HE83117. For system who switching or running in slow clock operation, the DRAM data may lost. For proper operation, it is suggested to run MCU in fast clock operation with DRAM application.

J. Application Circuit

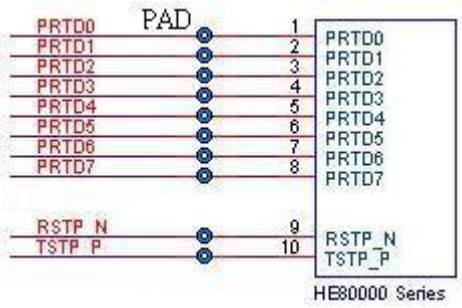


K. Important Note

1. For accessing any address large than 64KB, users must update TPP first, TPH then TPL. Only by this order, the pre-charge circuit of ROM will work correctly. 5us waiting is necessary before LDV instruction is executed since Data ROM is a low speed ROM. Users can not emulate this accessing process in ICE. So 5us delay should be added by firmware.

2. LCD driving circuit must be turn off before IC goes into sleep mode.

3. Please bonds the TSTP_P, RSTP_N and PRTD[7:0] with test point on PCB (can be soldered and probed) as you can, then KB can do some IC testing job on PCB. Neither VDD nor GND connection is necessary for TSTP_P. The following figure is an example (Testing point with through hole).



4. LV3 must small than 9.0 Volt. Otherwise IC may breakdown.

L. Updated Record

Version	Date	Section	Original Content	New Content
V3.2	Nov 28, 2001	B, H	2.2V (VDD operation voltage)	2.4V
		A, B	ROM: 192K Bytes	ROM: 256K Bytes
		K, L	New Section	