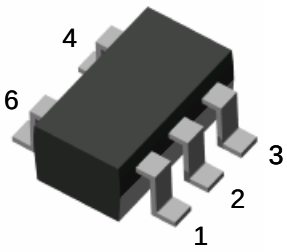
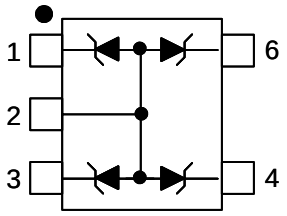
PRELIMINARY

QUAD TVS/ZENER FOR ESD AND LATCH-UP PROTECTION

This Quad TVS/Zener Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 4 data lines where the board space is a premium.





SC70-5L

SPECIFICATION FEATURES

- **150W Power Dissipation (8/20µs Waveform)**
- **Very Low Leakage Current, Maximum of 5µA @ 5Vdc**
- **Very low Clamping voltage (Max of 10V @ 14A 8/20µs)**
- **IEC61000-4-2 ESD 15kV air, 8kV Contact Compliance**
- **Industry standard SOT353 (Also known as SC70-5L)**

APPLICATIONS

- **Personal Digital Assistant (PDA)**
- **SIM Card Port Protection (Mobile Phone)**
- **Portable Instrumentation**
- **Mobile Phones and Accessories**
- **Computer Data Ports**

MAXIMUM RATINGS

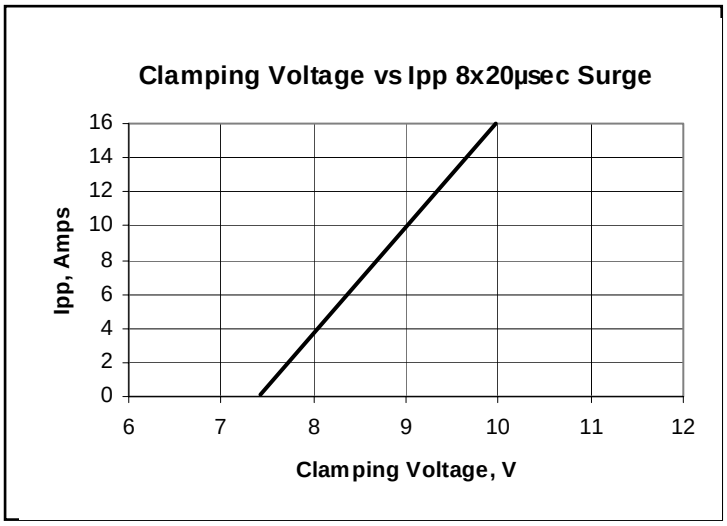
Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	150	W
Peak Pulse Current (8/20µs Waveform)	I_{pp}	14	A
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

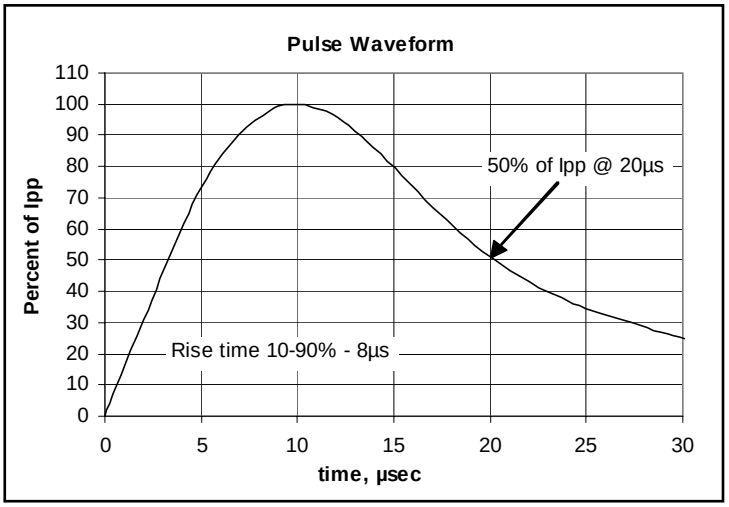
ELECTRICAL CHARACTERISTICS Tj = 25°C

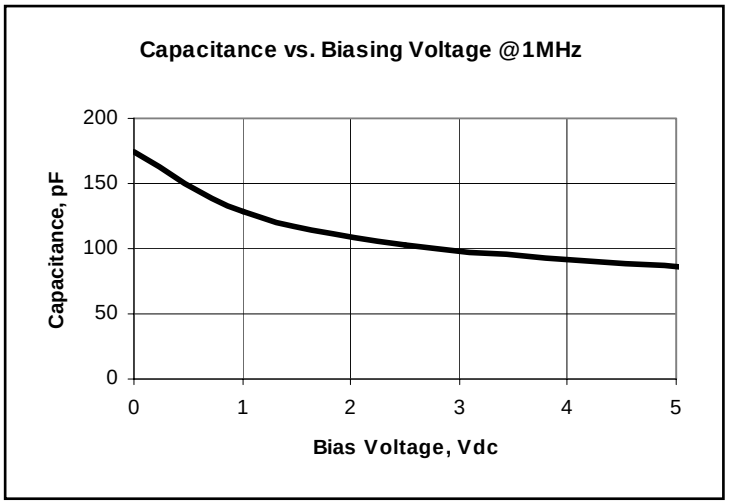
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	v
Reverse Breakdown Voltage	V_{BR}	I_{BR} =1 mA	6.2		7.2	V
Reverse Leakage Current	I_R	V_R = 5V			5	µA
Clamping Voltage (8/20µs)	V_c	I_{pp} = 5 Amps			8.6	V
Clamping Voltage (8/20µs)	V_c	I_{pp} = 10 Amps			9.1	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 7			180	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 7			90	pF

PRELIMINARY

TYPICAL CHARACTERISTICS

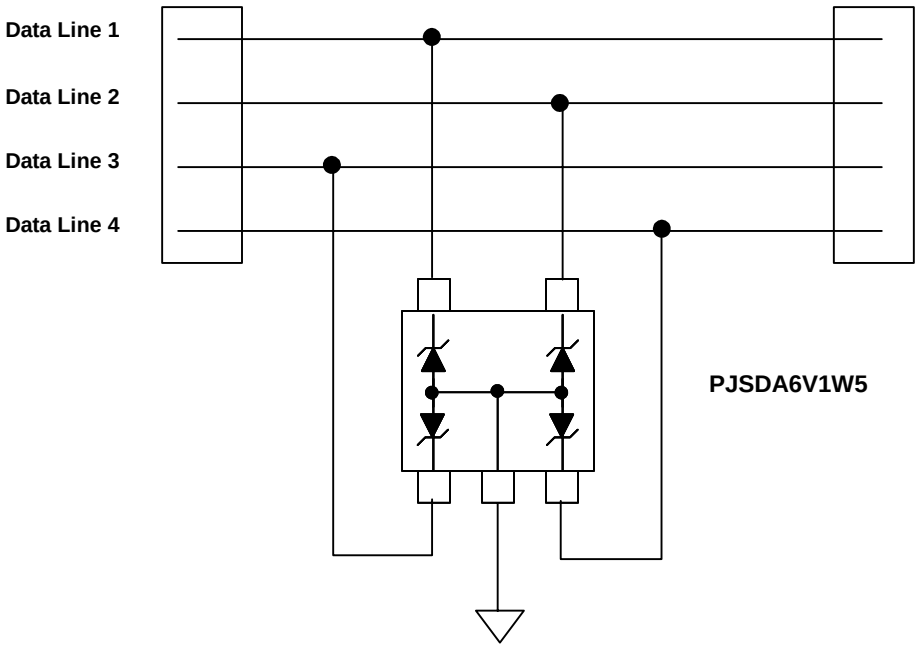






PRELIMINARY

TYPICAL APPLICATION EXAMPLE AND PACKAGE LAYOUT DIMENSIONS



SIM Card Port or Phone Port

SOT-353 Unit: inch (mm)