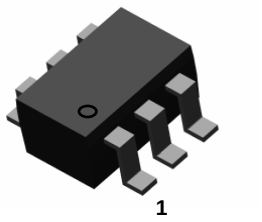
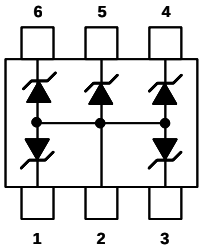
PANJIT SEMI CONDUCTOR

PRELIMINARY

5-TVS/ZENER ARRAY FOR ESD AND LATCH-UP PROTECTION

This 5-TVS/Zener Array has been designed to Protect Sensitive Equipment against ESD and to prevent Latch-Up events in CMOS circuitry operating at 5Vdc and below. This TVS array offers an integrated solution to protect up to 5 data lines where the board space is a premium.





SOT363

SPECIFICATION FEATURES

- **100W Power Dissipation (8/20µs Waveform)**
- **Low Leakage Current, Maximum of 0.5µA @ 5Vdc**
- **Very Low Clamping Voltage, Max of 10V @ 9Apk 8/20µs**
- **IEC61000-4-2 ESD 20kV air, 15kV Contact Compliance**
- **Max off state Capacitance of 90pF @ 0Vdc 1 MHz**
- **-Industry Standard Surface Mount Package SOT363 (SC70-6L)**

APPLICATIONS

- **Personal Digital Assistant (PDA)**
- **SIM Card Port Protection (Mobile Phone)**
- **Portable Instrumentation**
- **Mobile Phones and Accessories**
- **Memory Card Port Protection**

MAXIMUM RATINGS (Per Device)

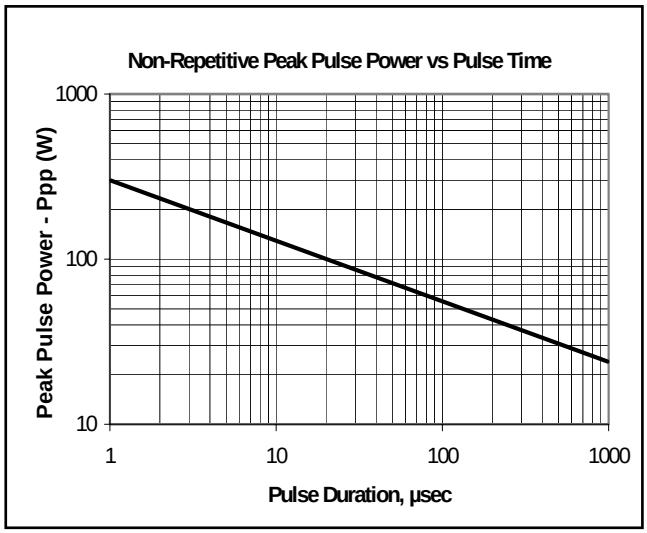
Rating	Symbol	Value	Units
Peak Pulse Power (8/20µs Waveform)	P_{pp}	100	W
Peak Pulse Current (8/20µs Waveform)	I_{pp}	10	A
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-55 to +150	°C
Storage Temperature Range	T_{stg}	-55 to + 150	°C

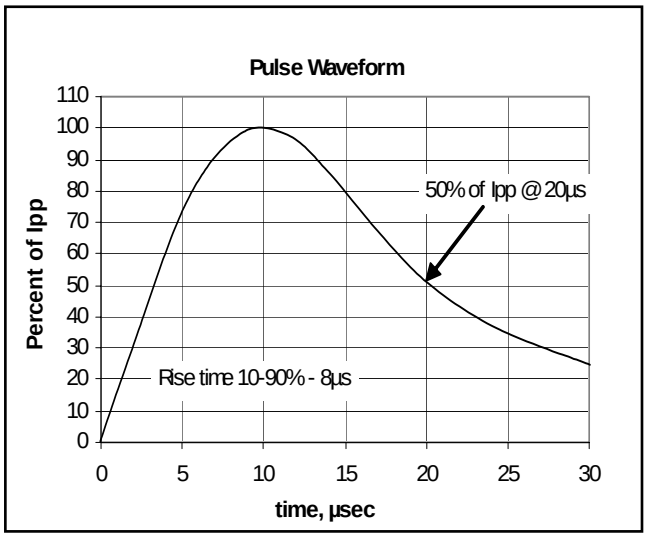
ELECTRICAL CHARACTERISTICS (Per Device) Tj = 25°C

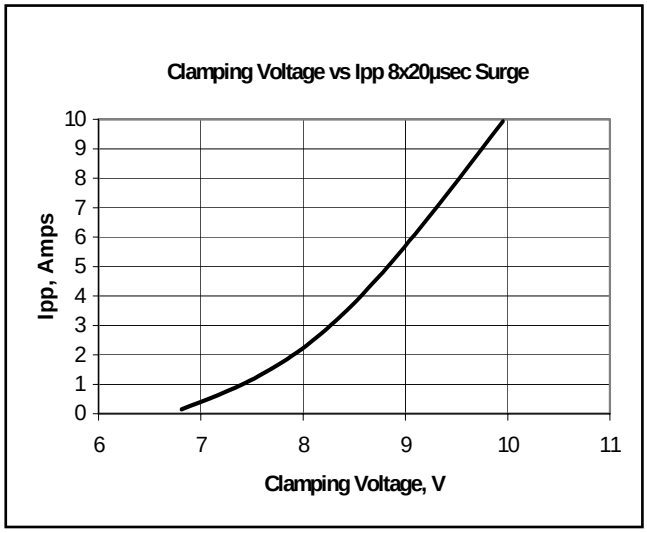
Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_{BR} = 1 mA	6		7.2	V
Reverse Leakage Current	I_R	V_R = 5V			0.5	µA
Clamping Voltage (8/20µs)	V_{cl}	I_{pp} = 5A			9	V
Clamping Voltage (8/20µs)	V_{cl}	I_{pp} = 9A			10	V
Off State Junction Capacitance	Cj	0 Vdc Bias f = 1MHz Between I/O pins and pin 2			90	pF
Off State Junction Capacitance	Cj	5 Vdc Bias f = 1MHz Between I/O pins and pin 2			45	pF

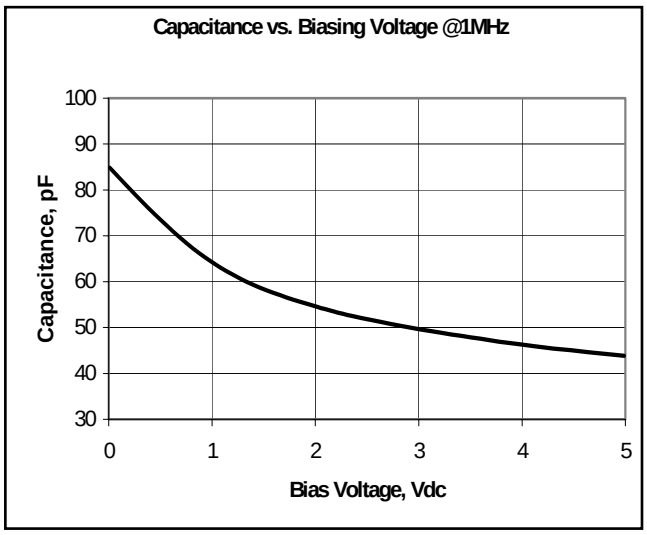
PRELIMINARY

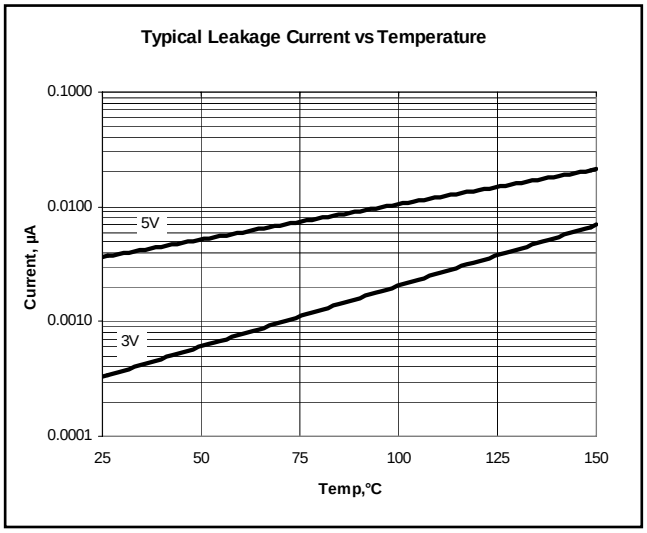
TYPICAL CHARACTERISTICS 25°C unless otherwise noted





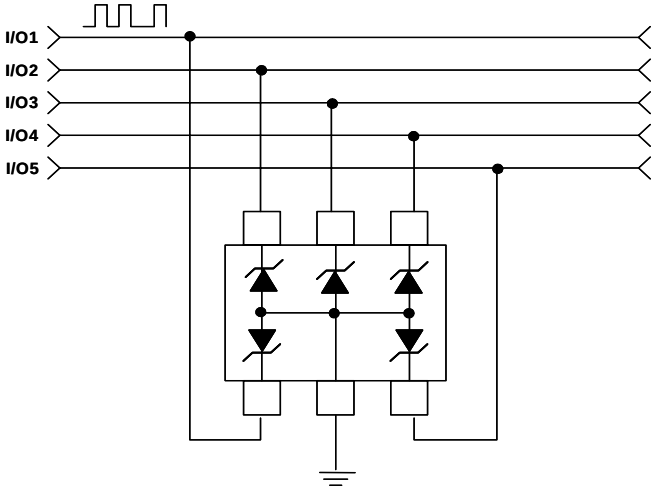






PRELIMINARY

TYPICAL APPLICATION EXAMPLE



Ground (Pin 2)

PACKAGE LAYOUT DIMENSIONS