DFPIC1655X

High Performance Configurable 8-bit RISC Microcontroller
ver 2.02

OVERVIEW

The DFPIC1655X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated for operation with **fast memory** (typically on-chip). The core has been designed with a special concern about **low power consumption**.

The DFPIC1655X is software compatible with the industry standard PIC16C554 and PIC16C558. It employs a modified RISC architecture (2 times faster than original implementation).

The DFPIC1655X have enhanced core features, configurable hardware stack, and multiple internal and external interrupt sources. The separate instruction and data buses allow a 14 bit wide instruction word with the separate 8 -bit wide data. The DFPIC1655X typically achieve a 2:1 code compression and a 8:1 speed improvement over other 8-bit microcontrollers in their class.

The power-down mode SLEEP allow user to reduce power consumption. User can wake up the controller from SLEEP through several external and internal interrupt and reset. An integrated Watchdog Timer with it's own clock signal provides protection against software lock-up.

The DFPIC1655X Microcontroller fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. Built-in power save mode and small used area in programmable devices make this IP perfect for applications applications with space and power consumption limitations.

DFPIC1655X is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow

CPU FEATURES

- Software compatible with industry standard PIC16C55X

- Harvard architecture 2 times faster compared to original implementation

- 35 instructions

- 14 bit wide instruction word

- Up to 512 bytes of internal Data Memory

- Up to 64K bytes of Program Memory

- Configurable hardware stack

- Power saving SLEEP mode

- Fully synthesizable, static synchronous design with no internal tri-states

- Scan test ready

- Technology independent HDL Source Code

http://www.DigitalCoreDesign.com
http://www.dcd.pl

PERIPHERALS

- Two 8 bit I/O ports
  - *Four 8-bit corresponding TRIS registers*
  - *Interrupt feature on PORTB(7:4) change*
- Timer 0
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
  - *Edge select for external clock*
- Watchdog Timer
  - *Configurable Time out period*
  - *7-bit software programmable prescaler*
  - *Dedicated independent Watchdog Clock input*
- Interrupt Controller
  - *Three individually maskable Interrupt sources*
    - *External interrupt INT*
    - *Timer Overflow interrupt*
    - *Port B[7:4] change interrupt*
- DoCD™ debug unit
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
    - *Hardware Stack and Stack Pointer*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
  - *Hardware breakpoints activated at a certain*
    - *Program address (PC)*
    - *Address by any write into memory*
    - *Address by any read from memory*
    - *Address by write into memory a required data*
    - *Address by read from memory a required data*
  - *Three wire communication interface*

CONFIGURATION

The following parameters of the DFPIC1655X core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

MEMORY Type	- synchronous - asynchronous
Number of hardware stack levels	- 1-16 - default 4
Program Memory size	- up 64 kWords - default 8k
SLEEP mode	- used - unused
WATCHDOG Timer	- used / width - unused
Timer system	- used - unused
PORTS A,B	- used - unused
DoCD™ Debug Unit	- used - unused

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted Megafunction or/and
  - plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

http://www.DigitalCoreDesign.com
http://www.dcd.pl

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

SYMBOL
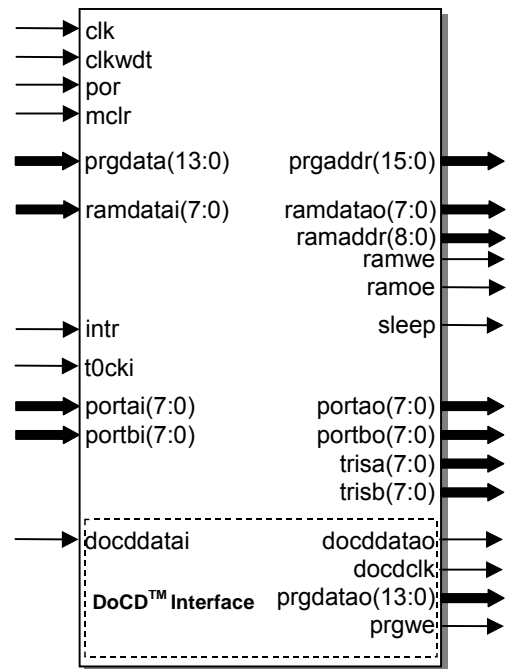
PINS DESCRIPTION

| PIN	TYPE	DESCRIPTION
clk	input	Global clock
clkwdt	input	Watchdog clock
por	input	Global reset Power On Reset
mclr	input	User reset
prgdata[13:0]	input	Data bus from program memory
ramdati[7:0]	input	Data bus from int. data memory
intr	input	External interrupt
t0cki	input	Timer 0 input
portax[7:0]	input	Port X input
docddatai	input	DoCD™ Debugger input
prgaddr[15:0]	output	Program memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramaddr[8:0]	output	RAM address bus
ramwe	output	Data memory write
ramoe	output	Data memory output enable
sleep	output	Sleep signal
portxo[7:0]	output	Port X output
trisx[7:0]	output	Data direction pins for Port X
docddatao	output	DoCD™ Debugger data output
docdclk	output	DoCD™ Clock line
prgdatao[13:0]	output	Program Memory data output
prgwe	output	Program Memory write enable

BLOCK DIAGRAM

ALU – Arithmetic Logic Unit performs arithmetic and logic operations during execution of an instruction. This module contains work register (W) and Status register.

Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.

Hardware Stack – The DFPIC1655X configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack when CALL instruction is executed or an interrupt causes a branch. The stack is popped while RETURN, RETFIE and RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push.
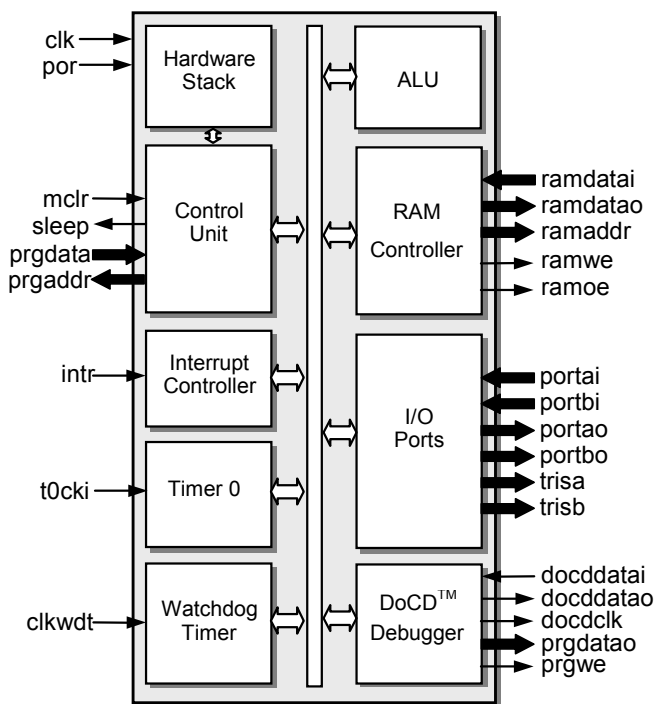
RAM Controller – It performs interface functions between Data Memory and DFPIC1655X internal logic. It assures correct Data memory addressing and data transfers. The DFPIC1655X supports two addressing modes: direct or indirect. In Direct Addressing the 9-bit direct address is computed from RP(1:0) bits (STATUS) and 7 least significant bits of in-struction word. Indirect addressing is possible by using the INDF register. Any instruction using INDF register actually accesses data pointed to by the file select register FSR. Reading INDF register indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation. An effective 9-bit address is obtained by concatenating the IRP bit (STATUS) and the 8-bit FSR register.

Interrupt Controller – Interrupt Controller module is responsible for interrupt manage system for the external and internal interrupt sources. It contains interrupt related register called INTCON The DFPIC1655X has three interrupt sources:

♦ External interrupt INT
♦ TMR0 overflow interrupt
♦ PORTB change interrupt (pins B7:B4)

The interrupt control register INTCON records individual interrupt requests in flag bits.
A global interrupt enable bit, GIE enables all unmasked interrupts. Each interrupt source has an individual enable bit, which can enable or disable corresponding interrupt.
When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. The interrupt flag bits must be cleared in software before re-enabling interrupts.

Timer 0 – Main system's timer and prescaler. The DFPIC1655X Timer operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer registers are incremented every 2 CLK periods. When the prescaler is assigned into the TIMER prescale ration can be divided by 2, 4 .. 256. In the "counter mode" the timer register is incremented every falling or rising edge of T0CKI pin, dependent on T0SE bit in OPTION register.

Watchdog Timer – it's a free running timer. WDT has own clock input separate from system clock. It means that the WDT will run even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT time-out generates a Watchdog reset. If the device is in SLEEP mode the WDT time-out causes the device to wake-up and continue with normal operation.

I/O Ports – Block contains DFPIC1655X's general purpose I/O ports and data direction registers (TRIS). The DFPIC1655X has two 8-bit full bi-directional ports PORT A, PORT B. Read and write accesses to the I/O port are performed via their corresponding SFR's PORTA, PORTB. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has an corresponding bit in TRISA and TRISB registers. When the bit of TRIS register is set this means that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

OPTIONAL MODULES

There are also available an optional peripherals, not included in presented DFPIC1655X Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- Full duplex UART
- SPI – Master and Slave Serial Peripheral Interface
- PWM – Pulse Width Modulation Timer
- I2C bus controller – Master / Slave

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	660	99 MHz
CYCLONE II	-6	663	91 MHz
STRATIX	-5	661	106 MHz
STRATIX II	-3	591	122 MHz
STRATIX GX	-5	661	101 MHz
APEX II	-7	804	71 MHz
APEX20KC	-7	739	61 MHz
APEX20KE	-1	739	56 MHz
APEX20K	-1	739	50 MHz
ACEX1K	-1	804	39 MHz
FLEX10KE	-1	804	38 MHz

Core performance in ALTERA® devices

IMPROVEMENT

Most instruction of DFPIC1655X is executed within 2 CLK cycles. Except the conditional program memory branches in case that the condition of branch instruction is met. The table below shows sample instructions execution times:

Mnemonic operands	DFPIC1655X (CLK cycles)	PIC16C554 (CLK cycles)	Impr.
ADDWF	2	4	2
ANDWF	2	4	2
RLF	2	4	2
BCF	2	4	2
DECFSZ	2(4)[1]	4(8)[1]	2
INCFSZ	2(4)[1]	4(8)[1]	2
BTFSC	2(4)[1]	4(8)[1]	2
BTFSS	2(4)[1]	4(8)[1]	2
CALL	2	8	4
GOTO	2	8	4
RETFIE	2	8	4
RETLW	2	8	4
RETURN	2	8	4

[1] **number of clock in case that result of operation is 0.**

http://www.DigitalCoreDesign.com
http://www.dcd.pl

DFPIC&DRPIC FAMILY OVERVIEW

The family of DCD DFPICXX & DRPICXX IP Cores combine a high–performance, low cost, and small compact size, offering the best price/performance ratio in the IP Market. The DCD's Cores are dedicated for use in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

DCD's DFPICXX & DRPICXX IP Cores family contains four 8-bit microcontroller Cores to best meet your needs: DFPIC165X 12-bit program word, DFPIC1655X 14-bit program word, and DRPIC1655X and DRPIC166X single cycle microcontrollers with 14-bit program word. All three microcontroller cores are binary compatible with widely accepted PIC16C5X and PIC16CXXX. They employ a modified RISC architecture two or four times faster than the original ones.

The DFPICXXX & DRPICXX IP Cores are written in pure VHDL/VERILOG HDL languages which make them technologically independent. All of the DFPICXX & DRPICXX family members supports a power saving SLEEP mode and allows the user to configure the watchdog time-out period and a number of hardware stack levels. DFPICXX & DRPICXX can be fully customized according to customer needs.

Design	Program Memory space	Data Memory space	Program word length	Number of instructions	I/O Ports	Timer 0	Timer 1	Timer 2	Watchdog Timer	CCP1	USART	Sleep Mode	External interrupts	Internal Interrupts	Levels of hardware stack	Wake up on port pin change	Speed rate	DoCD™ Debugger	Size (gate)
DFPIC 165X	2k	128	12	33	24	✓	-	-	✓	-	-	✓	-	-	2	-	2	-	2 700
DFPIC 1655X	64k	512	14	35	16	✓	-	-	✓	-	-	✓	5	1	8	✓	2	✓*	3 900
DRPIC 1655X	64k	512	14	35	32	✓	-	-	✓	-	-	✓	5	1	8	✓	4	✓*	4 800
DRPIC 166X	64k	512	14	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	8	✓	4	✓*	6 700

Optional

DFPIC & DRPIC family of High Performance Microcontroller Cores

C O N T A C T S

For any modification or special request please contact to Digital Core Design or local distributors.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check http://www.dcd.pl/apartn.php