DFPIC165X

High Performance
8-bit RISC Microcontroller
ver 2.01

O V E R V I E W

The DFPIC165X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated for operation with **fast memory** (typically on-chip). The core has been designed with a special concern about **low power consumption**.

The DFPIC165X is software compatible with the industry standard PIC16C54, PIC16C55, PIC16C56, PIC16C57 and PIC16C58. It employs a modified RISC architecture (2 times faster than original implementation).

The DFPIC165X have enhanced core features and configurable hardware stack. The separate instruction and data buses allow a 12 bit wide instruction word with the separate 8 -bit wide data. The DFPIC165X typically achieve a 2:1 code compression and a 8:1 speed improvement over other 8-bit microcontrollers in its class. The Core has 24 I/O lines and an 8-bit timer/counter with an 8-bit programmable prescaller.

The power-down mode SLEEP allow user to reduce power consumption. User can wake up the controller from SLEEP through an user reset or watchdog overflow. An integrated Watchdog Timer with it's own clock signal provides protection against software lock-up.

The DFPIC165X Microcontroller fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. Built-in power save mode and small used area in programmable devices make this IP perfect for applications applications with space and power consumption limitations.

DFPIC165X is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow.

C P U   F E A T U R E S

- Software compatible with industry standard PIC16C5X

- Harvard architecture 2 times faster compared to original implementation

- 33 instructions

- 12 bit wide instruction word

- Up to 256 bytes of internal Data Memory

- Up to 4K bytes of Program Memory

- Configurable hardware stack

- Power saving SLEEP mode

- Fully synthesizable, static synchronous design with no internal tri-states

- Scan test ready

http://www.DigitalCoreDesign.com
http://www.dcd.pl

PERIPHERALS

- Three 8 bit I/O ports
  - *Three 8-bit corresponding TRIS registers*
- Timer 0
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Edge select for external clock*
- Watchdog Timer
  - *Configurable Time out period*
  - *7-bit software programmable prescaler*
  - *Dedicated independent Watchdog Clock input*

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted Megafunction or/and
  - plain text EDIF
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

CONFIGURATION

The following parameters of the DFPIC165X core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

Parameter	Options
RAM memory type	- synchronous - asynchronous
RAM size	- up to 256 - default 128
Program Memory size	- up 4 kWords - default 2k
Number of hardware stack levels	- 1-8 - default 2
SLEEP mode	- used - unused
WATCHDOG Timer	- used / width - unused
Timer system	- used - unused
PORTS A,B,C	- used - unused

PINS DESCRIPTION

| PIN	TYPE	DESCRIPTION
clk	input	Global clock
clkwdt	input	Watchdog clock
por	input	Global reset Power On Reset
mclr	input	User reset
prgdata[11:0]	input	Data bus from program memory
ramdati[7:0]	input	Data bus from int. data memory
t0cki	input	Timer 0 input
portai[7:0]	input	Port A input
portbi[7:0]	input	Port B input
portci[7:0]	input	Port C input
prgdata[11:0]	input	Data bus from program memory
ramdati[7:0]	input	Data bus from int. data memory
prgaddr[11:0]	output	Program memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramaddr[7:0]	output	RAM address bus
ramwe	output	Data memory write
ramoe	output	Data memory output enable
sleep	output	Sleep signal
portao[7:0]	output	Port A output
portbo[7:0]	output	Port B output
portco[7:0]	output	Port C output
trisa[7:0]	output	Data direction pins for Port A
trisb[7:0]	output	Data direction pins for Port B
trisc[7:0]	output	Data direction pins for Port C

SYMBOL

BLOCK DIAGRAM
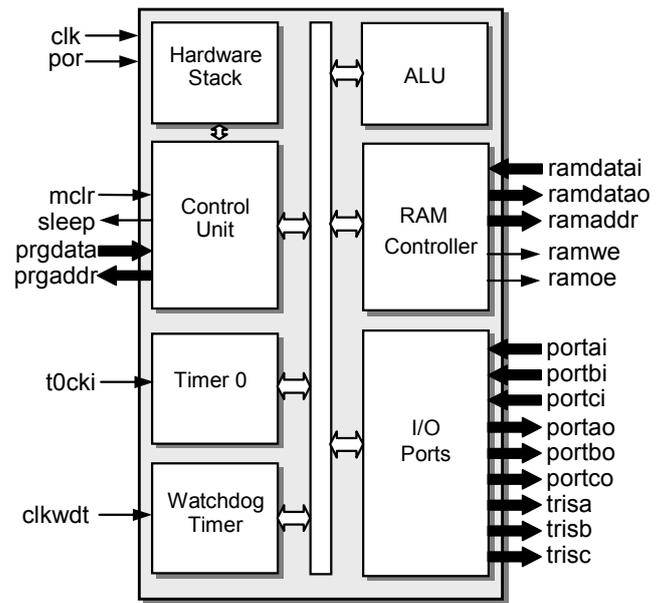
ALU – Arithmetic Logic Unit performs arithmetic and logic operations during execution of an instruction. This module contains work register (W) and Status register.

Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.

Hardware Stack – The DFPIC165X configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack when CALL instruction is executed or an interrupt causes a branch. The stack is popped while RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed two times, the third push overwrites the value that was stored from the first push.

RAM Controller – It performs interface functions between Data Memory and DFPIC165X internal logic. It assures correct Data memory addressing and data transfers. The DFPIC165X supports two addressing modes: direct or indirect. In Direct Addressing the 8-bit direct address is computed from FSR(7:5) bits 5 least significant bits of instruction word.
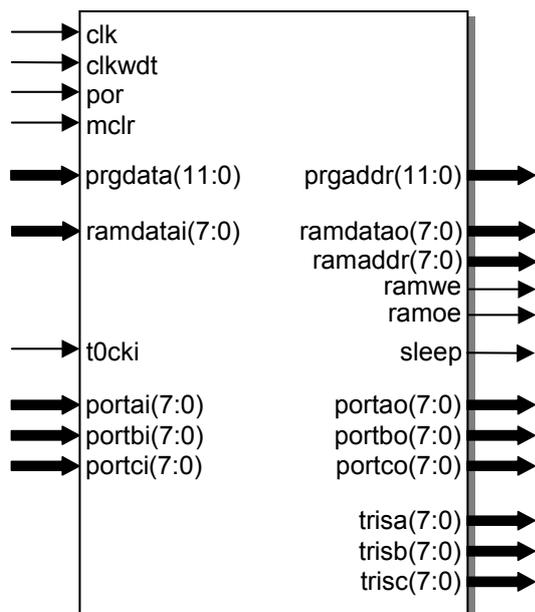
Indirect addressing is possible by using the INDF register. Any instruction using INDF register actually accesses data pointed to by the file select register FSR. Reading INDF register indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation. An effective 8-bit address is obtained from an 8-bit FSR register.

Timer 0 – Main system's timer and prescaler. The DFPIC165X Timer operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer registers are incremented every 4 CLK periods. When the prescaler is assigned into the TIMER prescale ration can be divided by 2, 4 .. 256. In the "counter mode" the timer register is incremented every falling or rising edge of T0CKI pin, dependent on T0SE bit in OPTION register.

Watchdog Timer – it is a free running timer. WDT has own clock input separate from system clock. It means that the WDT will run even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT timeout generates a Watchdog reset. If the device is in SLEEP mode the WDT timeout causes the device to wake-up and continue with normal operation.

I/O Ports – Block contains DFPIC165X's general purpose I/O ports and data direction registers (TRIS). The DFPIC165X has three 8-bit full bi-directional ports PORT A, PORT B and PORT C. Read and write accesses to the I/O port are performed via their corresponding SFR's PORTA, PORTB, PORTC. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has an corresponding bit in TRISA, TRISB and TRISC registers. When the bit of TRIS register is set this means that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

OPTIONAL PERIPHERALS

There are also available an optional peripherals, not included in presented DFPIC165X Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- Full duplex UART
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- PWM – Pulse Width Modulation Timer
  - *2 independent 8-bit PWM channels, concatenated on one 16-bit PWM channel*
  - *Software-selectable duty from 0% to 100% and pulse period*
  - *Software-selectable polarity of output waveform*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kbs*
  - *FAST speed 400 kbs*
  - *HIGH speed 3400 kbs*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	551	105 MHz
CYCLONE II	-6	547	108 MHz
STRATIX	-5	551	108 MHz
STRATIX II	-3	456	178 MHz
STRATIX GX	-5	551	109 MHz
APEX II	-7	635	73 MHz
APEX20KC	-7	635	68 MHz
APEX20KE	-1	635	56 MHz
APEX20K	-1	635	45 MHz
ACEX1K	-1	648	50 MHz
FLEX10KE	-1	648	48 MHz

*CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, 256 B RAM, 4k of Program memory

Core performance in ALTERA® devices

IMPROVEMENT

Most instruction of DFPIC165X is executed within 2 CLK cycles. Except the conditional program memory branches in case that the condition of branch instruction is met. The table below shows sample instructions execution times:

Mnemonic operands	DFPIC165X (CLK cycles)	PIC16C54 (CLK cycles)	Impr.
ADDWF	2	4	2
ANDWF	2	4	2
RLF	2	4	2
BCF	2	4	2
DECFSZ	2(4)[1]	4(8)[1]	2
INCFSZ	2(4)[1]	4(8)[1]	2
BTFSC	2(4)[1]	4(8)[1]	2
BTFSS	2(4)[1]	4(8)[1]	2
CALL	2	8	4
GOTO	2	8	4
RETLW	2	8	4

[1] - number of clock in case that result of operation is 0.

DFPIC&DRPIC FAMILY OVERVIEW

The family of DCD DFPICXX & DRPICXX IP Cores combine a high–performance, low cost, and small compact size, offering the best price/performance ratio in the IP Market. The DCD's Cores are dedicated for use in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

DCD's DFPICXX & DRPICXX IP Cores family contains four 8-bit microcontroller Cores to best meet your needs: DFPIC165X 12-bit program word, DFPIC1655X 14-bit program word, and DRPIC1655X and DRPIC166X single cycle microcontrollers with 14-bit program word. All three microcontroller cores are binary compatible with widely accepted PIC16C5X and PIC16CXXX. They employ a modified RISC architecture two or four times faster than the original ones.

The DFPICXXX & DRPICXX IP Cores are written in pure VHDL/VERILOG HDL languages which make them technologically independent. All of the DFPICXX & DRPICXX family members supports a power saving SLEEP mode and allows the user to configure the watchdog time-out period and a number of hardware stack levels. DFPICXX & DRPICXX can be fully customized according to customer needs.

Design	Program Memory space	Data Memory space	Program word length	Number of instructions	I/O Ports	Timer 0	Timer 1	Timer 2	Watchdog Timer	CCP1	USART	Sleep Mode	External interrupts	Internal Interrupts	Levels of hardware stack	Wake up on port pin change	Speed rate	DoCD™ Debugger	Size (gate)
DFPIC165X	2k	128	12	33	24	✓	-	-	✓	-	-	✓	-	-	2	-	2	-	2 700
DFPIC1655X	64k	512	14	35	16	✓	-	-	✓	-	-	✓	5	1	8	✓	2	✓*	3 900
DRPIC1655X	64k	512	14	35	32	✓	-	-	✓	-	-	✓	5	1	8	✓	4	✓*	4 800
DRPIC166X	64k	512	14	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	8	✓	4	✓*	6 700

* Optional

DFPIC & DRPIC family of High Performance Microcontroller Cores

http://www.DigitalCoreDesign.com
http://www.dcd.pl

C O N T A C T S

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